Irfu

cea

saclay

Recent Front-end developments at Saclay

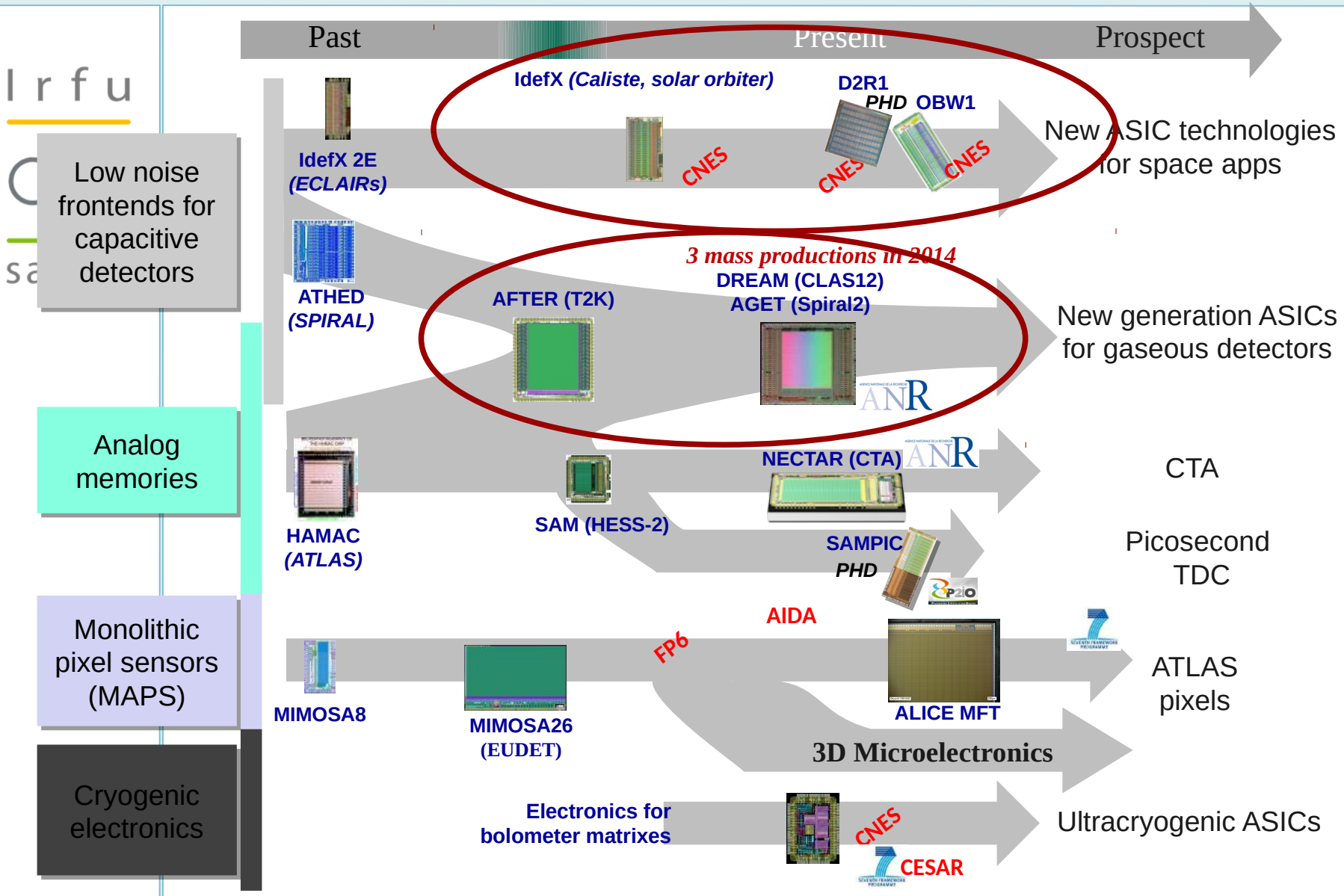
Damien Neyret, on behalf of the SEDI Microelectronics group

(particularly O. Gevin, P. Baron)

CEA Saclay IRFU/SPhN

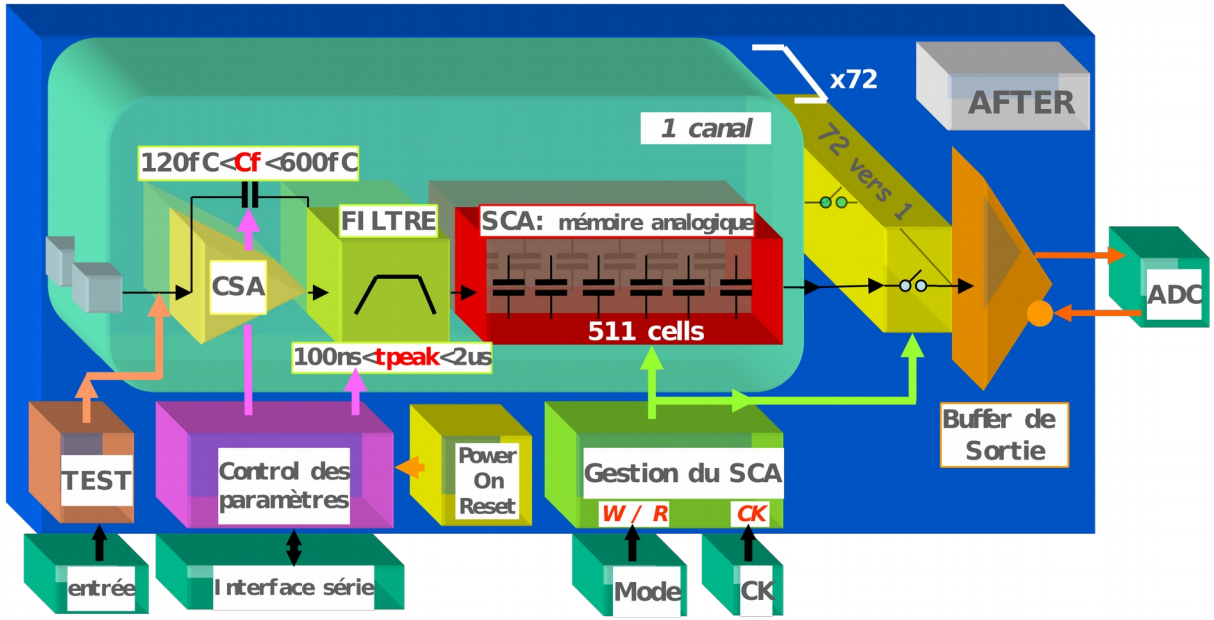
9/11/2017

Front-end chips road-map



AFTER front-end chip

AFTER : developed for T2K TPC Micromegas



72 channels: analog part + memory (SCA)

- Analog part
  - Charge preamplifier + filtering
  - 4 gains; 16 peaking times; + ou - polarities
- Analog memory part
  - 511 cells deep
  - Fwrite < 100 Mhz; Fread = 20 Mhz

- Slow control
- Test:
  - 1 current input (calibration)
  - 1 voltage input (test or fonctionnal)
- Spy mode on channel 1

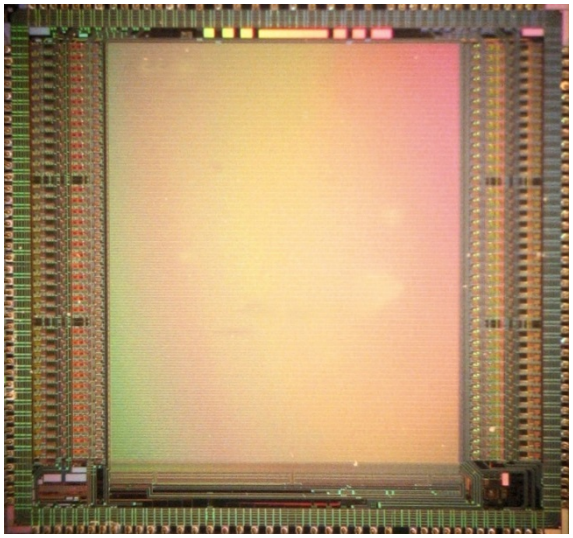
AFTER front-end chip

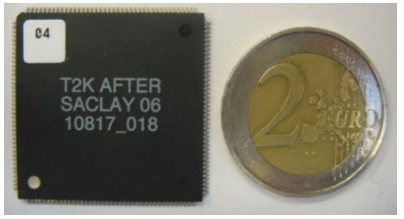
Specifications

Parameter	Value
Polarity of detector signal	Negative or Positive
Channels number	72
Charge measurement	
Input dynamic range	120 fC, 240 fC, 360 fC, 600 fC
Output dynamic range	2V p-p (differential)
I.N.L	< 2%
Resolution	< 850 e- (Gain: 120fC; Peaking Time: 200ns; Cinput < 30pF)
Sampling	
Peaking time	100 ns to 2 µs (16 values)
SCA time bin number	511
Sampling Frequency	1 MHz to 50 MHz
Readout	
Readout frequency	20 MHz
Channel Readout mode	All channels
SCA Readout mode	All
Test	
calibration	1 channel among 72; 1 external test capacitor
test	1 channel among 72; internal test capacitor (1 among 4)
functional	1 to 72(76) channels; 1 internal test capacitor per channel
Counting rate	< 0.3 Hz/channel
Power consumption	< 10 mW / channel @ 3.3V

Layout & package

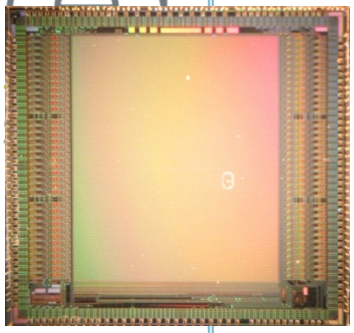
- Technology: AMS CMOS 0.35 µm
- Surface: 7.8 x 7.4 mm^2
- Number of transistors:# 500 000
- Package: LQFP 160 (28 x 28 x 1.4 mm)
- 2008: end of test production (5300)

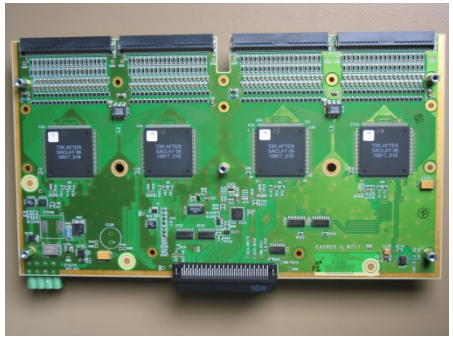


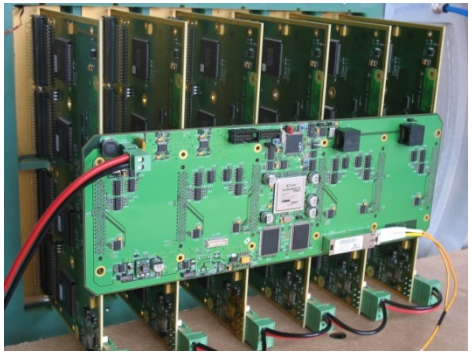


AFTER front-end chip

- Read-out electronics of the 3 T2K TPCs

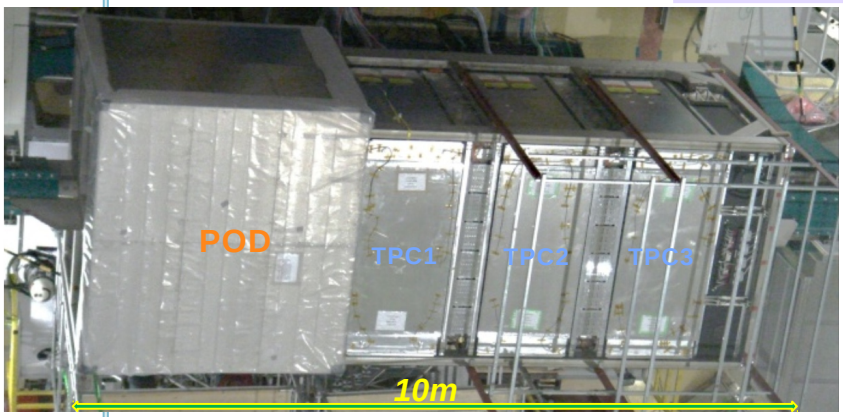


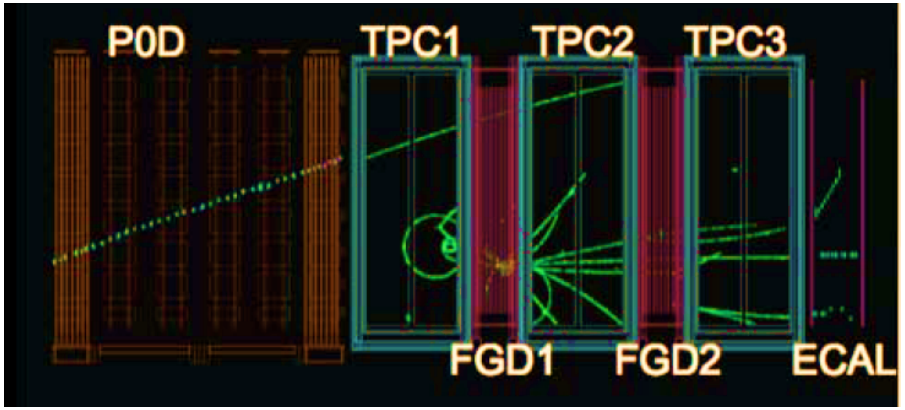




- ND280: Near detector

TOKAI : *1st detected event (19/12/2009)*





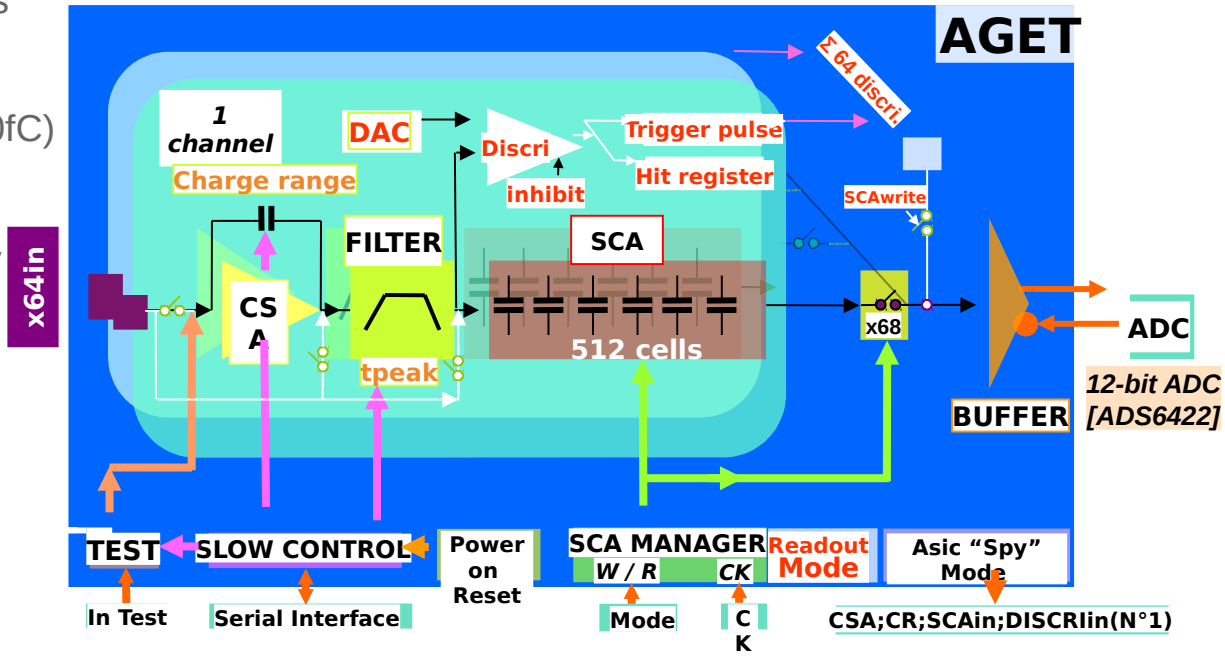
Also used for TRIUMF GD (SiPM read-out), ILC TPC tests, CAST, several R&D,...

AGET front-end chip

GET project : international collaboration to develop a modular read-out electronics for several types of TPC for nuclear experiments

AGET: AFTER ASIC + Discriminator + tunable analog memory read-out

- **64** (AFTER: 72) channels
- 4 Gains / channel:
  120 fC; 240 fC;
  1pC; **10 pC** (AFTER: 600fC)
- 16 filtering settings:
  50(100)ns à **1**(2) µs
- **512**(511) analog memory cells
- Sampling rates:
  1MHz to 100 MHz
- Read-out rate:
  25(20)MHz



- Auto trigger: discriminator + tunable threshold (3 global bits + 4 bits / channel)
- Multiplicity measurement: analog "OR" of the 64 discriminators
- Hit channels addresses
- SCA read-out modes: all, hit channels only, selected channels
- Read-out of 1 to 512 memory cells / trigger
- Possibility to short the CSA and input directly into RC2 filter or into SCA

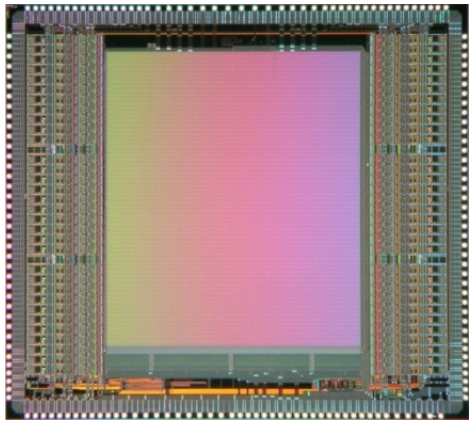
AGET front-end chip

Specifications

Parameter	Value
Polarity of detector signal	Negative or Positive
Channels number	64
External Preamplifier	Yes; access to the filter or SCA input (external CSA)
Charge measurement	
Input dynamic range	120 fC, 240 fC, 1 pC, 10 pC
Gain	Adjustable per channel
Output dynamic range	2V p-p (differential)
I.N.L	< 2%
Resolution	< 850 e- (Gain: 120fC; Peaking Time: 200ns; Cinput < 30pF)
Sampling	
Peaking time	50 ns to 1 µs (16 values)
SCA time bin number	512 or 2 x 256 cells
Sampling Frequency	1 MHz to 100 MHz
Multiplicity	
Multiplicity signal	Analog “OR” of 64 discriminator outputs
Input dynamic range	5% or 17.5% of input channel input charge range
I.N.L	< 5%
Threshold value	7-bit DAC [(3-bit + polarity bit) common DAC + 4-bit DAC/channel]
Readout	
Readout frequency	25 MHz
Channel Readout mode	Hit, selected or all
SCA Readout mode	1 to 512 cells
Test	
calibration	1 channel among 64; 1 external test capacitor
test	1 channel among 64; internal test capacitor (1 among 4)
functional	1 to 64(68) channels; 1 internal test capacitor per channel
Counting rate	< 1 kHz
Power consumption	< 10 mW / channel @ 3.3V

Layout & package

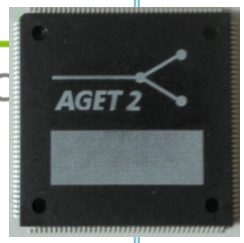
- Technology: AMS CMOS 0.35 µm
- Surface: 8,5 x 7,6 mm^2 [7,8 x 7,4 mm^2]
- Number de transistors:# 700 000 [500 000]
- Package: LQFP 160 (28 x 28 x 1.4 mm)
- 2014: end of test production (700 + 2500)

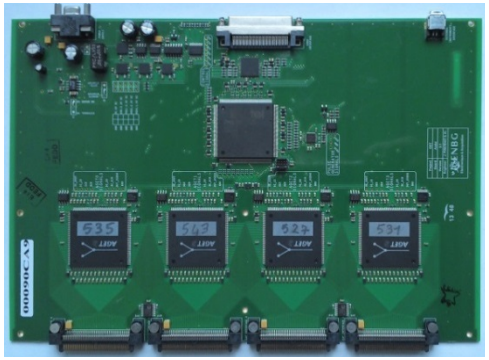


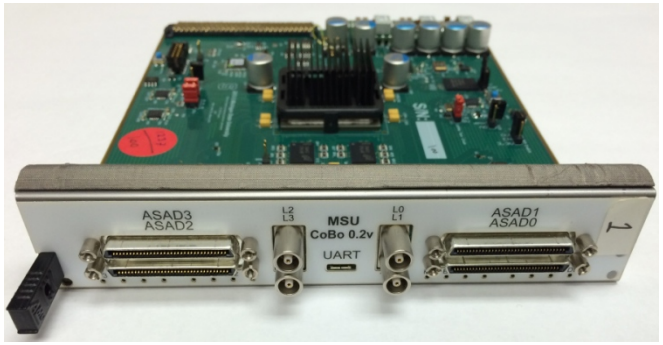
Also to mention **ASTRE** chip :

- derivative from AGET
- peaking times 70 ns to 8 µs
- space grade (HARPO project)
- produced and tested at low quantities

AGET front-end chip

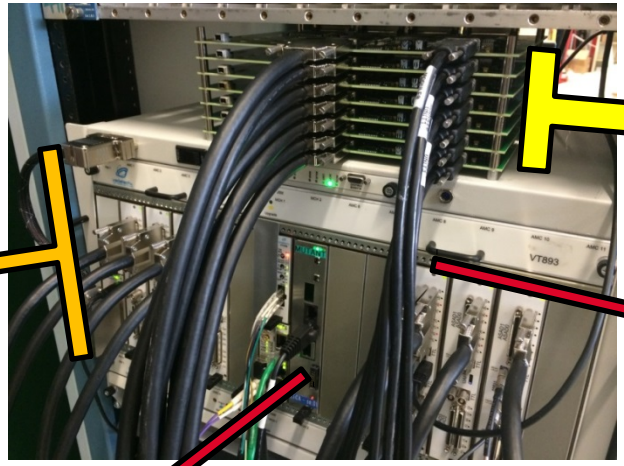






ASIC AGET ***AsAd card (ADC + data concentration)*** ***CoBo card (event building)***

AT-TPC test détecteur



AsAd

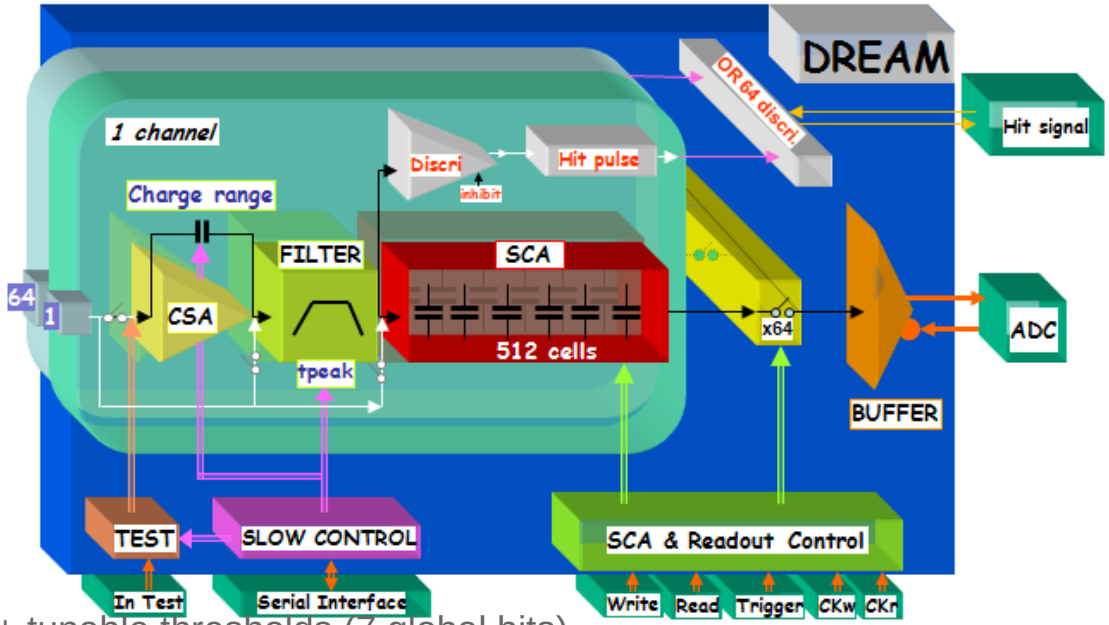
µTCA crate

CoBo

MuTanT card (trigger)

DREAM front-end chip

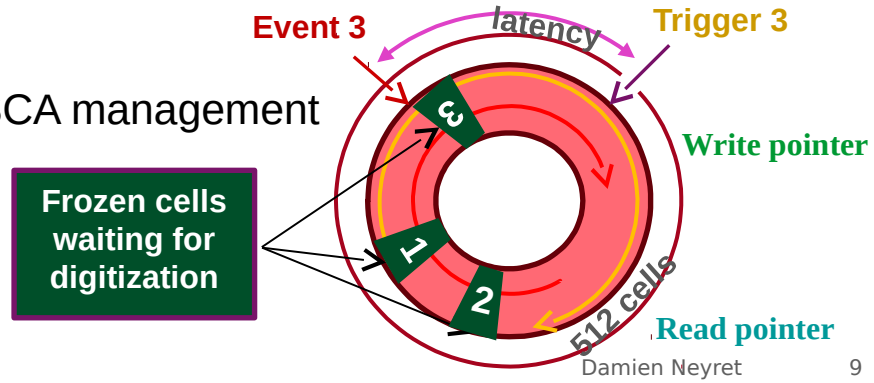
- 64 channels
- 4 gains / channel: 50 fC, 100 fC, 200 fC, 600fC
- 16 peaking times: 50 ns to 1 µs
- **512**(511) analog memory cells
- Sampling rates: 1MHz to 50 MHz
- Read-out rate: 20 MHz



- Auto trigger: discriminator + tunable thresholds (7 global bits)
- Multiplicity information: digital signal (LVDS); 8 multiplicity levels
- SCA read-out: only “trigged” cells of the 64 channels
- Possibility to short the CSA and input directly into RC2 filter or into SCA

DREAM ASIC
- developed for CLAS12 Micromegas
- stand high input capacity (> 200pF)
- large trigger and counting rates

SCA management



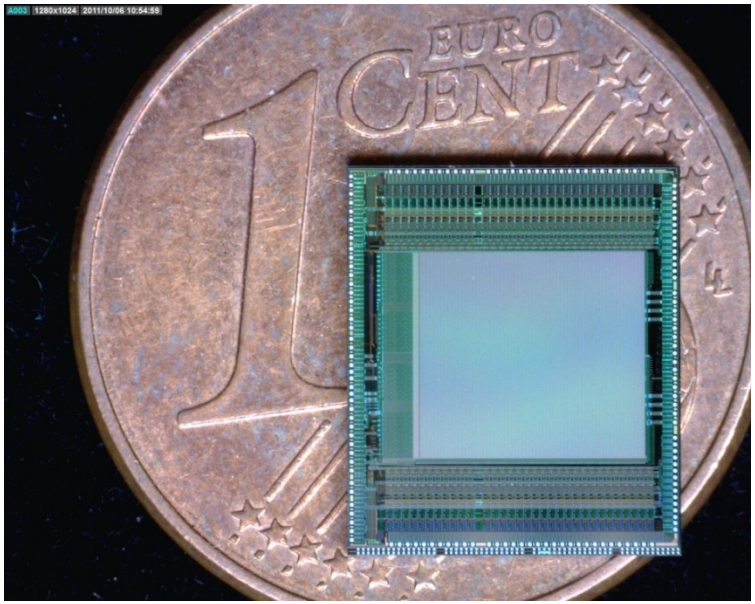
DREAM front-end chip

Specifications

Parameter	Value
Polarity of detector signal	Negative or Positive
Channels number	64
External Preamplifier	Yes; access to the filter or SCA input (external CSA)
Charge measurement	
Input dynamic range	50 fC, 100 fC, 200 fC, 600 fC
Gain	Adjustable per channel
Output dynamic range	2V p-p (differential)
I.N.L	< 2%
Resolution	< 2500 e- (Gain: 200fC; Peaking Time: 180ns; Cinput < 200pF)
Sampling	
Peaking time	50 ns to 900 ns (16 values)
SCA time bin number	512
Sampling Frequency	1 MHz to 50 MHz
Multiplicity	
Multiplicity signal	LVDS signal; 8 multiplicity levels
Input dynamic range	5% or 17.5% of input channel input charge range
I.N.L	< 5%
Threshold value	7-bit DAC + polarity bit
Readout	
Readout frequency	20 MHz
Channel Readout mode	All channels
SCA Readout mode	Triggered columns only
Test	
calibration	1 channel among 64; 1 external test capacitor
test	1 channel among 64; internal test capacitor (1 among 4)
functional	1 to 64 channels; 1 internal test capacitor per channel
Counting rate	< 50 kHz / channel
Trigger rate	Up to 20 kHz (4 samples read/trigger)
Power consumption	< 10 mW / channel @ 3.3V

Layout & package

- Technology: AMS CMOS 0.35 µm
- Surface: 8,6 x 7,5 mm^2
- Number of transistors:# 700 000
- Package: LQFP 128 (14 x 14 x 1,4 mm)
- 2014: end of test production (1600)



DREAM front-end chip

Off-detector frontend electronics
~1.5-2m

Synchronous
optical links

Concentrator electronics
~10-20m

Front-**E**nd **U**nit (FEU)

Back-**E**nd **U**nit (BEU)

Micro-coaxial
assemblies

CPU SD SSP SSP SSP T

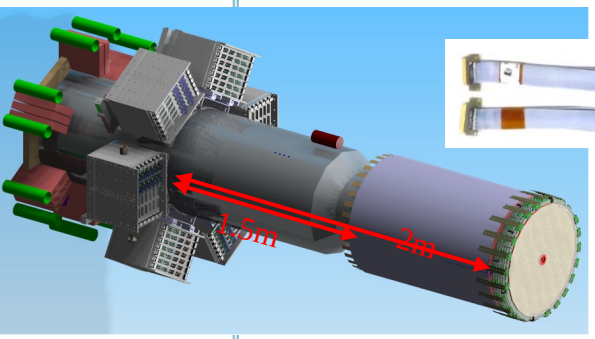
VXS / VME64

Adaptation of JLab developments

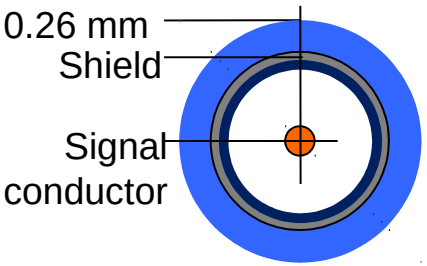
Development based on a new ASIC Dream

Trigger interface
optical fiber
← clock/ trigger
↔ fast control

DAQ interface
Ethernet
→ data
↔ slow control



Micro-coax flat cable



FEU

SSP

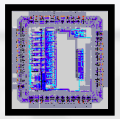
Comparison between chips

Parameter	AFTER	AGET	DREAM
Polarity of detector signal	Negative or Positive	Negative or Positive	Negative or Positive
Number of channels	72	64	64
External Preamplifier	No	Yes; access to the filter or SCA inputs	Yes; access to the filter or SCA inputs
Charge measurement			
Input dynamic range/gain	120 fC; 240 fC; 360 fC; 600 fC	120 fC; 240 fC; 1 pC; 10 pC /channel	50 fC; 100 fC; 200 fC; 600 fC /channel
Gain v.s Cdet (200pF)			
200 fC; tp = 230 ns	- 13%	- 13%	-0,9%
Sampling			
Peaking time value	100 ns to 2 µs (16 values)	50 ns to 1 µs (16 values) (ASTRE : 8µs)	50 ns to 900 ns (16 values)
Number of SCA Time bins	511	512	512
Sampling Frequency (WCk)	1 MHz to 100 MHz	1 MHz to 100 MHz	1 MHz to 50 MHz
Triggering			
Discriminator solution	No	Leading edge	Leading edge
HIT signal		OR of the 64 discri. outputs in LVDS level	OR of the 64 discri. outputs in LVDS level; 8 multiplicity levels
Threshold Range		5% or 17.5% of the dynamic range	5% or 17.5% of the dynamic range
Threshold value		(3-bit + polarity bit) common DAC + 4-bit DAC / channel	(7-bit + polarity bit) DAC common to all channels
Readout			
Readout frequency	20 MHz	25 MHz	Up to 20 MHz
Channel Readout mode	all channels	All, hit or selected	all channels
SCA cell Readout mode	all	1 to 512	Triggered columns only
Trigger rate			Up to 20kHz (4 samples read/trigger).
Counting rate	< 0.3 Hz / channel	< 1 kHz / channel	< 50 kHz / channel
Power consumption	< 10 mW / channel	< 10 mW / channel	< 10 mW / channel
Status	**Production**	**Production**	**Production**
Noise 120 fC; 200 ns peaking time	370 e- + 14.6 e- / pF (measured)	580 e- + 9 e- / pF (measured)	
Noise 200 fC; 200 ns peaking time	700 e- + 8.5 e- / pF (measured)		610 e- + 9 e- / pF (measured)
Electronics	T2K (AFTER + FEC + FEM) AFTER + FEC + evaluation kit AFTER + FEC + STUC AFTERSED	GET AGET + AsAd + rCoBo FEMINOS	DREAM + FEU + SSP DREAM + FEU + TCM

IDeF-X ASIC family

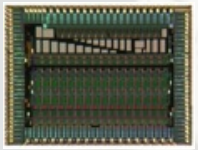
Very low noise chips for solid detectors, to be considered for ionization detection ?

AMS 0.35µm — **IDeF-X :spectrometry channel**

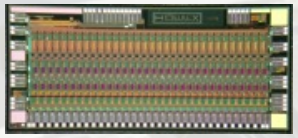


***V0**, Chip test, CSAs*

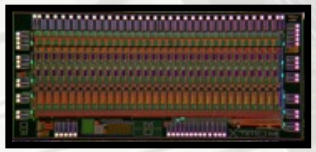
***V1.0** Full analog chains*



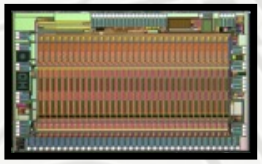
***V1.1** Analog + Mux / Caliste64*
System approach
Radiation evaluation



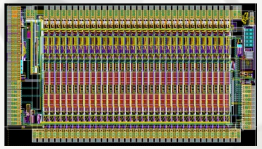
***V.2 – ECLAIRs** / Caliste 256*
Fully programmable
Space qualified



***BD** – SSL/CINEMA*
Fully programmable
Si or DSSD adapted



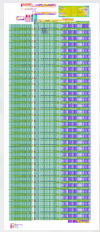
***HD** – Caliste HD*
Low Power
Fully programmable
HD-BD upcoming



***HD-LXE**–*
Low Power
Fully programmable
// outputs

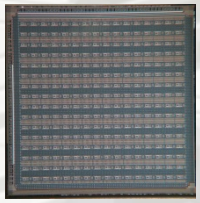
XFAB 0.18µm — **IDeF-X :spectrometry channel**

ADC



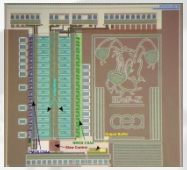
***OWB-1** – ADC //*
32 channel
13 bits
Low power
SEL hardened

Caterpylar
Chip test
Very low noise
Very low power



***D^2R_1**, 256 Pixels*
300×300 µm²
Auto-trigger
very low power.

AMS 0.18µm — **IDeF-X :spectrometry channel**



Caterpylar AMS
Chip test
Very low noise
Very low power

IDeF-X chip family

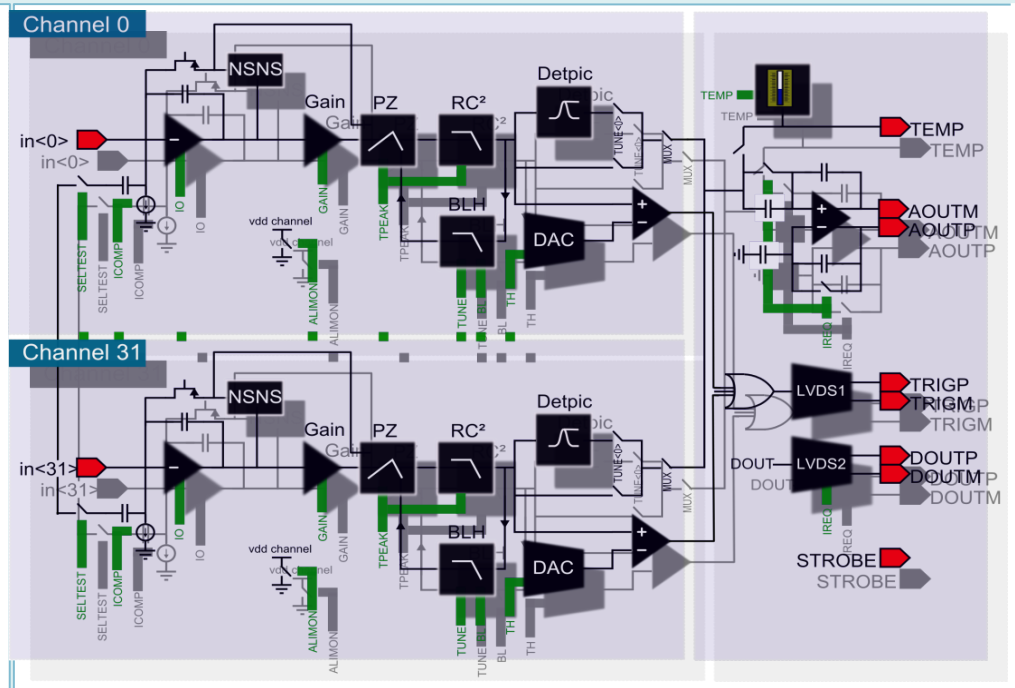
ASIC	Detector	Ch	out	Self-Trig?	Dyn (ke-)	Power mW /ch	Tpeak µs	Noise floor el rms	Radiation
V0	CdTe, Ge	1	//	X	+/-500	3	ext	33	TID
V1.1	CdTe	16	// & mux	✔	+/-**50**	2.8	1-10	33	TID
ECLAIRs	CdTe	32	Mux diff	✔	+50	3.4	1-10	33	TID,SEL,SEU$_{flag}$
HD	CdTe	32	Mux diff	✔	+240	0.9	1-13	18	TID,SEL,SEU$_{flag}$
BD	CdTe,DSSD	32	Mux diff	✔	+/-50	3.4	1-10	33	TID,SEL,SEU$_{flag}$
LXE	CdTe, DSSD, LiqAr TPC	32	//	✔	+240	2.2	1-13	33	TID,SEL,SEU$_{flag}$
Caterpylar		1	//	X	+/-50		ext	12	TID,SEU$_{flag}$
D2R1	CdTe, DSSD	256	1/row	✔	+/-60	0.3	2-20	25	SEU$_{flag}$
Caterpylar AMS		1	//	X	+/-50		ext	10	SEU$_{flag}$

TID: total ionizing dose (200 krad a.l.) tests have been done without significant degradation of performances.

SEL: Single Event Latch-up hardened ASIC

SEU$_{flag}$: a dedicated output triggers in case of Single Event Upset.

IDeF-X HD chip fo CdTe detection



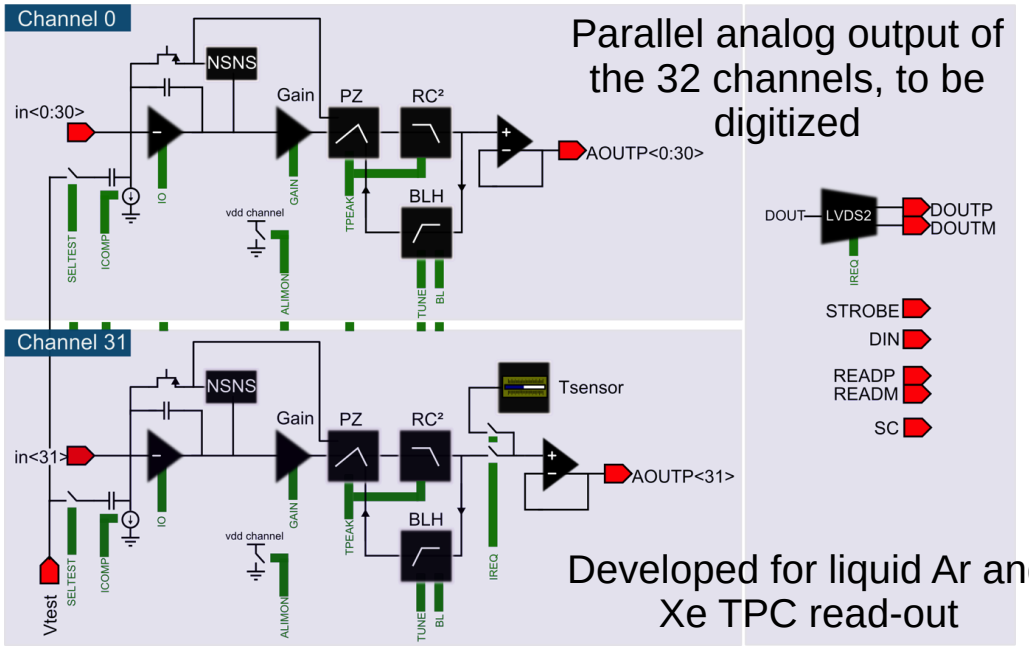
- 32 channels. Muxed output
- CSA (new concept)
- Gain (50, 100, 150, 200mV/fC)
- PZ cancellation
- RC² filter (T_{PEAK}=1 to 10µs)
- Base Line Holder (switchable)
- Peak detector

- 1 Threshold/ channel (6 bits)
- Dynamic up to +1.2MeV (CdTe).
- "OR" Trigger output.
- 3 modes of readout:
  - All channels.
  - Hit channels.
  - On demand

- Embedded temperature Sensor with absolute resolution of 0.5°C.
- Energy and T readout via differential output buffer.

- Slow Control
  - ✓Multi ASIC interface
  - ✓Gain
  - ✓T_{PEAK}
  - ✓I_{CSA}(23-100µA)
  - ✓I_{LEAK}
  - ✓Channel mask
  - ✓Test mask
  - ✓AlimON
- Power on reset
- "smart" LVDS input/output
- Hardened digital standard cell
- Low power: 0.8mW /channel

IDeF-X HD LXE version



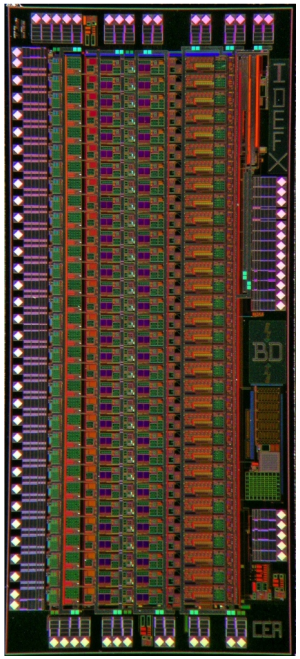
- 32 channels. ~~Muxed~~ parallel analog output
- CSA (new concept)
- Gain (50, 100, 150, 200mV/fC)
- PZ cancellation
- RC² filter (T_{PEAK}=1 to 10µs)
- Base Line Holder (switchable)
- ~~Peak detector~~

- ~~1 Threshold/ channel (6 bits)~~
- ~~Dynamic up to +1.2MeV (CdTe).~~
- ~~"OR" Trigger output.~~
- ~~3 modes of readout:~~
  - ~~All channels.~~
  - ~~Hit channels.~~
  - ~~On demand~~

- Embedded temperature Sensor with absolute resolution of 0.5°C.
- ~~Energy and T readout via differential output buffer.~~

- Slow Control
  - ✓Multi ASIC interface
  - ✓Gain
  - ✓T_{PEAK}
  - ✓I_{CSA}(23-100µA)
  - ✓I_{LEAK}
  - ✓Channel mask
  - ✓Test mask
  - ✓AlimON
- Power on reset
- "smart" LVDS input/output
- Hardened digital standard cell
- Low power: 0.8mW /channel

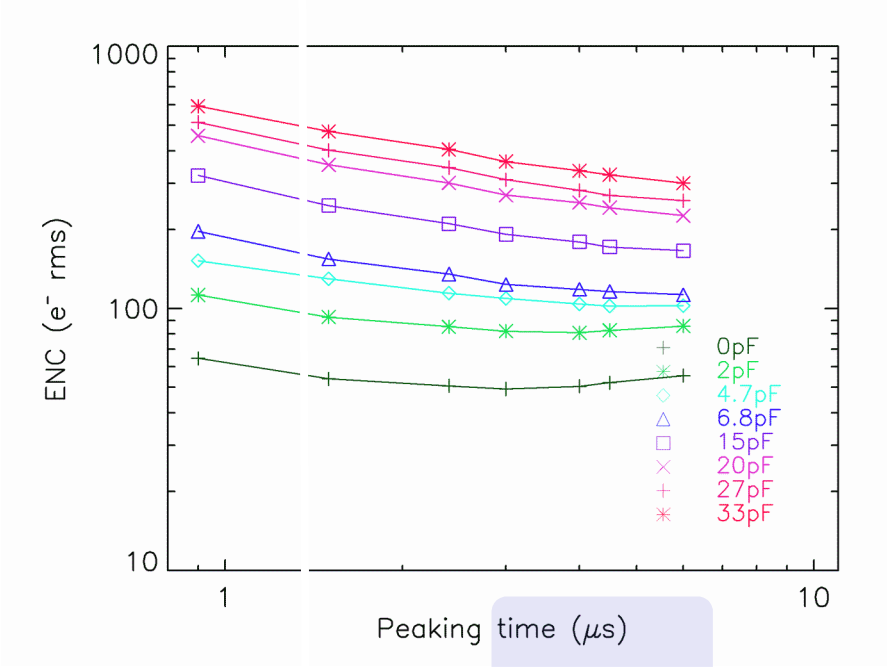
IDeF-X HD (LXE) performance



6400 µm

2800 µm

LXE version used for XEMIS project (liquid Xenon TPC, D.Thers, Subatech) for 3 gammas medical imaging.



Noise level :

- 80 e^- + 15 e^-/pF with 1 µs peaking time
- 33 e^- + 6 e^-/pF with 12 µs peaking time

Extrapolation for Cdet=50pF, ileak=20nA @ t_{peak} min

1000 e- rms=> 8460 eV FWHM (CdTe)

Low threshold (5s) = 18 keV

But Dynamic Range limited to 230 keV

Conclusions

Irfu cea saclay

Chips for MPGD detectors

- AGET well adapted to TPC read-out: auto-trigger, choice of channels to read, long peaking time with ASTRE chip
- DREAM fitted for high flux MPGD read-out: auto-trigger, simultaneous read and write, works with large detector capacitances

Very low noise IDeF-X front-end chip family

- Dedicated to solid detector read-out, also used with liquid noble gas TPC (IDeF-X HD LXE)
- Could it be used for gaseous primary ionization read-out ? With which digital read-out ?

Prospects for future chips

- ADC integration in front-end chip
- Continuous digitization with fast digital link
- Long term: adaptative front-end chip → FPGA with low noise analog part ?
- Very low noise amplifier combined with analog memory or continuous digitization