INFN TORINO ELECTRONICS SERVICE

DAQ/FEE/Trigger workshop for COMPASS beyond 2020
Prague 9-11 November 2017

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Outline

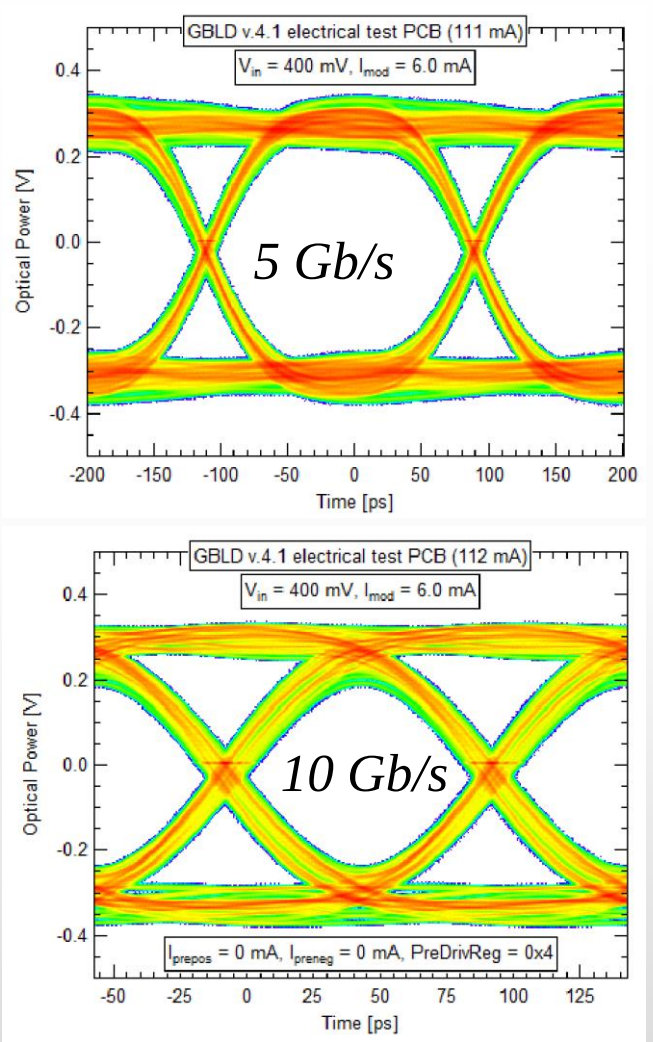
- Introduction
- IC design
  - Contributions in common projects
  - System level ASIC design
  - R&D activity
- FPGA design
- PCB design
- Wire bonding and testing facilities

Who we are

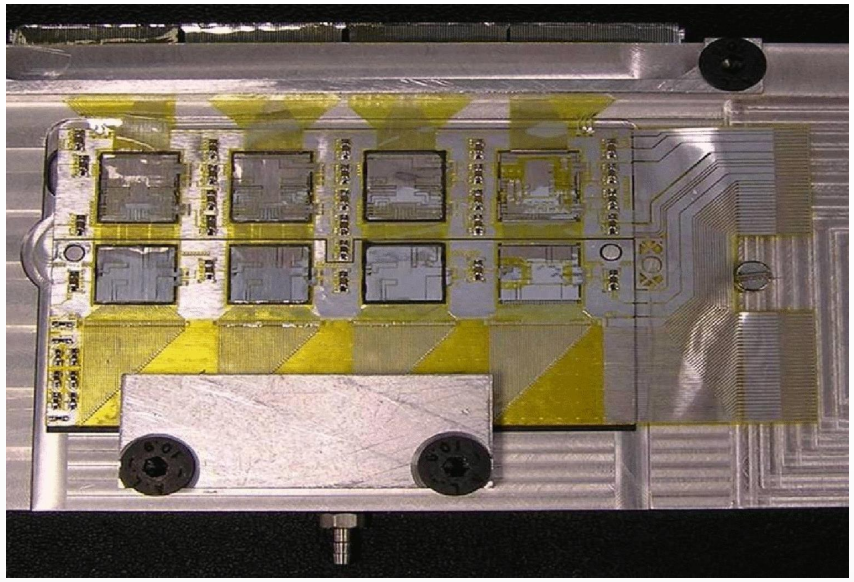
- INFN Torino personnel consists of 87 staff members and 275 associated members (students and researcher from University and other institutions)
- Electronics Laboratory at INFN Torino is made up of 14 staff members
  - 2 Postdoc and more than 10 PhD students involved in IC design. Big resource!
- The Electronics Laboratory fulfils all the requests made by different physics research groups providing both design, systems realization and test capabilities of discrete electronics and microelectronics devices
- Design activities range from the very front-end electronics to the development of full read-out and data acquisition systems

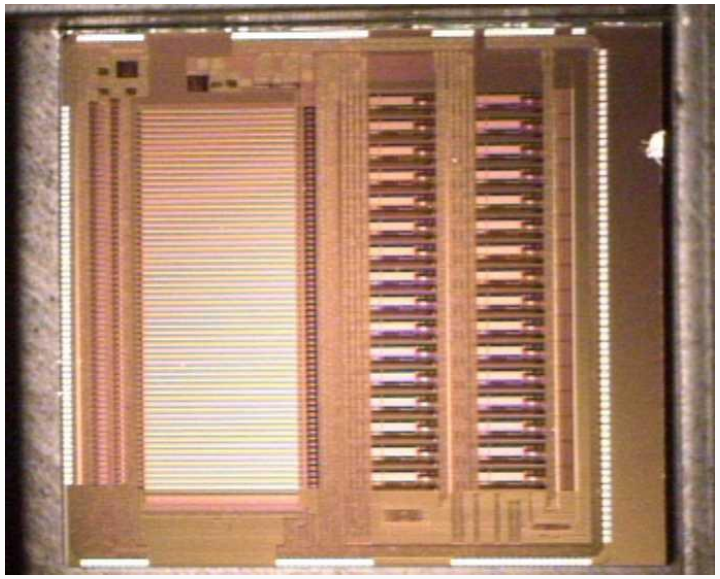
IC design - contributions

- ALICE ITS upgrade: ALPIDE Monolithic Pixel Sensor chip (TowerJazz 180 nm)
  - 1.2 Gb/s Data Transmission Unit (DTU) DDR mode with SEU protection. PLL design x15 clock multiplication (40 -> 600 MHz)
- GBLD: Laser Driver for the CERN's GBT project. 4.8 Gb/s, radiation tolerant in CMOS 130 nm (IBM). R_j<1 ps rms
- HL-LHC CMS ECAL upgrade:
  - 12-bit ADC 160 Ms/s, developed by private company
  - chip integration (2 ADC per ASIC), data compression and readout logic development (E-DTU) in CMOS TSMC 65 nm



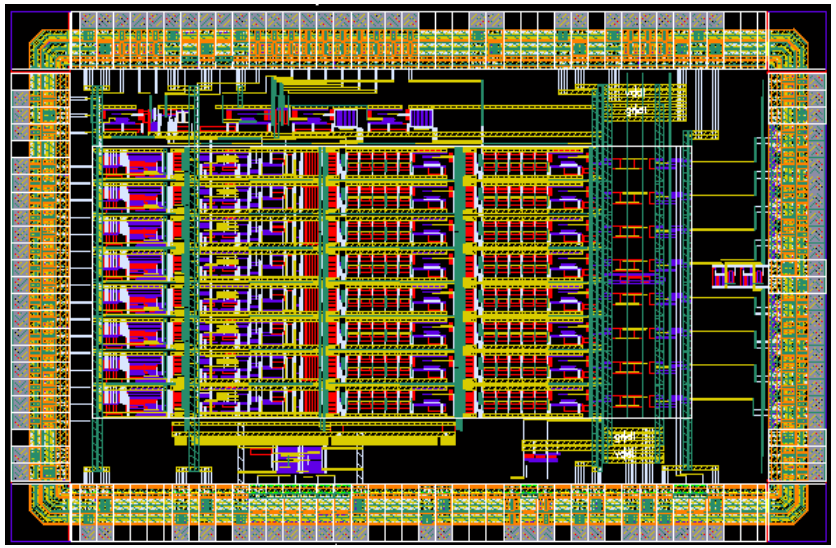
IC design – system level ALICE

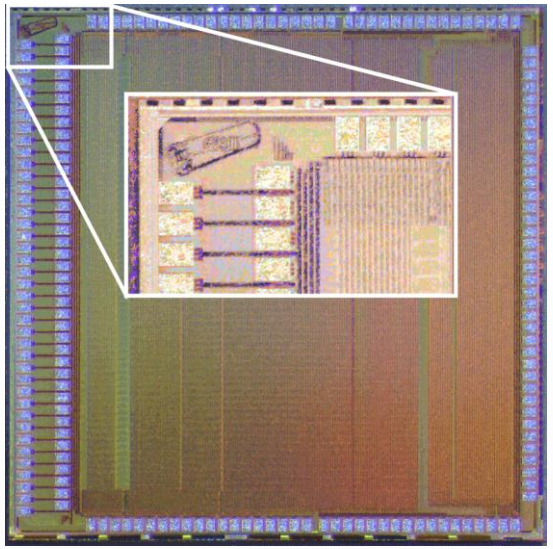




- ALICE ITS Silicon Drift Detector: development, test production and assembly of the readout electronics for the SDD detector
  - PASCAL: 64 channels analogue frontend. Preamp. and analogue storage. 10-bit SAR ADC 40 Ms/s
  - AMBRA: digital 4-events buffer, data compression from 10 to 8 bits
  - CMOS 0.25 μm

IC design - system level

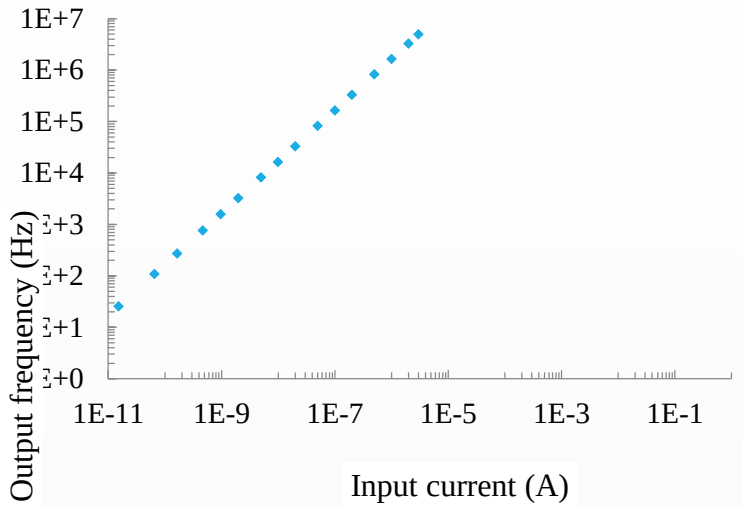


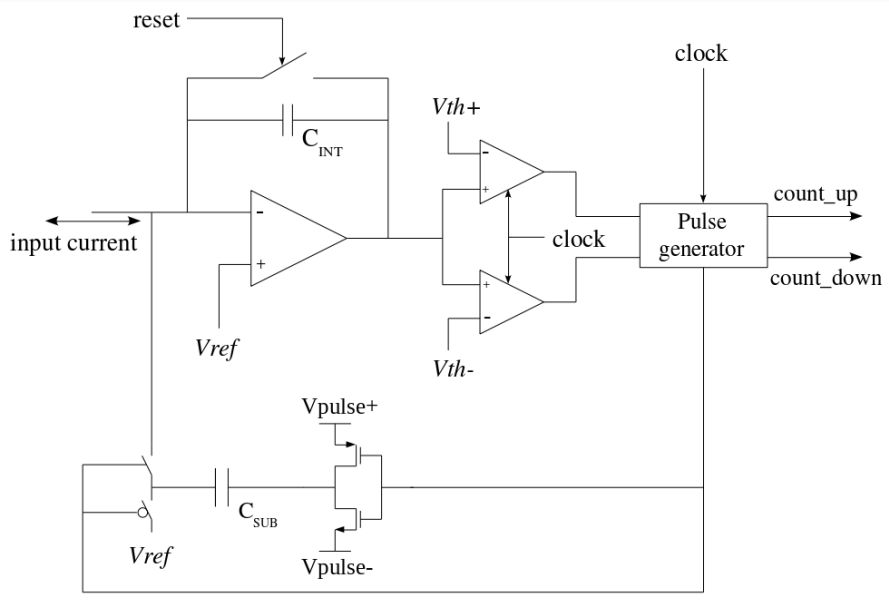


- COMPASS CMAD: readout of photomultiplier of RICH detector
  - 8 channels with variable gain
  - 10-bit DAC
  - LVDS serial interface
  - CMOS 0.35 µm
- BESIII CGEM readout chip: TIGER
  - CMOS UMC 110 nm
  - 64 channels, VFE + TDC/ADC
  - Charge and time measurement

IC design - system level – TERA/CNAO

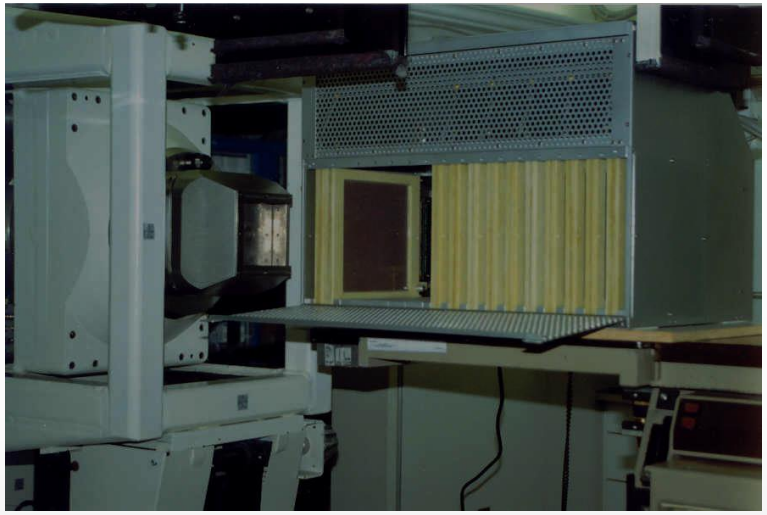
Technology	input polarity	Csub	Clock frequency	Max conv. freq.	Counter # bits	Control logic
CMOS 1.2 µm	unipolar	200 fF	N/A	5 MHz	20	async
CMOS 0.8 µm	unipolar	200 fF	N/A	5 MHz	20	async
CMOS 0.8 µm	unipolar	200 fF	20 MHz	5 MHz	16	synch
CMOS 0.35 µm	bipolar	50÷350 fF	100 MHz	20 MHz	32	synch
CMOS 0.35 µm	bipolar	200 fF	280 MHz	70 MHz	32	synch

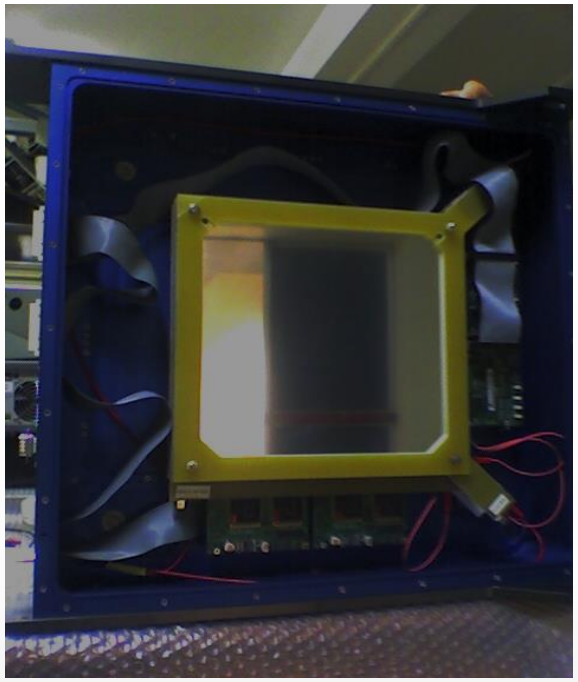




- TERA: design of a ASIC family, high linearity 64 channels for charge measurements in dosimetry and hadron therapy
- Based on a current to frequency converter followed by a counter
- Very good linearity of the pulse frequency as a function of the input current
- Used for the CNAO beam monitor system (Centro Nazionale di Adroterapia Oncologica) and private companies

IC design - system level – TERA/CNAO



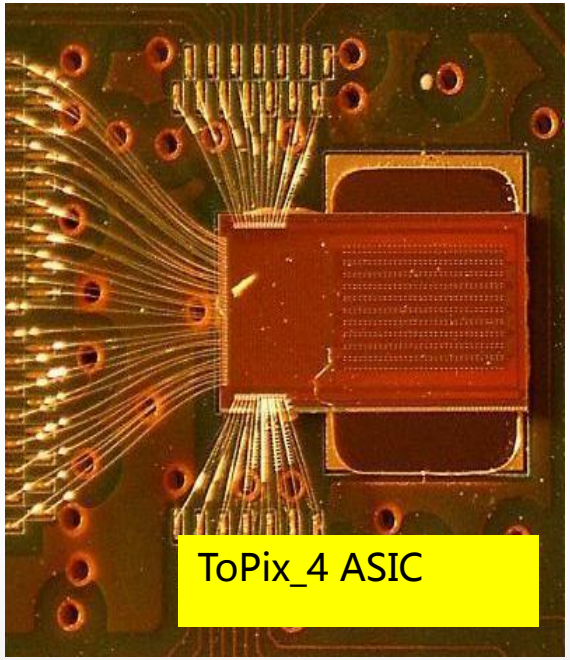


- Application 1: Magic Cube
  - 3D dosimeter
  - 12 planes strip gas detector
  - 64 channels/plane
  - 250 x 250 x 400 mm^3 active volume
- Application 2: CNAO
  - 2D beam monitor at CNAO
  - 32 x 32pixel matrix
  - 160 x 160 mm^2 active area
- Application 3: IBA dosimeters
  - MatriXX and StarTrack dosimeters

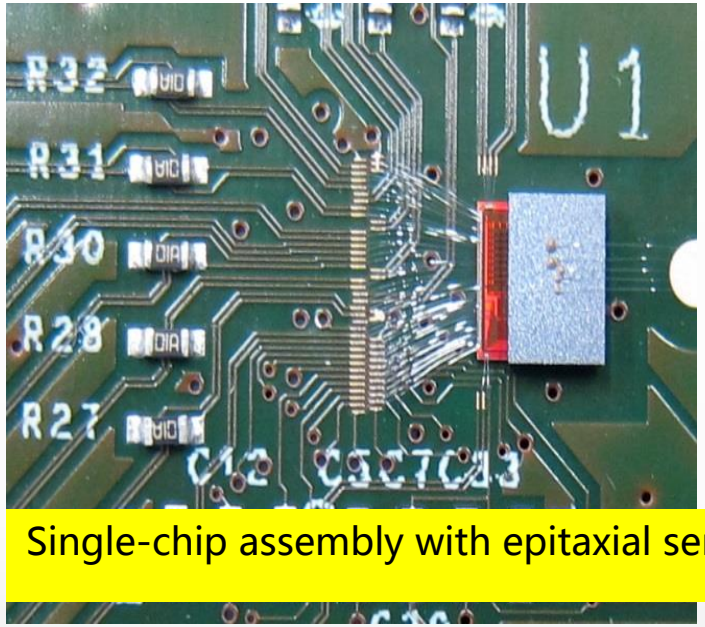
IC design – R&D

- Timing application:
  - TOFEE: amplifier-discriminator chip for timing measurement of Ultra Fast Silicon Detector (resolution required ~30 ps per detector layer in CMS-TOTEM PPS). 8 channels, CMOS 110 nm (UMC), ToT time walk correction
  - TOF-PET: analogue CMOS front-end for silicon photomultiplier (SiPM) for time-of-flight measurement in compact Positron Emission Tomography medical imaging. CMOS 130 nm, 64 channels, 100 kHz per channel, 50ps TDC time binning, ToT time walk correction
  - NA62: development of a prototype for the readout of Gigatracker detector of the NA62 experiment. CMOS 130 nm, 4 TDC per channel (Wilkinson ADC), CFD time walk correction, 100 ps time binning
- SEED: Sensor with Embedded Electronics Development. Study of a innovative technology HVCMOS 130 nm for monolithic sensors
- Starting development 16 nm FIN-FET (technology evaluation studies on F/E design and radiation tolerance)
- Technology transfer: frontend and readout ASIC, with time measurement per channel less than 100 ps rms of a 1024 channels hybrid pixels sensor (CMOS 110 nm)

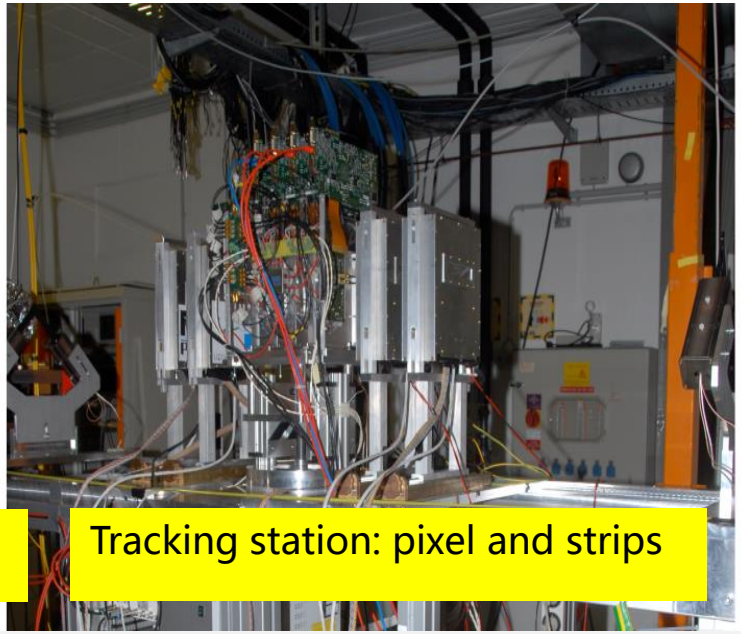
IC design – R&D - PANDA



ToPix_4 ASIC



Single-chip assembly with epitaxial sensor

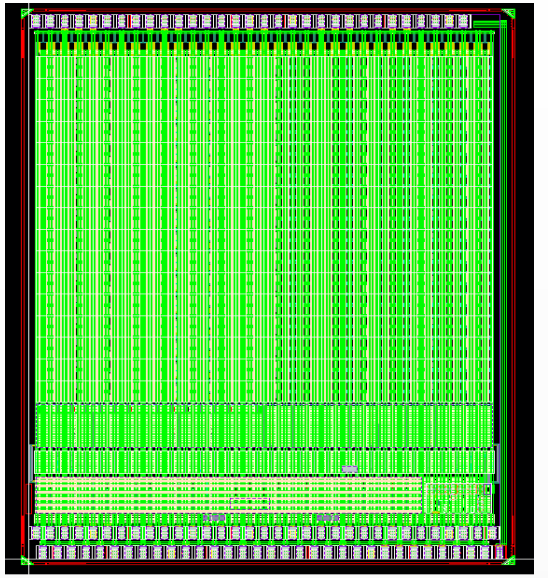


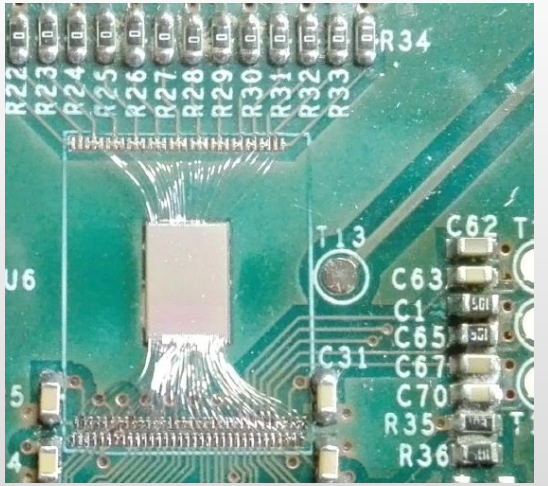
Tracking station: pixel and strips

- Responsibility of the Micro Vertex Detector (MVD): ~11 millions of pixels and 200k micro strips
- High speed trigger less readout for both the systems ToPix (pixels) and PASTA (strips)
- ToPix: first CMOS 130nm (IBM) prototype tested at INFN with intensive studies of radiation damages
- Development with FBK of epitaxial silicon sensors

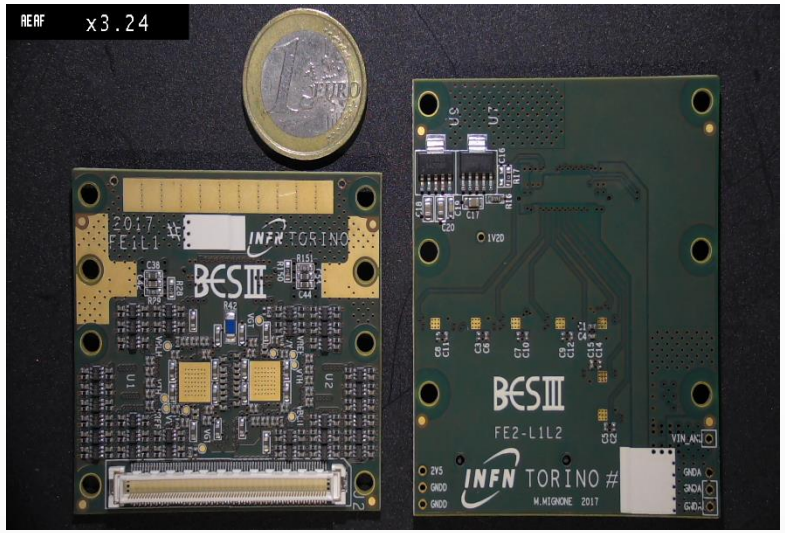
IC design – R&D CHIPIX65

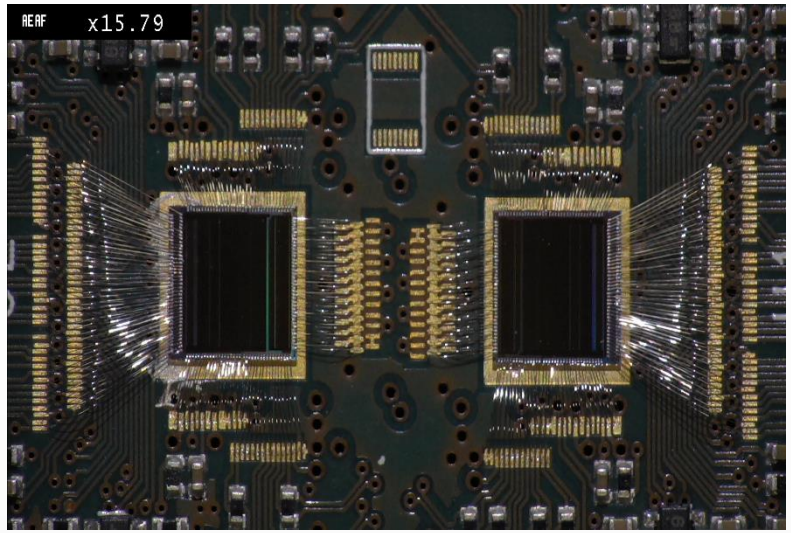
- CHIPIX65: Italian project, involving more than seven INFN institutes, for development of an innovative pixel sensors readout chip in CMOS 65 nm, coping with high rates and high radiation environments (HEP experiments)
- Close collaboration with CERN's RD53 (ATLAS-CMS R&D activity for development pixels readout chip for HL-LHC)
- CHIPIX65: 64x64 pixel matrix
  - Pixel size 50 µm x 50 µm
  - Two analogue frontend architectures (synchronous Torino / asynchronous Pavia-Bergamo)
  - 4x4 macro region readout architecture
  - 40 MHz clock
  - Hit rate up to 3 GHz/cm^2
  - Trigger matcher on pixel region (12.8 µs trigger latency)
  - Signal digitization: 5-bit fast ToT counting with latch turned into a local oscillator (100-900 MHz)
  - Chip fully functional also after 230 Mrad irradiation test

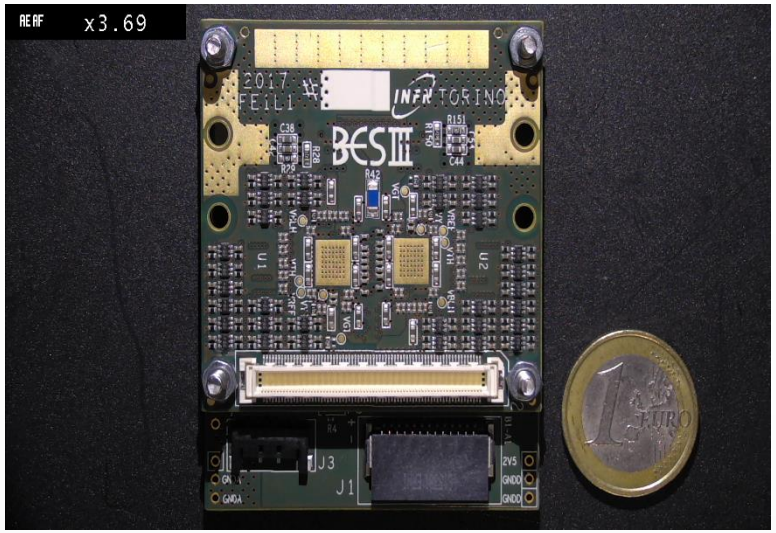




PCB design – BES III

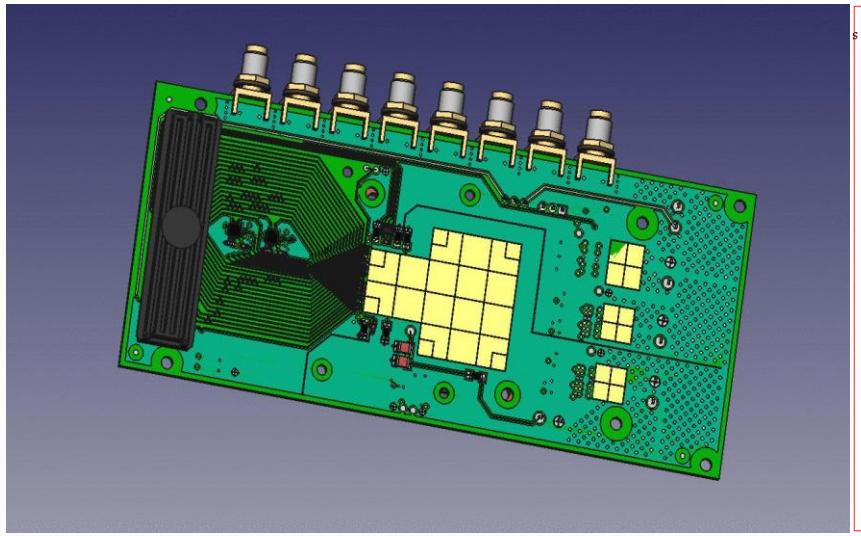


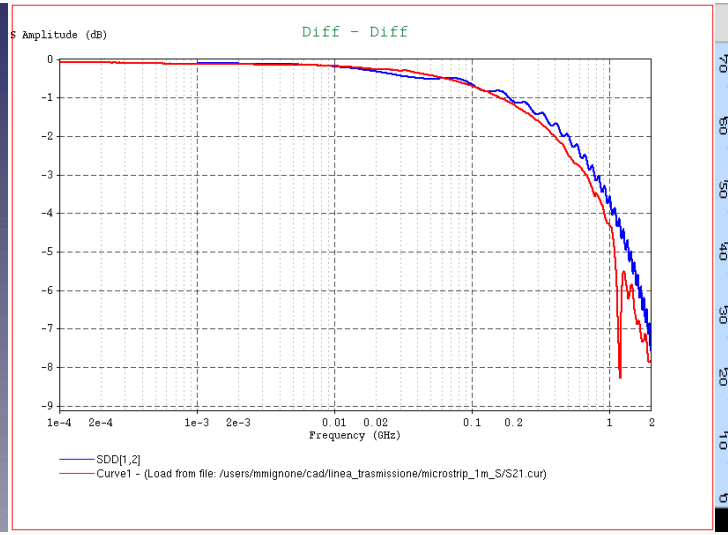


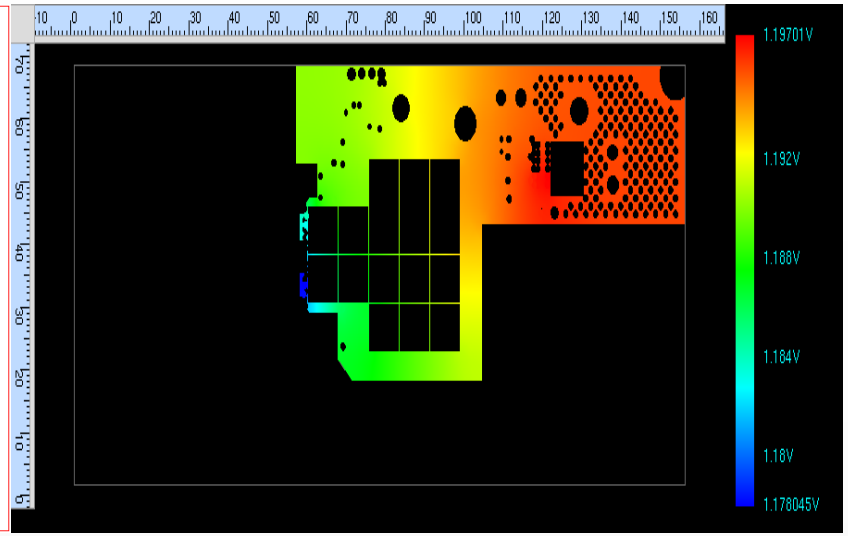


- Torino involved in the construction of the Cylindrical GEM detector for the inner tracker of the BES III experiment
- VFE CGEM readout developed in Torino (TIGER ASIC)
- On detector readout electronics: 10000 channels, 160 ASIC, 80 FE boards

PCB design – test boards





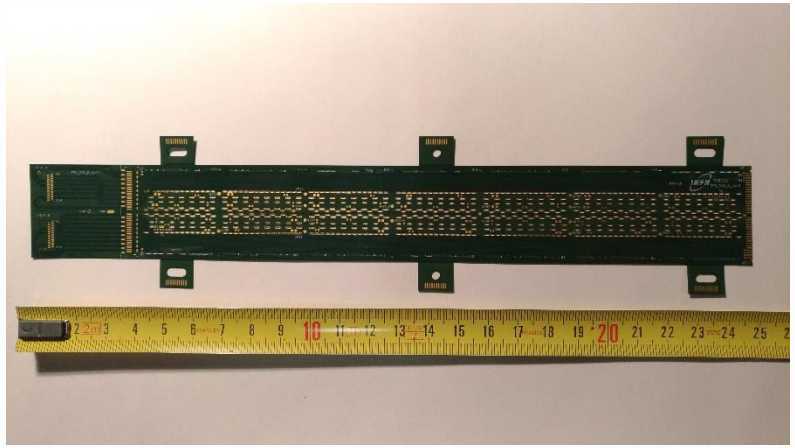


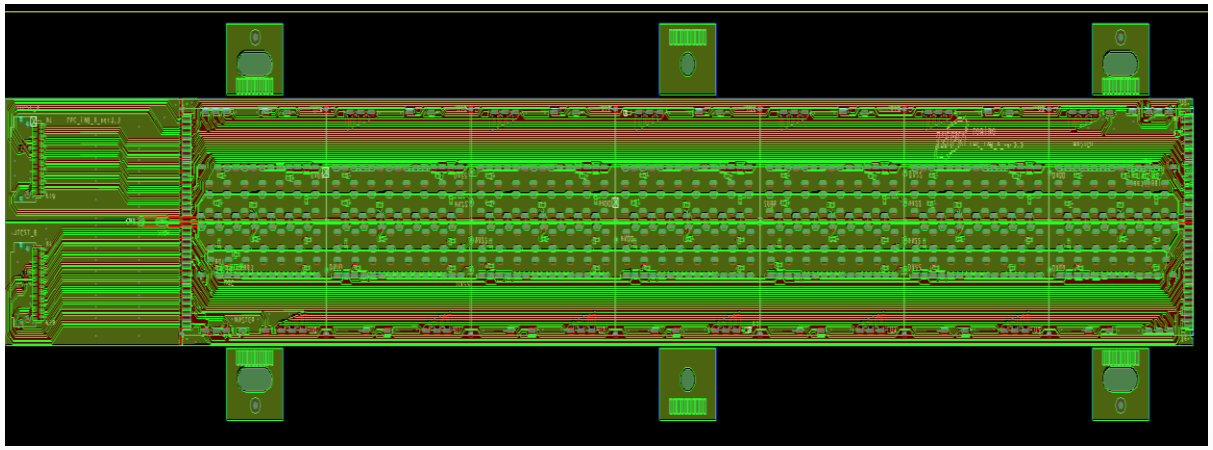
S parameters measurements vs simulation

Voltage drop simulation

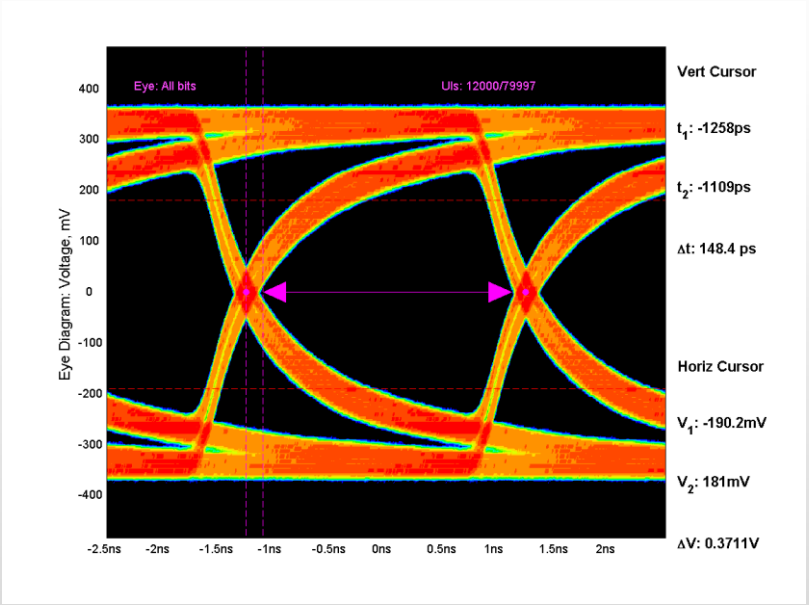
- Each ASIC designed in Torino requires a dedicated PCB test board
- Each board is designed by our PCB expert staff
- Signal and power integrity simulations are performed when required

ALICE ITS upgrade

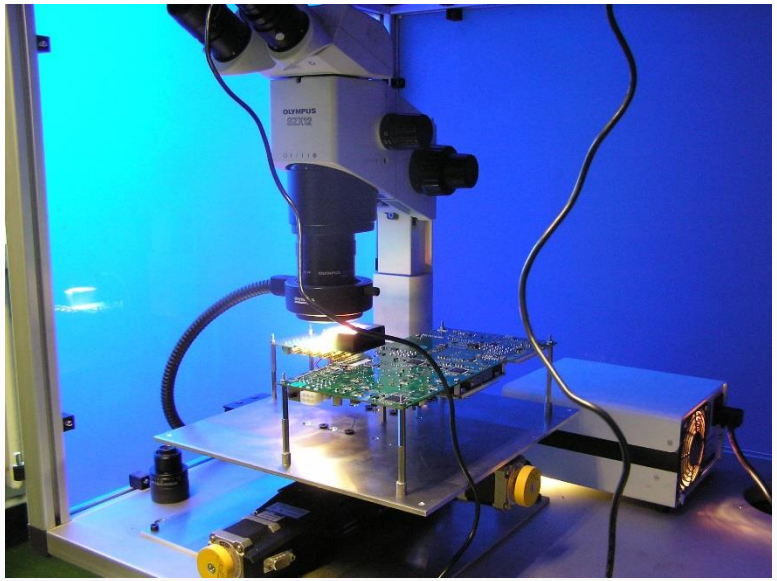


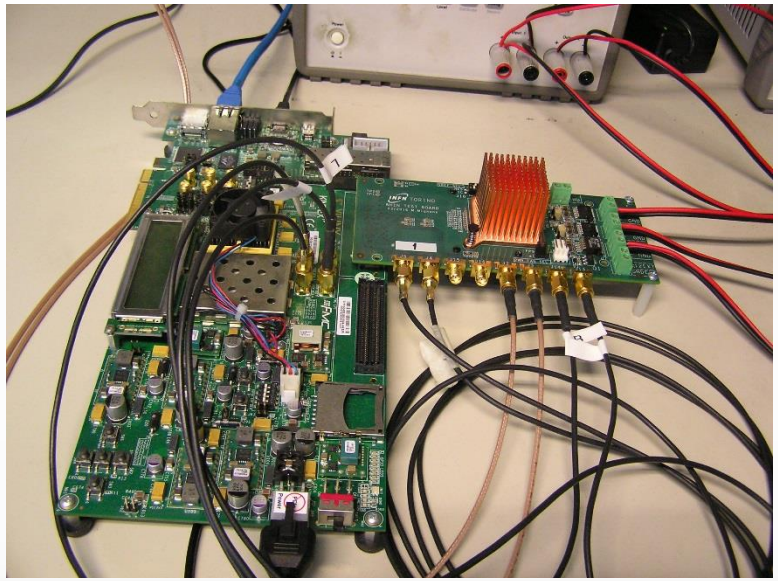


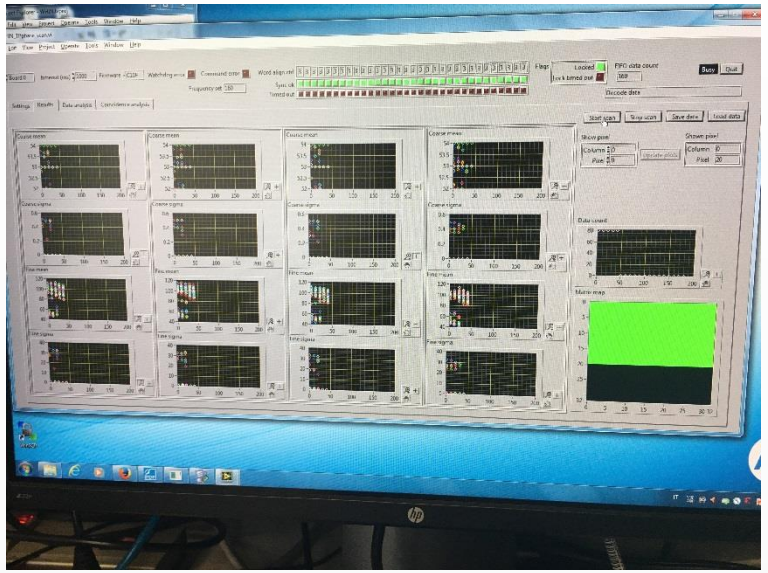
- Responsibility in Torino (hardware):
  - Design of the detector data transmission system (flex cable with data rate up to 400 Mb/s per channel)
  - Production of 2500 flex circuits
  - Design of assembly tools for all the sites
  - Construction of 30 *STAVE* modules



FPGA design – testing

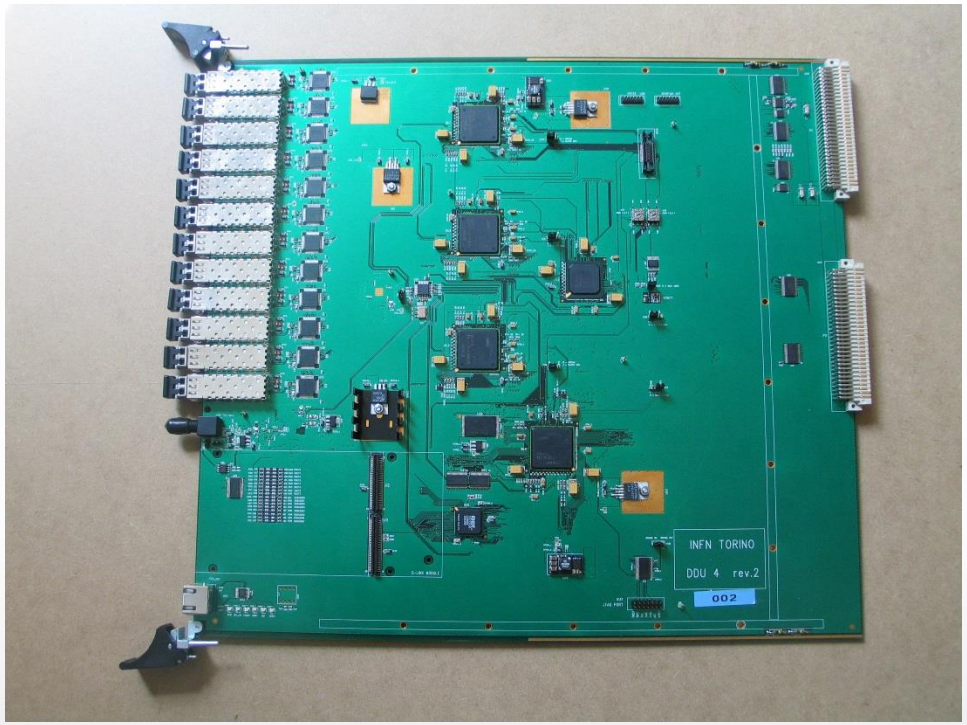


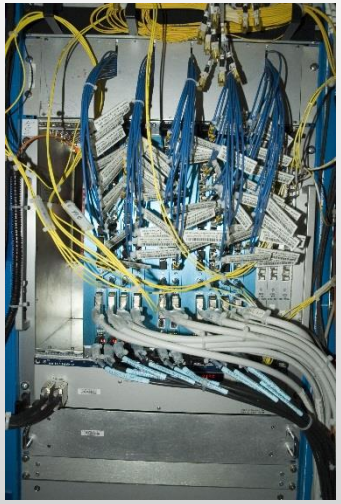




- Test and characterization performed for each developed ASIC
- FPGA Xilinx Kyntex 7 development kit
- ASIC - FPGA through high speed serial I/O
- FPGA- PC through Ethernet links
- LabVIEW software for analysis

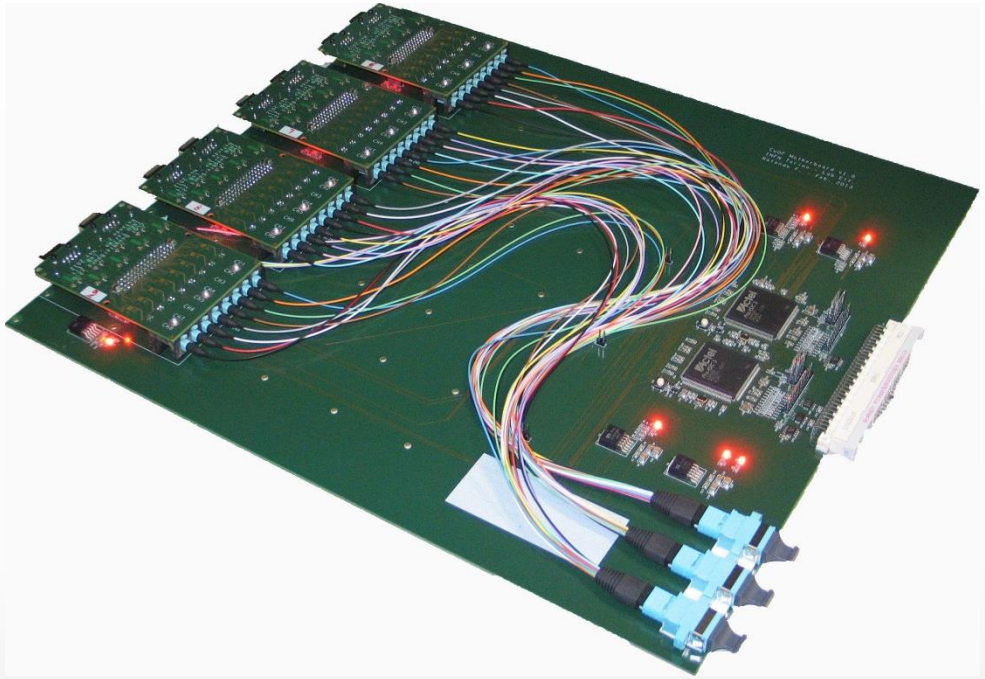
FPGA design – CMS /ALICE

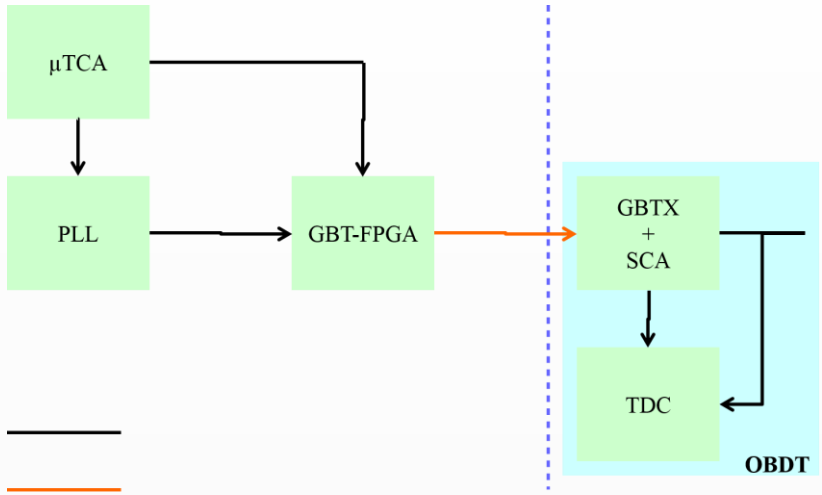




- CMS DT Front End Driver (DDU): HW and firmware design (Xilinx Virtex II pro)
- ALICE SSD readout superCARLOS rx: HW design (Xilinx Virtex 5)

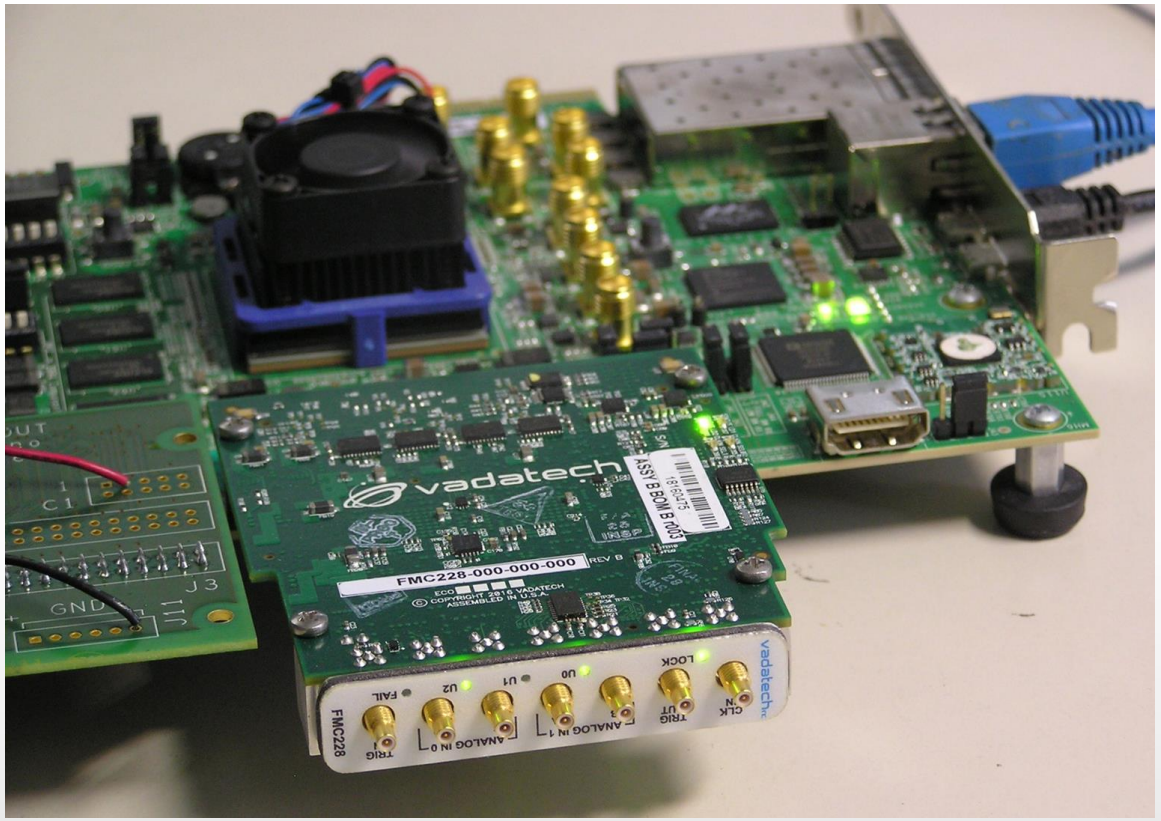
FPGA design – CMS DT upgrade





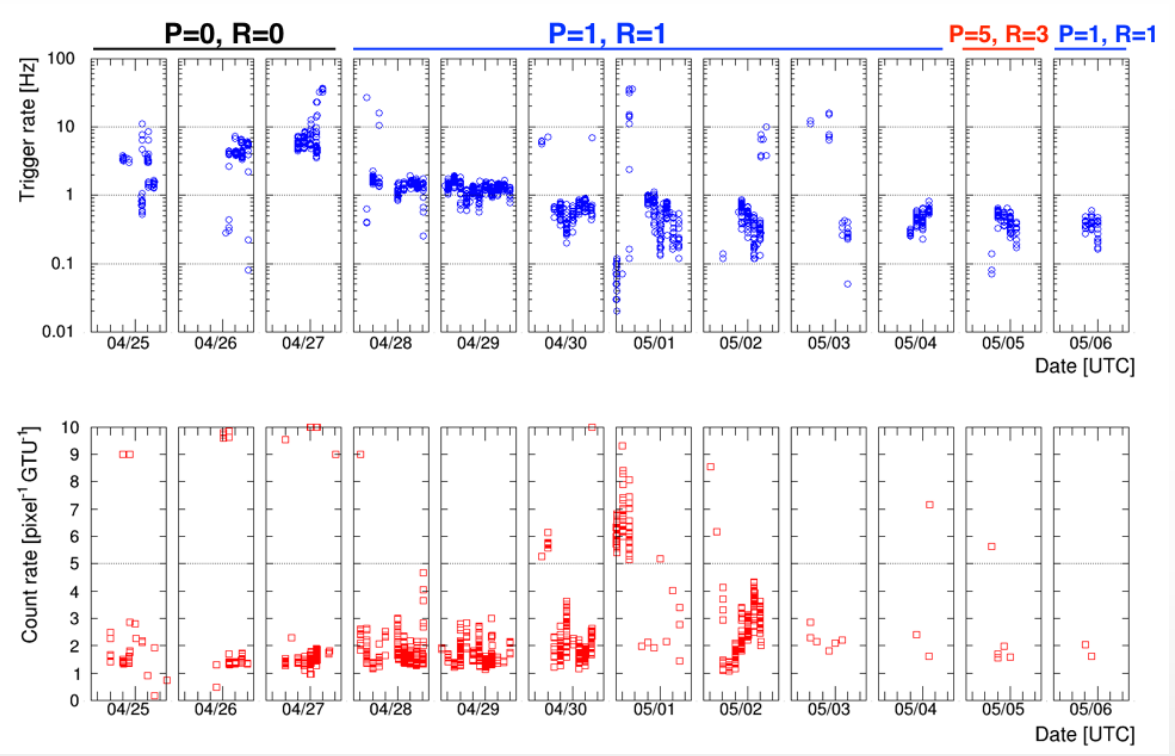
- CMS DT readout upgrade: HW design and installation of the CUOF system (Copper to Optical Fibre board). 3500 optical links at 480 Mb/s, to manage data transfer (readout +trigger) between detector area (UXC) and counting room (USC)
- Custom implementation on a Xilinx Virtex 7 FPGA of the CERN's GBT protocol at 5 Gb/s with trigger data and slow control for the next upgrade of the DT chambers readout

FPGA design – ALICE ZDC upgrade



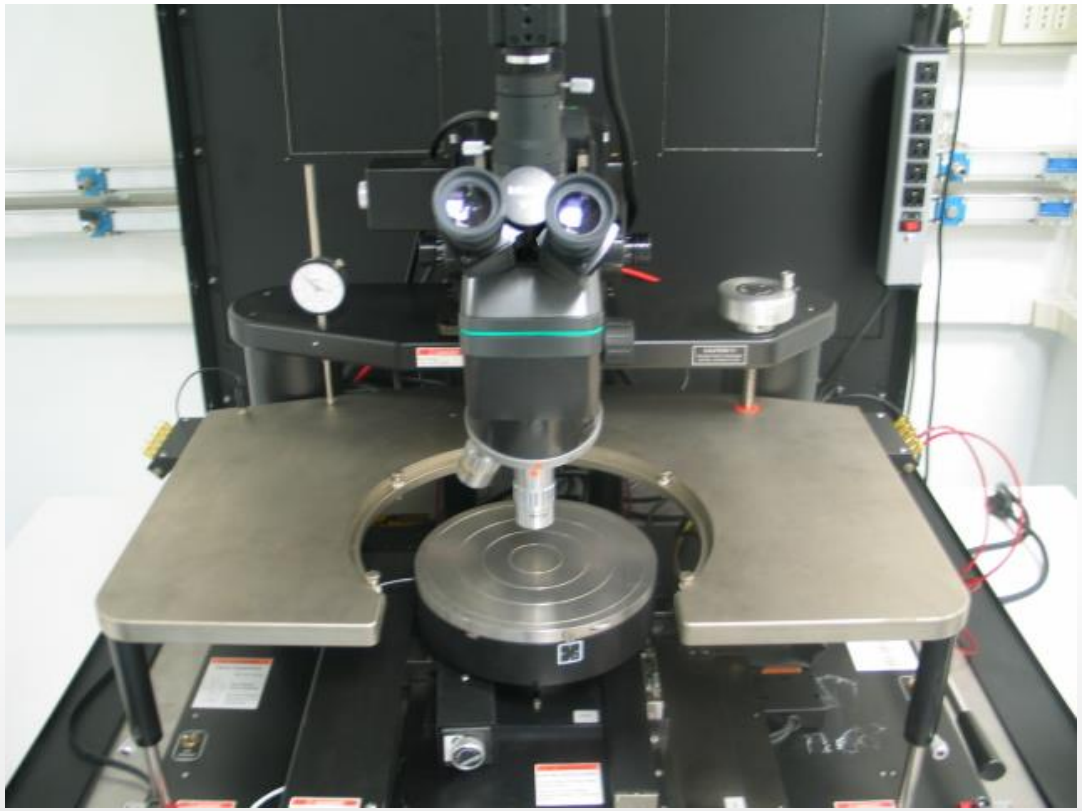
- Firmware implementation on a Xilinx Kintex evaluation kit of the JESD protocol to acquire data from VADATECH digitizers, with an overall throughput of 80 Gb/s

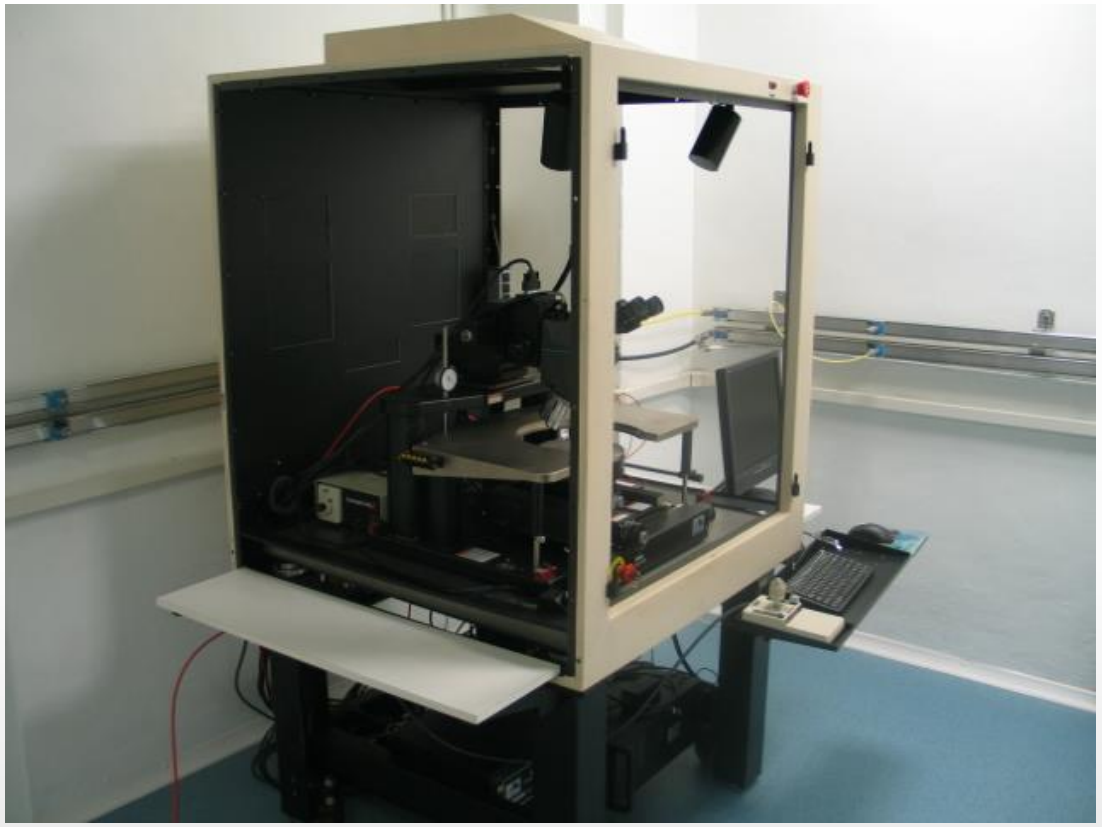
FPGA design – JEM-EUSO trigger



- Cosmic rays observation from the NASA Super Pressure Balloon (JEM-EUSO) and from ISS (MINI-EUSO, not yet launched)
- L1 trigger algorithm implemented in a Xilinx ZYNQ FPGA
- L1 and L2 trigger algorithm for MINI-EUSO

Testing

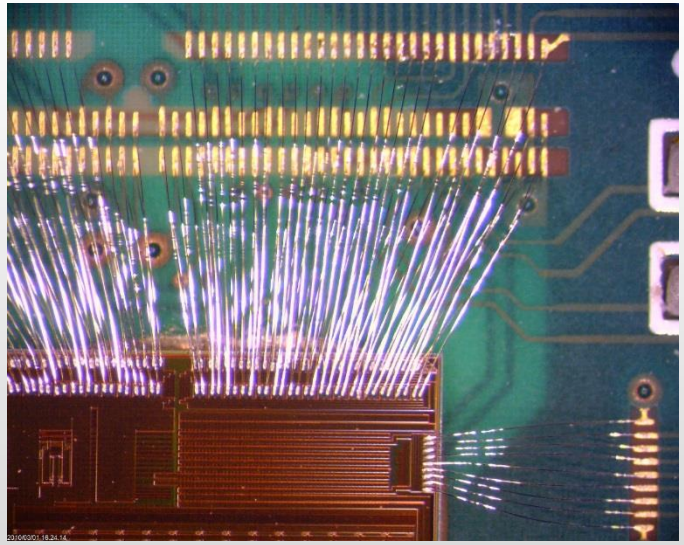


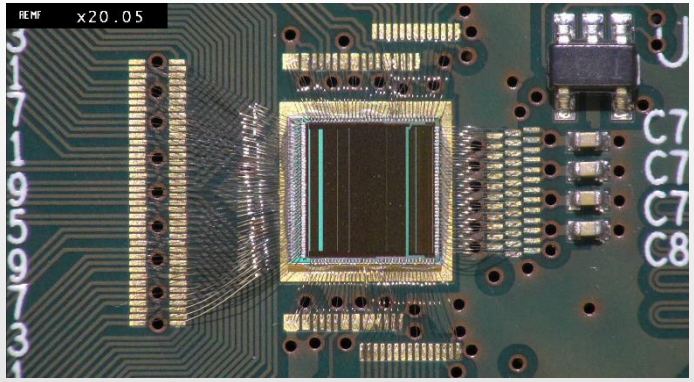


- 8” probe station (CASCADE – MICROTECH REL 6100)
- ISO 7 clean room (~ $15\ m^2$)

Wire Bonding facility

- Up to 100 µm pitch
- AL wire up to 17 µm





Conclusion – recent activity

- BELLE II
- BES III
- CMS DT
- CMS ECAL
- CMS TK
- COMPASS
- NA62
- AUGER
- JEM-EUSO
- ALICE ZDC
- ALICE ITS
- NUMEN
- CHIPIX65
- e-LIBANS
- INSIDE
- SEED
- UFSD
- WHIN
- PANDA
- DARKSIDE
- DIESIS
- MOVE-IT
- LHAASO
- TOTEM
- SCALTECH28
- SYNCFEL
- TIMESPOT
- EEE
- FOOT
- DIACELL
- ASIDI
- FINFET16
- TRIMAGE