



picoTDC: Pico-second TDC for HEP

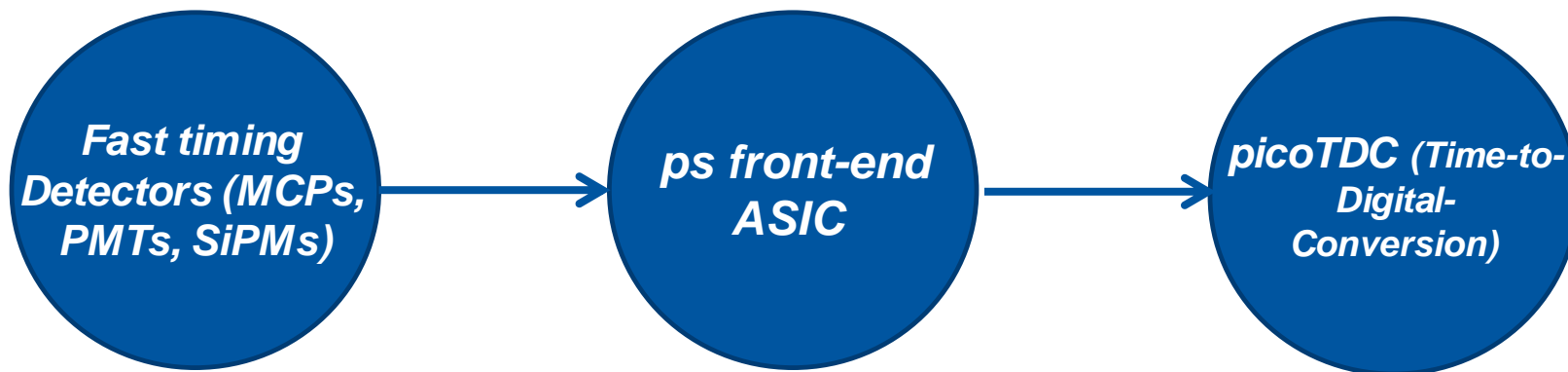
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CERN/EP-ESE-ME

Overview of Timing IC Developments

- SCA-based ICs (SAMPIC, TARGET, ...)
- TDCPix
- Timepix3 → Timepix4
- HPTDC → picoTDC
- SuperNINO
- FastIC
- Many others (Timing layers for the experiments, ...)

FastIC



| | FastIC |
|---|--|
| Availability | 2019 (First prototype submission: Q2 2018) |
| Technology | 65nm CMOS |
| Number of channels | 32/64 |
| Minimum threshold | <10fC |
| SPTR (Single Photon Time Resolution) (Sensor+Front-end) | ~50ps (FWHM) (MCPs, small SiPMs) |
| Intrinsic CTR electronics | <12ps FWHM |
| Energy measurement | Linear |
| Testing and calibration structures | Yes |

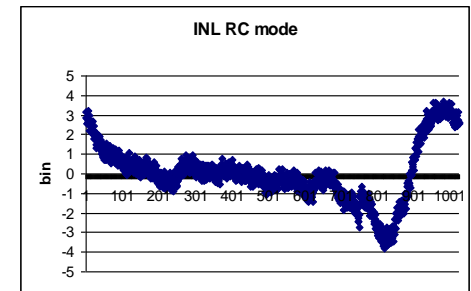
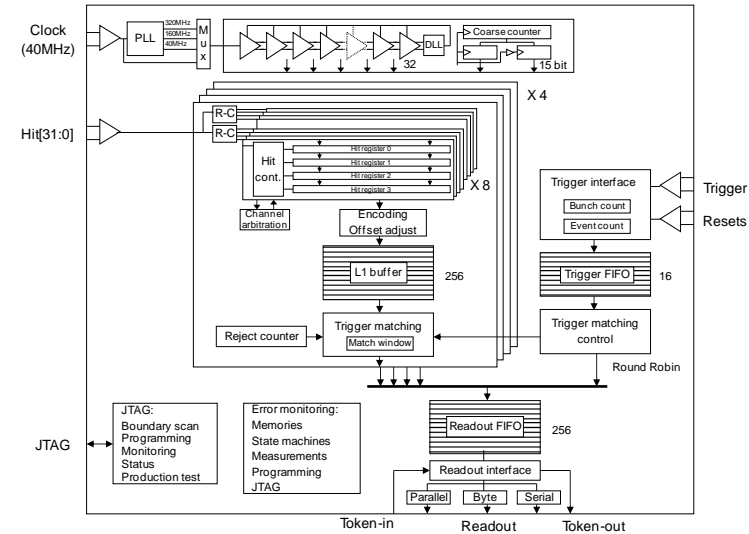
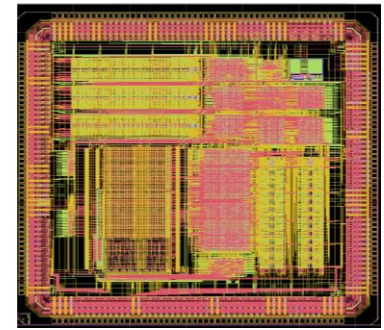
- Circuit to be configured with different detectors (PMTs, MCPs, SiPMs) in multiple configurations
- Collaboration CERN University of Barcelona
- KT funded CERN project
- Study to evaluate optimal input impedance and bandwidth as a function of input capacitance and parasitic inductance for different detectors (completed)

Timepix3 → Timepix4

| | | | Timepix3 (2013) | Timepix4 (2018/19) |
|---------------------------------|-------------|----------------|---|---|
| Technology | | | IBM 130nm – 8 metal | TSMC 65nm – 10 metal |
| Pixel Size | | | 55 x 55 μm | 55 x 55 μm |
| Pixel arrangement | | | 3-side buttable 256 x 256 | 4-side buttable 512 x 448 3.5x |
| Sensitive area | | | 1.98 cm^2 | 6.94 cm^2 |
| Readout Modes | Data driven | Mode | TOT and TOA | |
| | | Event Packet | 48-bit | 64-bit 33% |
| | | Max rate | < 43 Mhits/ cm^2/s | 178.8 Mhits/ cm^2/s 4x |
| | Frame based | Mode | PC (10-bit) and iTOT (14-bit) | CRW: PC (8 or 16-bit) |
| | | Frame | Zero-suppressed (with pixel addr) | Full Frame (without pixel addr) |
| | | Max count rate | 82 Ghits/ cm^2/s | ~800 Ghits/ cm^2/s 10x |
| TOT energy resolution | | | < 2KeV | < 1Kev 2x |
| Time resolution | | | 1.56ns [409 μs] | ~200ps [1.638 ms] 8x |
| Readout bandwidth | | | $\leq 5.12\text{Gb}$ (8x SLVS@640 Gbps) | $\leq 81.92\text{Gbps}$ (16x @5.12 Gbps) |
| Target global minimum threshold | | | <500 e^- | <500 e^- |

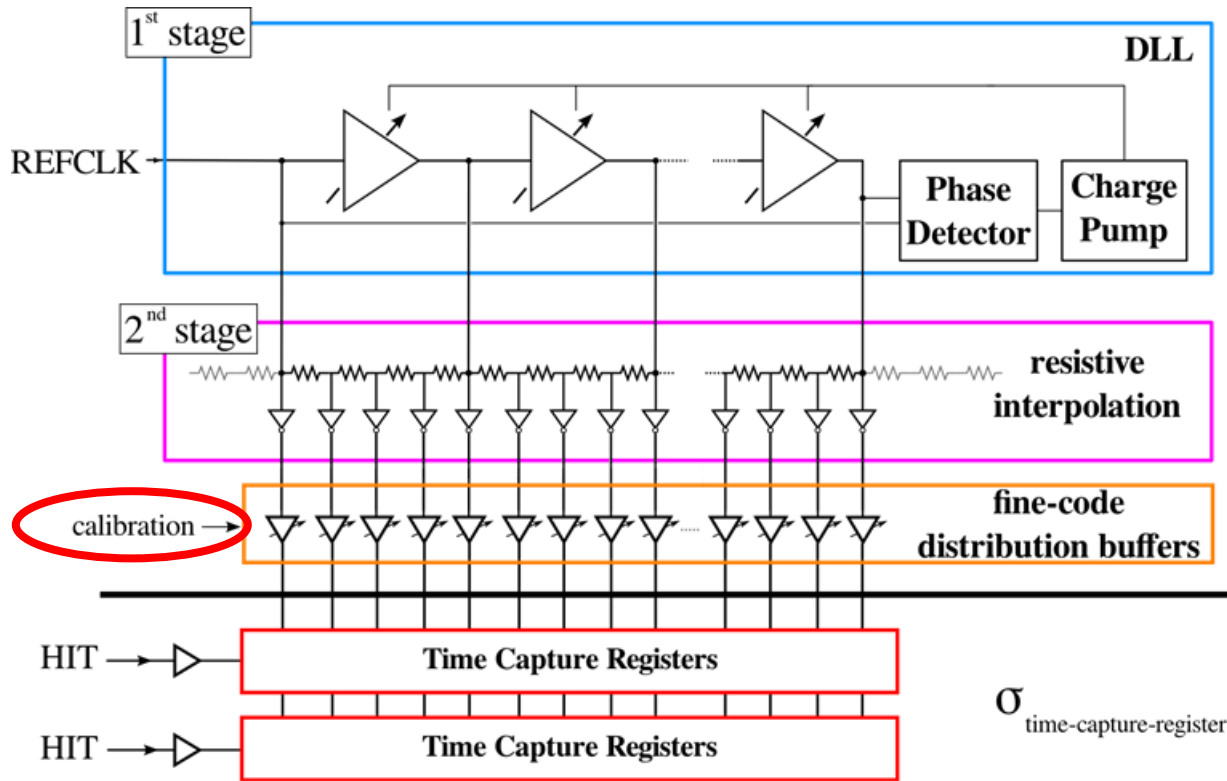
HPTDC

- History
 - Architecture initially developed at CERN for ATLAS MDT (design transferred to KEK)
 - CMS Muon and ALICE TOF needed similar TDC with additional features / increased resolution
- Features
 - 32 channels(100ps binning),
8 channels (25ps binning)
 - 40MHz time reference (LHC clock)
 - Leading, trailing edge and TOT
 - Triggered or non triggered
 - **Highly flexible data driven architecture with extensive data buffering and different readout interfaces**
- Used in large number of applications:
 - More than 20 HEP applications: ALICE TOF, CMS muon, STAR, BES, KABES, HADES, NICA, NA62, AMS, Belle, BES, , ,
 - We still supply chips from current stock.
 - Other research domains: Medical imaging,
 - Commercial modules from 3 companies: CAEN, Cronologic, Bluesky
 - ~50k chips produced
- 250nm technology (~10 years ago for LHC)
 - Development: ~5 man-years + 500kCHF.
 - Can not be produced any more
- http://tdc.web.cern.ch/TDC/hptdc/docs/hptdc_manual_ver2.2.pdf

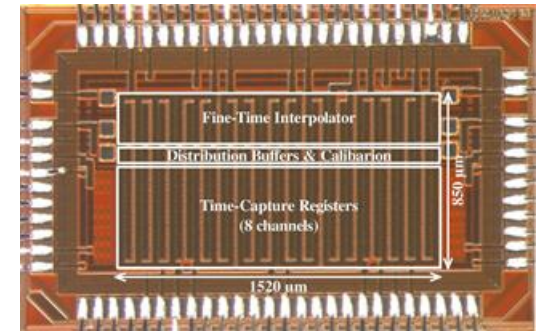


17ps RMS

TDC Architecture Prototyped in 130nm

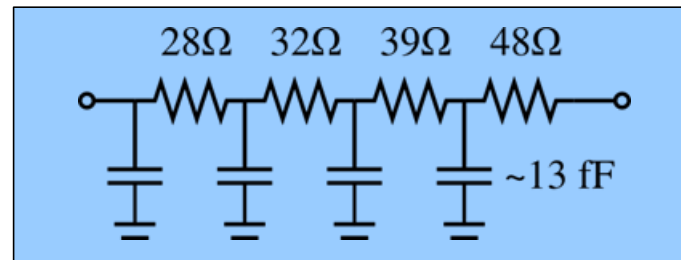
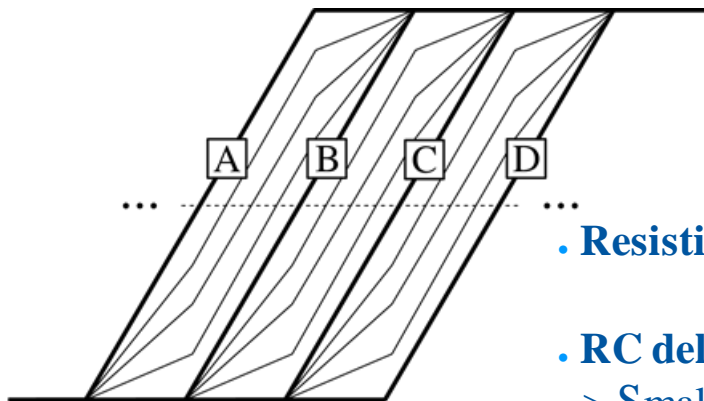
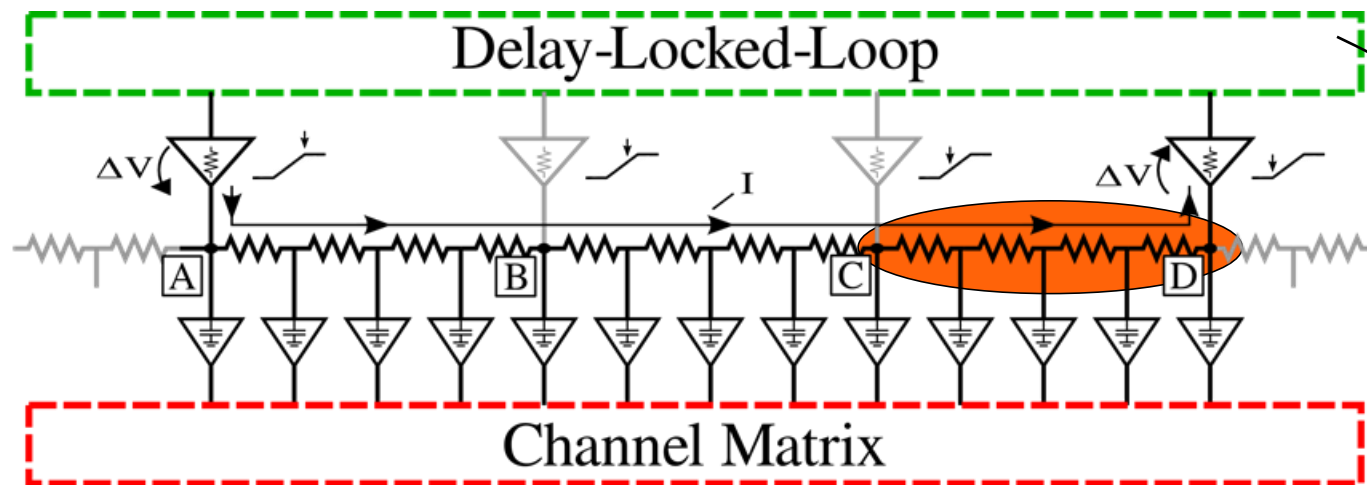


Counter



- External time reference (clock).
- 3 stage time measurement:
 - Counter: 800ps, Delay locked loop: 25ps, Resistive interpolation: 6.25ps
- Self calibrating using Delay Locked Loop (DLL)
- Design: Lukas Perktold

Resistive Interpolation (130nm)



- **Resistive voltage divider**

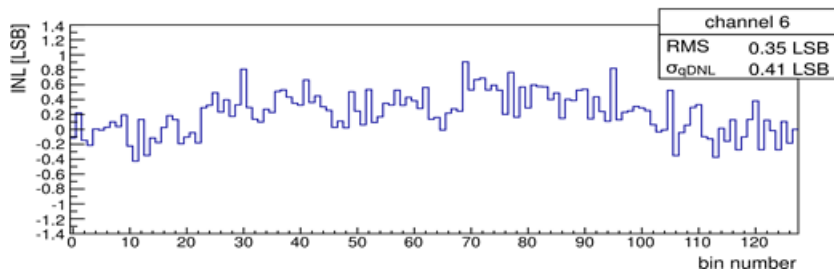
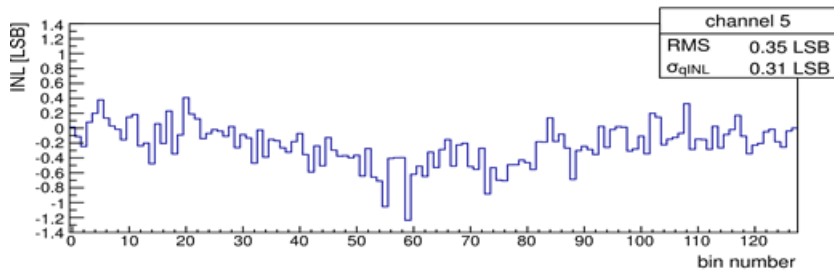
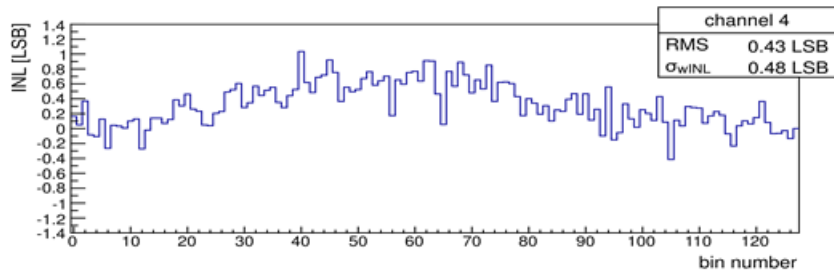
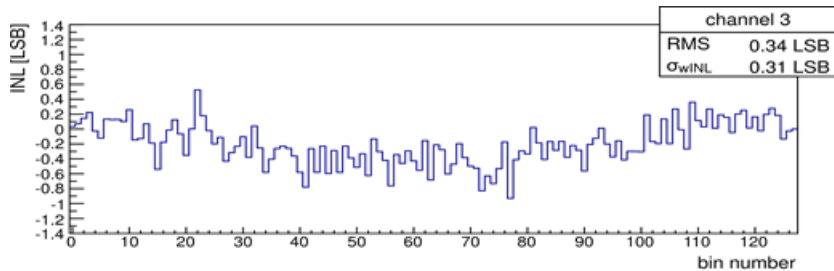
- > Signal slopes longer than delay, stabilized by DLL

- **RC delay (capacitive loading)**

- > Small resistances, small loads

- > Simulation based optimization of resistor values

Measured Performance



Code Density Test

$$INL = \pm 1.3 \text{ LSB}$$

$$RMS = < 0.43 \text{ LSB (2.2 ps)}$$

Expected RMS resolution from circuit simulations:
including quantization noise, INL & DNL

$$2.3 \text{ ps-RMS} < \sigma_{qDNL/wINL} < 2.9 \text{ ps-RMS}$$

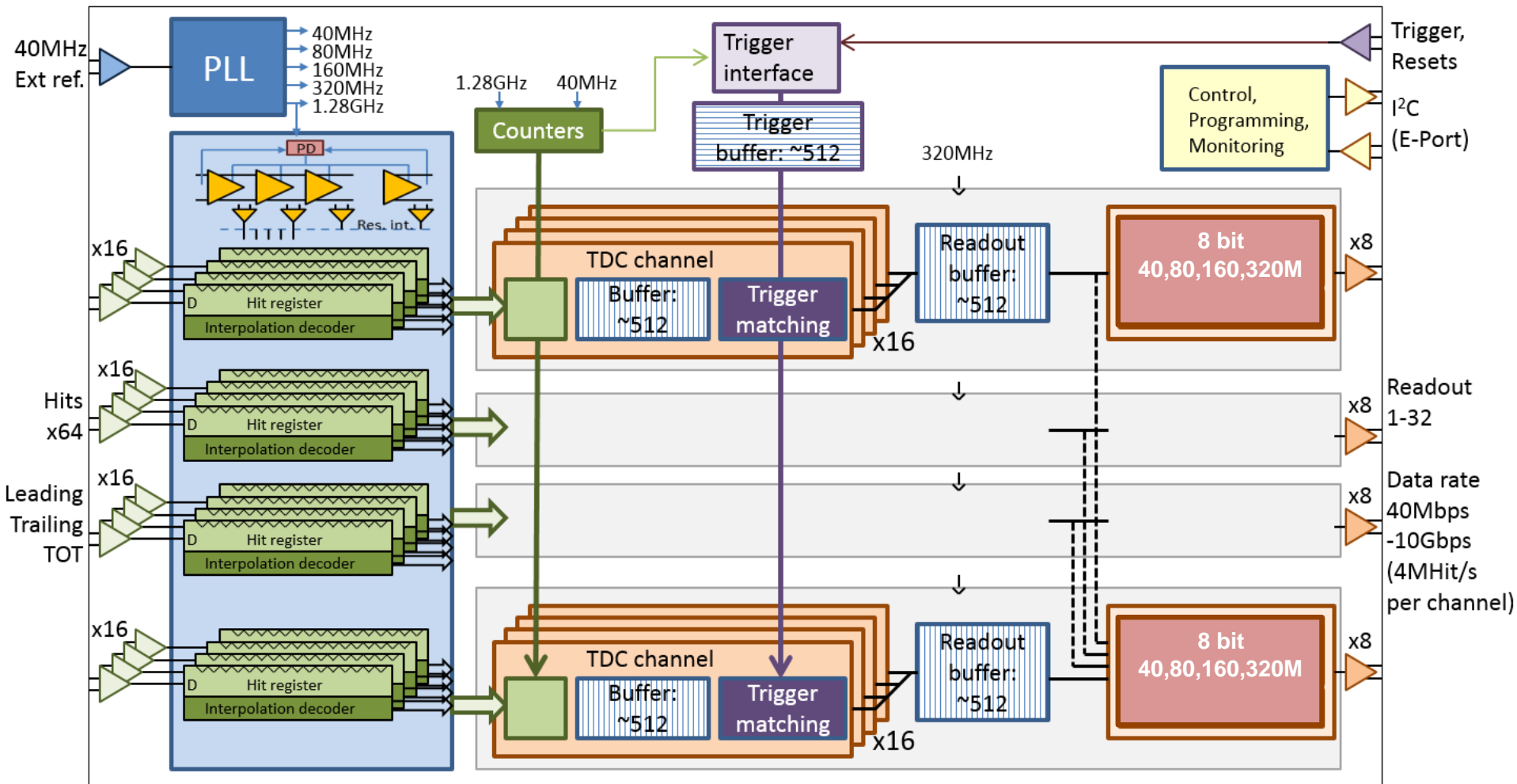
INL can be corrected for in software

DNL, Noise and jitter can not be corrected
(single shot measurements)

Mapping to TSMC 65nm

- Uncertain long term availability of IBM 130nm (now Globalfoundries)
- 2x time performance: -> 3ps binning
- Lower power consumption: $< \sim 1/2$
 - $\sim 1/8$ if DLL binning of 12ps enough (RMS ~ 4 ps).
- Larger data buffers
- More channels
- Smaller chip
- But higher development costs

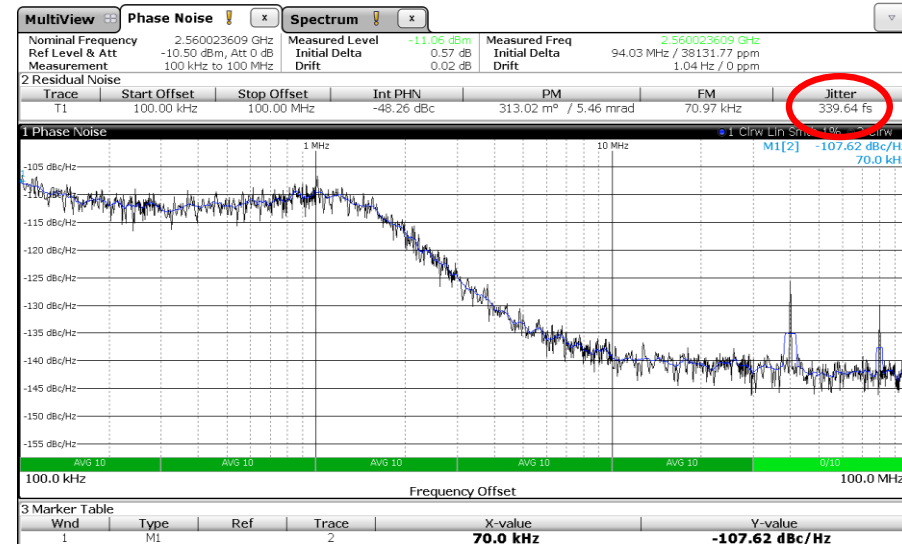
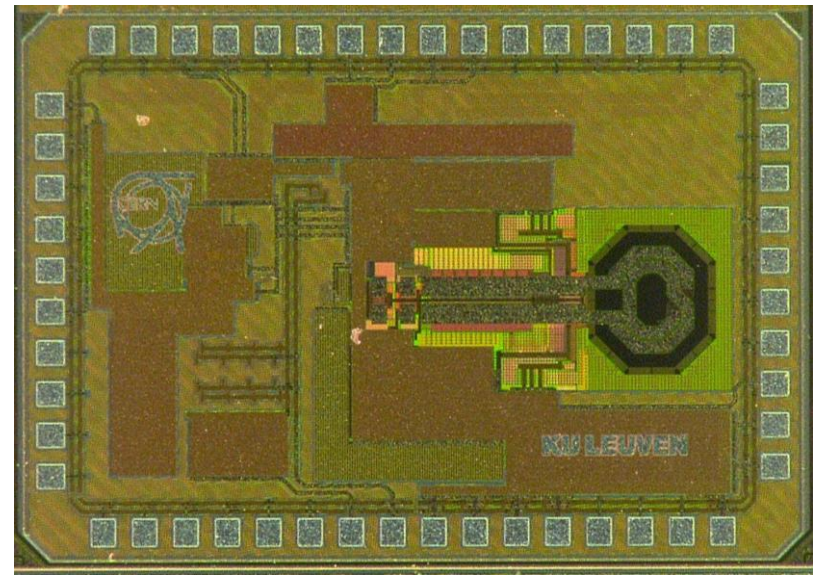
picoTDC Architecture



64 channels, 3ps or 12ps time binning, 200us dynamic range

Low Jitter PLL

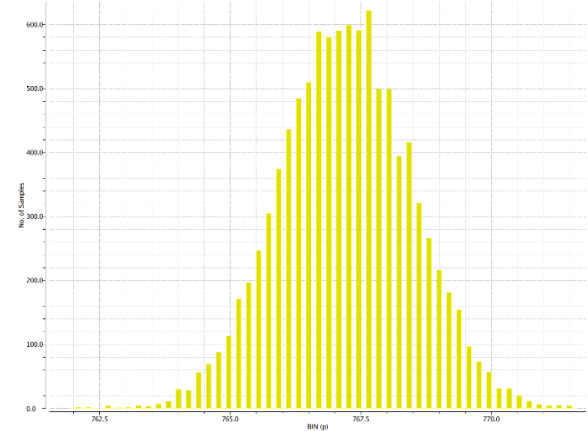
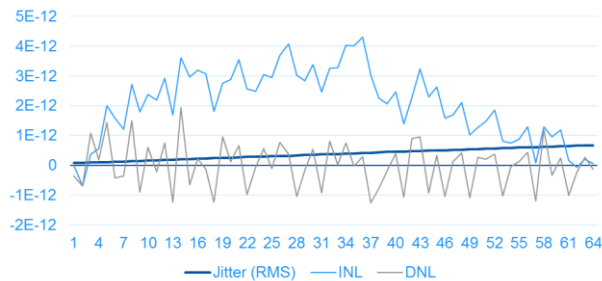
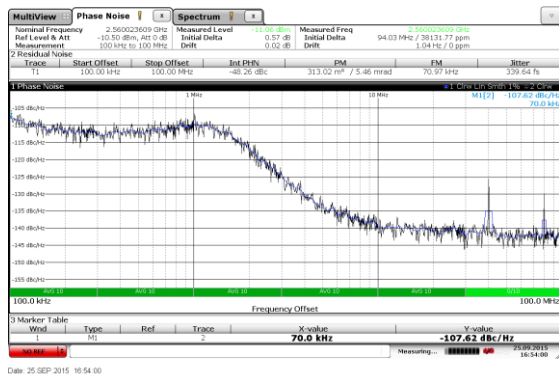
- Clock multiplication from 40MHz to 2.56GHz for fine time counter and time interpolator
 - Low jitter critical
 - Jitter filtering of 40MHz clock to the extent possible
 - 40MHz reference MUST be very clean
 - LC based oscillator
- Design: Jeffrey Prinzie, KU Leuven
- Detailed layout and optimization
- Prototyped May 2015
- Measurements very promising (350fs RMS jitter)



Phase Noise vs. Freq. Offset

Sources of Measurement Deviation

- Bin size 3ps -> 880fs RMS
- PLL: 350fs RMS phase Jitter
- DLL: 400fs RMS phase Jitter, INL/DNL can be calibrated
- Capture FFs: <1ps mismatch (DNL)
- Hit receivers: <1ps jitter
- ~1.75ps RMS total deviation
- External sources: input clock jitter, signal preprocessing



TDC Logic

- Synthesized logic from SystemVerilog RTL
- Based on data driven architecture from HPTDC
 - Simplifications with individual buffers, 512 words per channel
 - Clocking: 320 MHz
 - Trigger matching based on time measurements
- Extensive verification environment
- New interfaces defined and implemented
 - Control/monitoring, Trigger, Readout

Logic Features

- Untriggered or triggered with configurable latency and length, overlapping possible
- TOT or leading and trailing separate
- Relative or absolute time with triggers
- Naturally overflowing counter used for calculating trigger matches, TOT etc.
- Counter with arbitrary overflow and reset for machine cycle, can be inserted in event header when triggered or in measurements when untriggered

Constraints on Hit Signals

- Max. one edge per 1.28GHz-Cycle ($\sim 0.8\text{ns}$)
- Internal glitch filter
 - Filter time can be programmed to enforce the 0.8ns or more for filtering e.g. oscillations
- Small derandomizer (4 hits) for each channel running @1.28GHz
- Sustainable rate to channel buffer 320MHz, trigger matching running @320MHz for each channel separate
- No bottlenecks until readout buffers
- Trigger in each 40MHz-Cycle possible

Readout

- 1 or 4 readout ports
 - 4 ports: High rate applications (e.g. non triggered)
16 TDC channels per port
 - 1 port: Low-medium rate
64 channels (or 32 channels in 32 channel mode)
Round robin with channel group separators, max. consecutive hits per group can be configured
- Readout data: 32bit words
 - Headers, trailers, TDC data, status, etc.
- Readout ports interface
 - Byte wise:
 - 40, 80, 160, 320 MHz
 - Sync signal to mark first byte of word
- TDC readout bandwidth:
 - Max: $8 \times 4 \times 320\text{Mbits/s} = 10\text{Gbits/s}$ ($\sim 4\text{Mhits/s}$ per channel)
 - Min: $8 \times 40\text{Mbits/s} = 320\text{Mbits/s}$

32 Bit Frames

TDC measurement



Event headers (up to two)



Possible fields: event ID, Bx ID, natural ID, status & monitoring

Event trailers (up to two)



Possible fields: event ID, Bx ID, natural ID, #hits, status & monitoring

In untriggered mode, trigger input can be used to generate headers with selectable data (e.g. internal counters)

Errors/status



Channel group separator (for single readout port)



Absolute TDC data

Full TDC data, **DEFAULT FORMAT**



Relative to Trigger

A: Triggered with relative time: Same as absolute

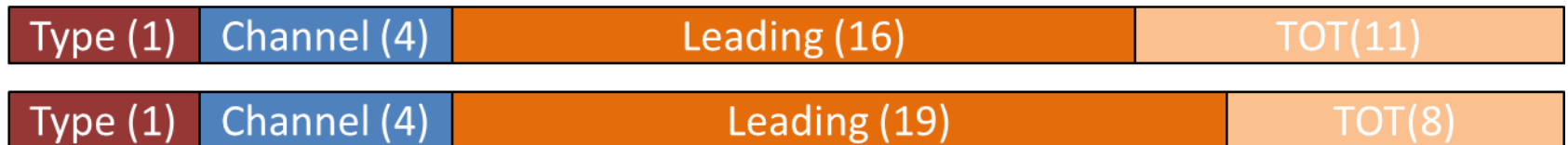


B: Triggered with relative leading and TOT: Same as absolute Lead. + TOT



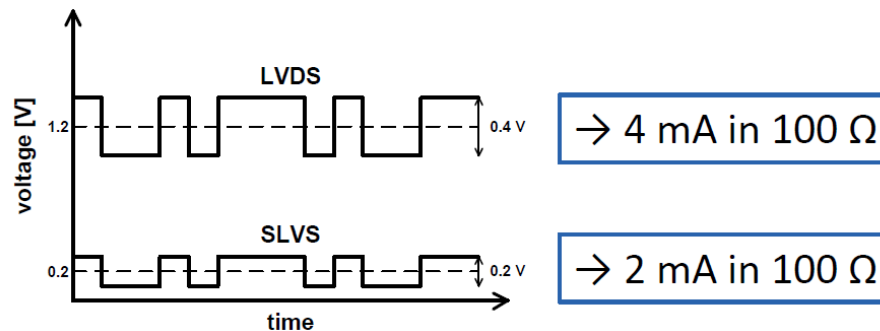
Leading + TOT

- Packet Type: 1 bit
- Channel ID: 4 bits, for single port readout +2 bit group separator
- Leading: 16/19 bits
 - Large dynamic range
 - 16bit 3ps resolution: 200ns
 - 19bit 3ps resolution: 1600ns
 - **Programmable part of full 25bits leading TDC**
 - **(Relative to trigger to be useable)**
- TOT (Relative to leading): 11/8 bits
 - Short dynamic range:
 - 8bit 3ps resolution: 780ps
 - 11bit 3ps resolution: 6.1ns
 - **Programmable part of full 25bits TOT difference**
 - TOT assumed to be used for offline time-walk correction of leading.
- Alternative: Readout of Individual Leading and Trailing edges with full range/resolution
 - 2x readout bandwidth



Electrical Interfaces

- Hits: Differential (LVDS “compatible”, common mode from 0.2V to 1.2V)
 - Highest speed (resolution) @ ~800mV common mode
- Time reference: 40MHz differential
 - Low jitter reference critical for high time resolution
- Trigger/Event-Rst/BX-Rst/reset: Sync Yes/No
- Control/monitoring: I²C at CMOS 1.2V-levels
- Readout: 4 readout ports byte wise differential signals
 - Common mode 0.6V, programmable current 1-4mA
 - Compatible with LpGBT and FPGAs
- Packaging: 400 pin BGA, 1mm pitch

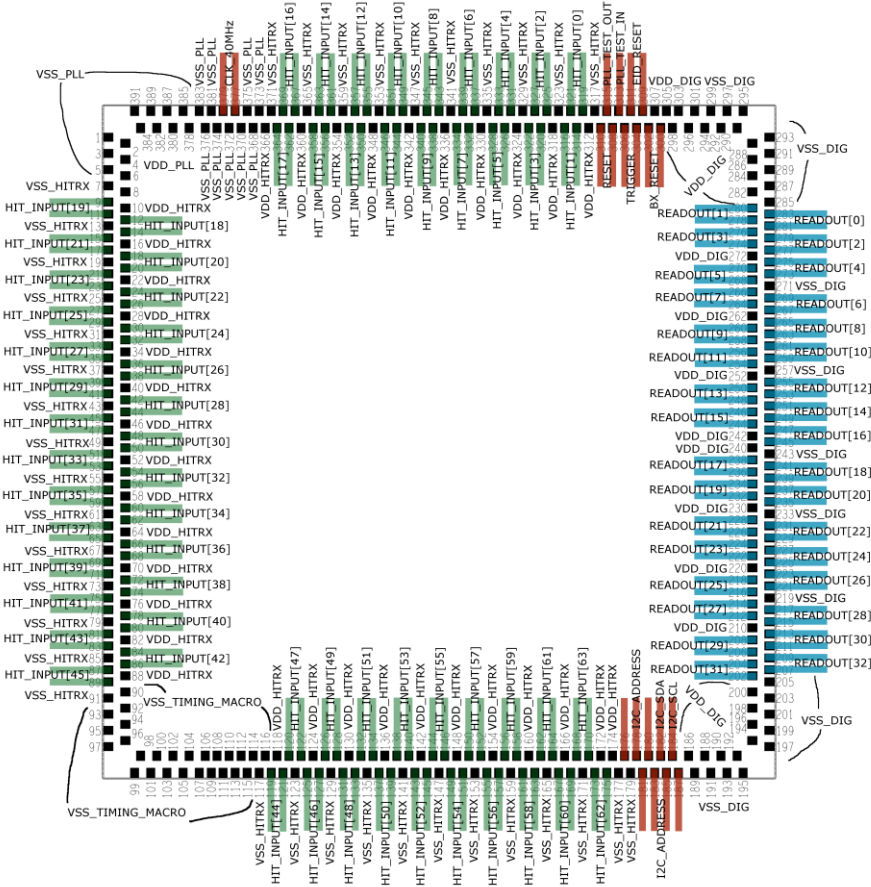


Power

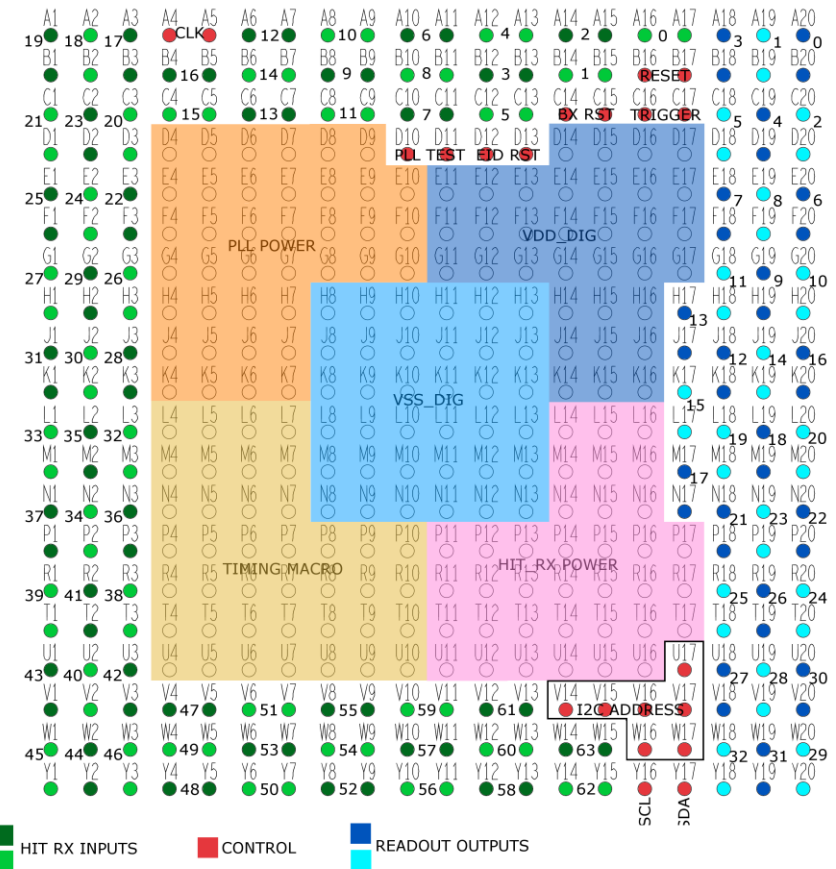
Main power consumption at high resolution comes from timing macro

- 3ps bin size, 64 channels: 1000mW
- 3ps bin size, 32 channels: 700mW
- 12ps bin size, 64 channels: 500mW
- 12ps bin size, 32 channels: 400mW

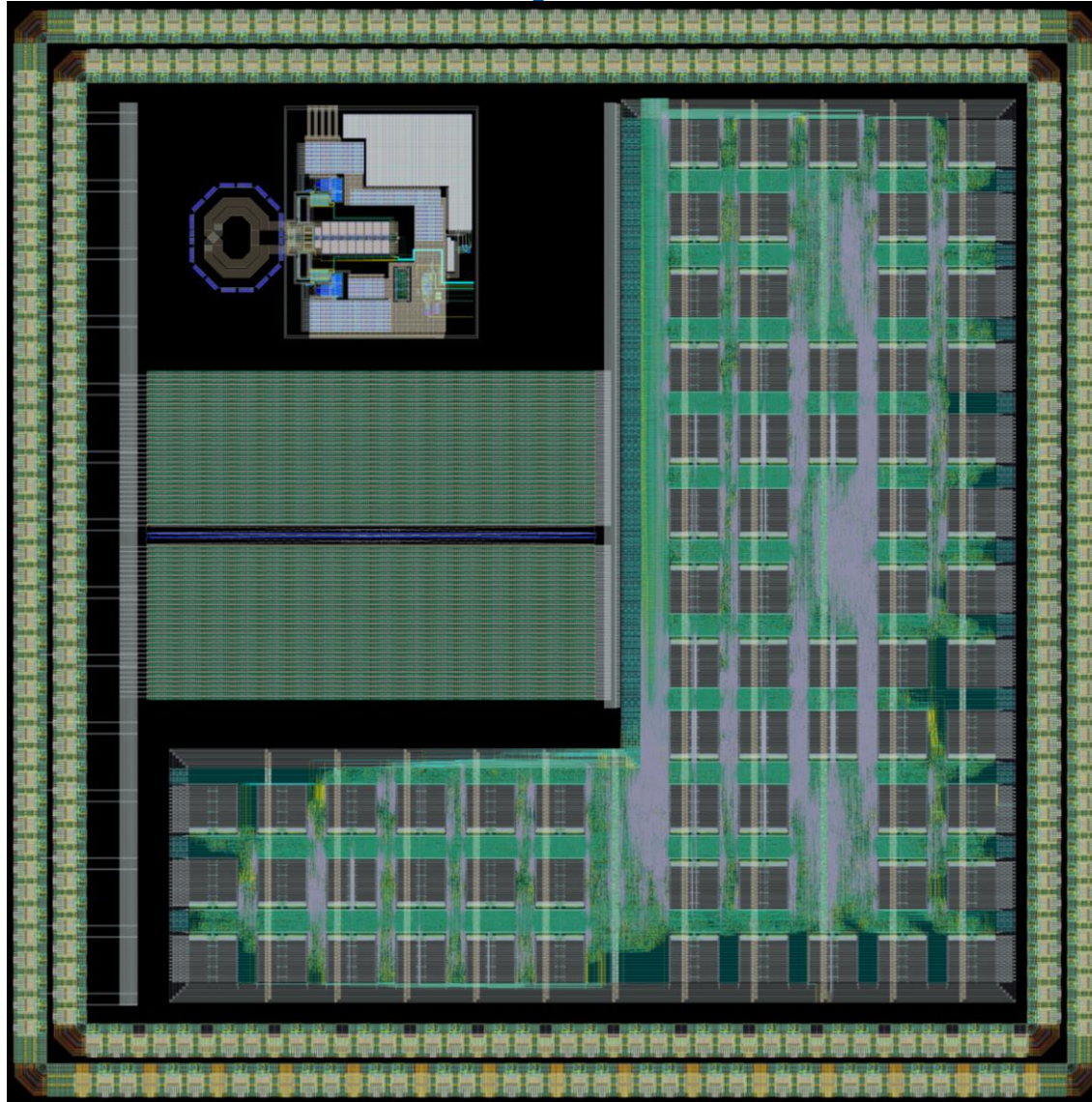
Pinouts

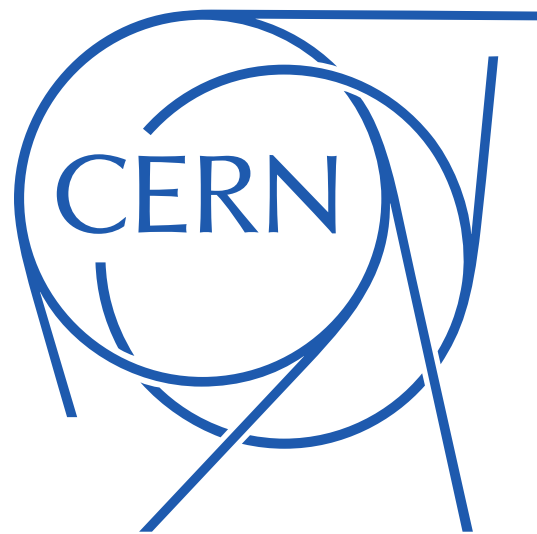


ASIC Die Pinout



Full ASIC Floorplan





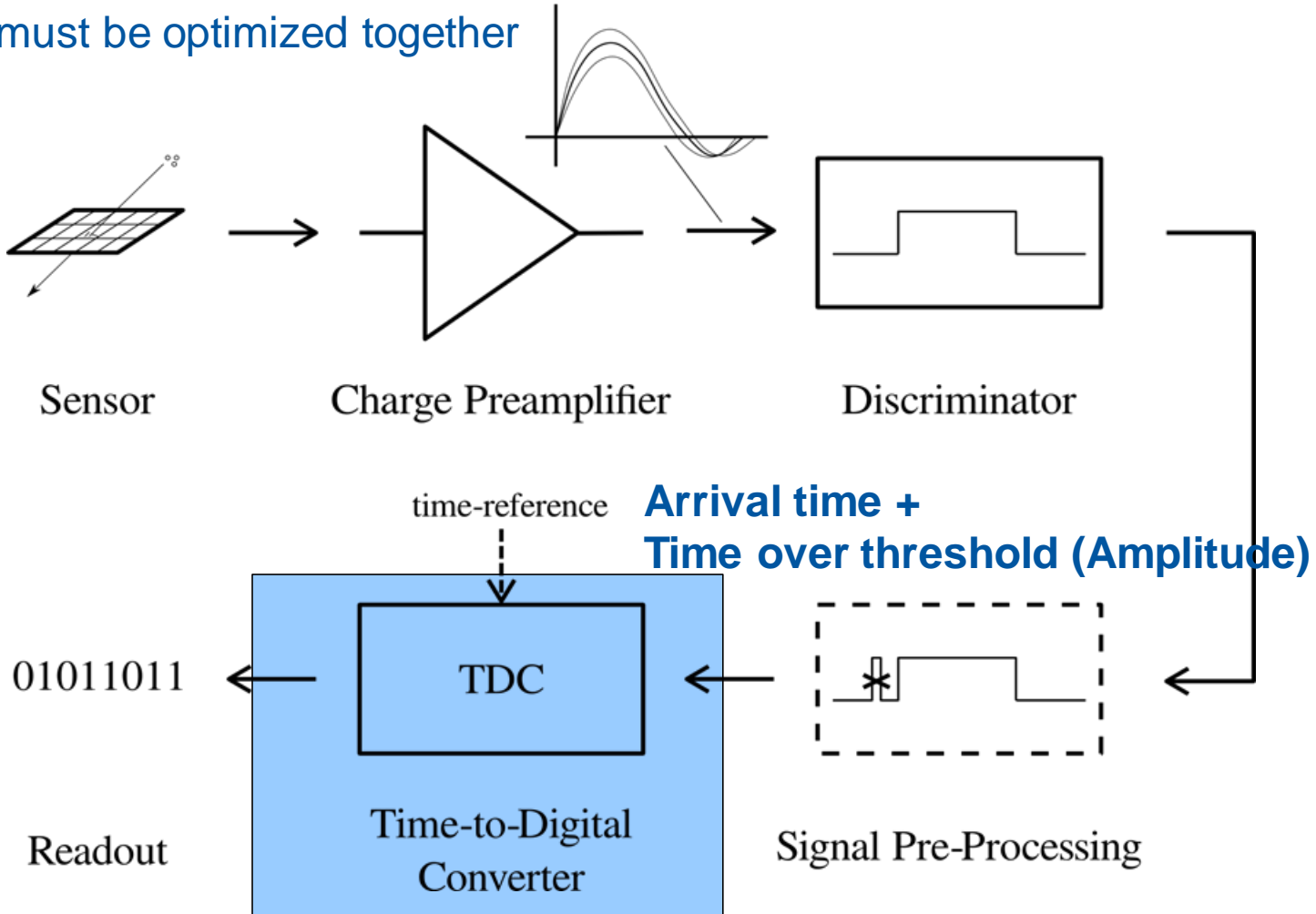
Backup Slides

TDCPix (NA62 Gigatracker)

| | |
|-----------------------------------|---|
| Pixels per chip | 40 columns \times 45 pixels = 1800 |
| Chip size | 12 mm \times 20.4 mm |
| Dissipated power | 3.5 W |
| Dynamic range | 3600 – 60000 e ⁻ (0.6 – 10 fC) |
| Total dose in 1 year | $\sim 10^5$ Gy |
| Time resolution | < 200 ps |
| Peaking time | 5 ns |
| TDC bin size | 100 ps |
| Efficiency per station | > 99% |
| Particle rate per (central) pixel | ~ 140 kHz |
| Particle rate per chip | ~ 150 MHz |
| Data bandwidth | 4 \times 3.2 Gb/s |

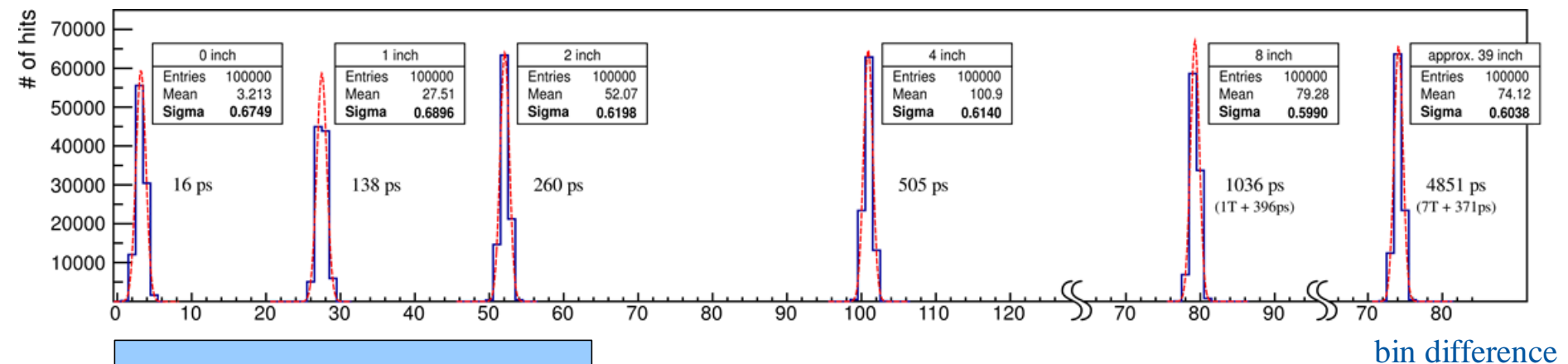
Time Measurement Chain

Detector and discriminator critical and must be optimized together



Single Shot Precision

- Three measurement series using cable delays
 - Both hits arrive within one reference clock cycle
 - Second hit arrives one clock cycle later
 - Second hit arrives multiple clock cycles later (~5ns)



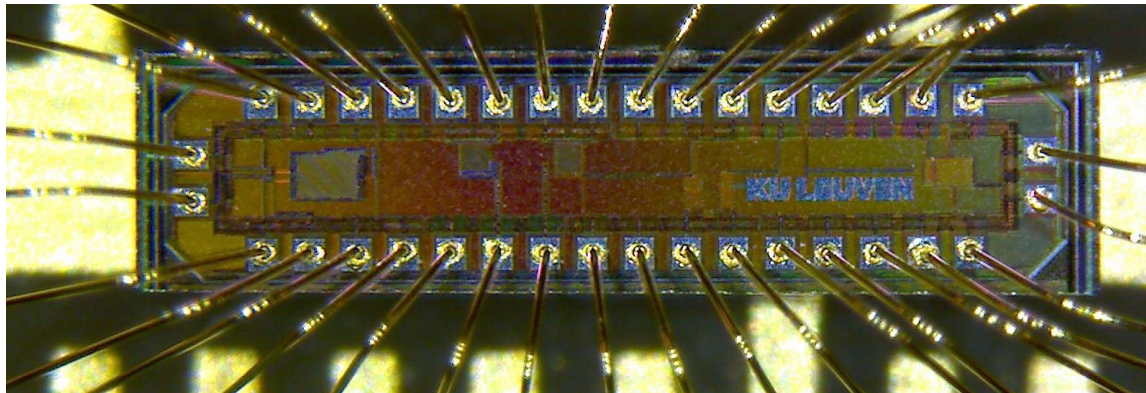
$$\sigma_{\text{TDC}} < 2.44 \text{ ps-RMS}$$

TWEPP2013 slides and paper: <https://indico.cern.ch/event/228972/session/6/contribution/61>

ESE seminar: <https://indico.cern.ch/event/225547/material/slides/0.pdf>

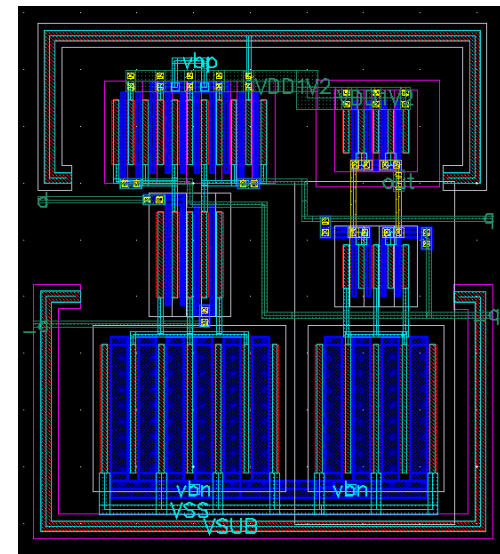
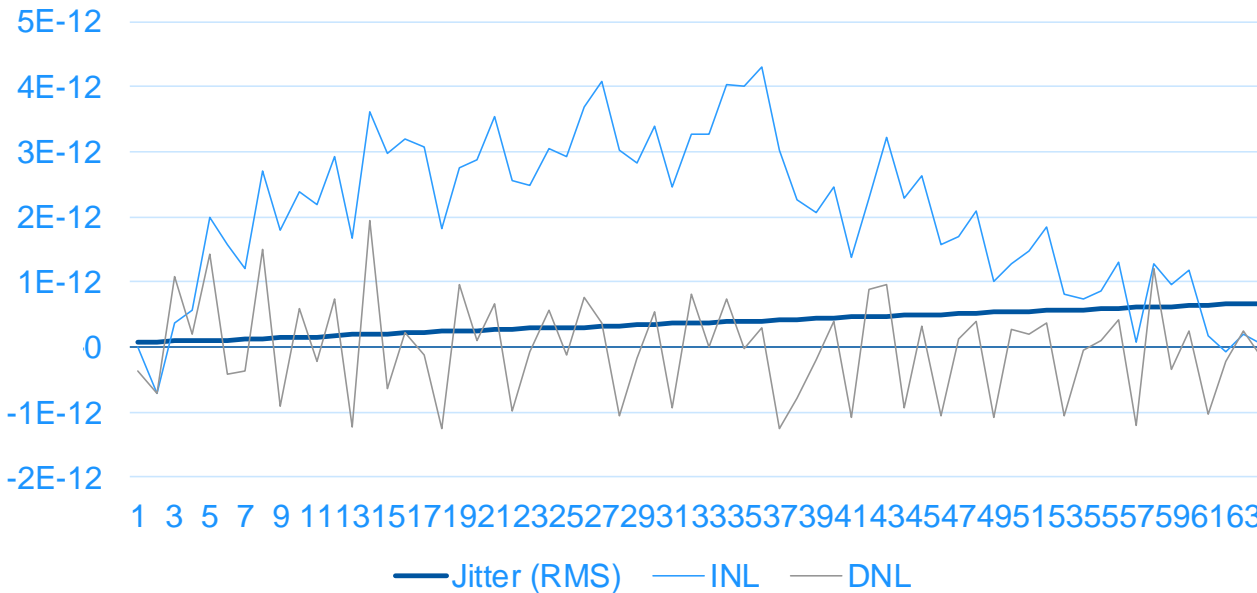
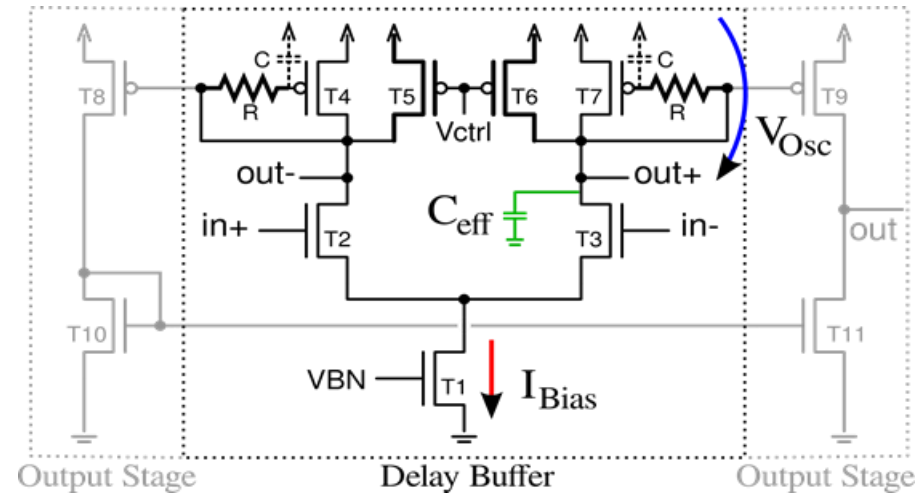
Hit Receivers

- Differential receivers optimized for ultra-low jitter, low power
- Full Range (common mode 0V .. VDD=1.2V), somewhat LVDS-compatible
- Highest speed @ ~800mV common mode
- Optimized for 200mV Peak-Peak amplitude
- Design: Bram Faes, KU Leuven
- Prototyped & tested



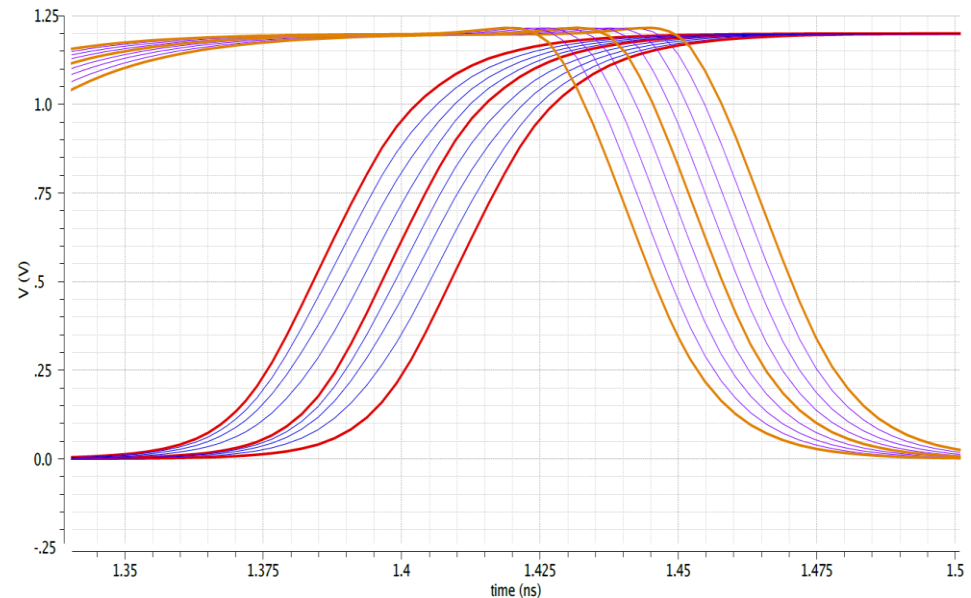
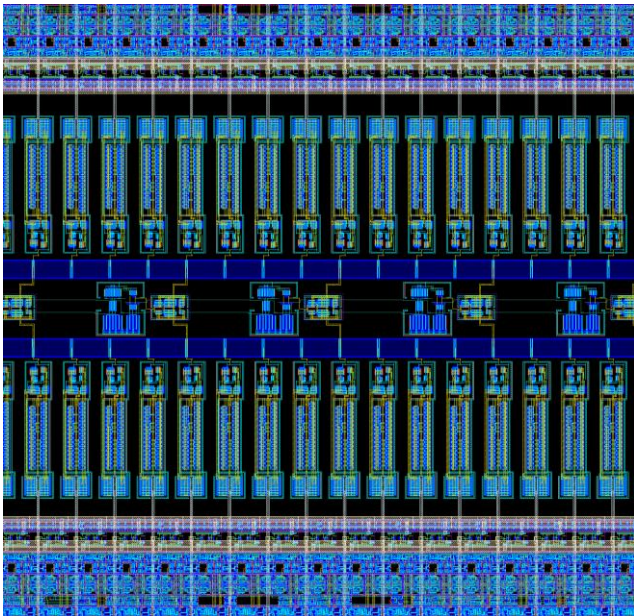
DLL

- 64 taps, 12.2ps delay
- Self-Calibrating
- Jitter not as critical, doesn't pile up



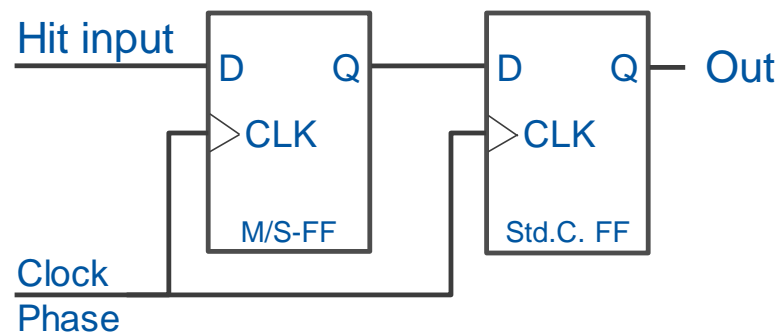
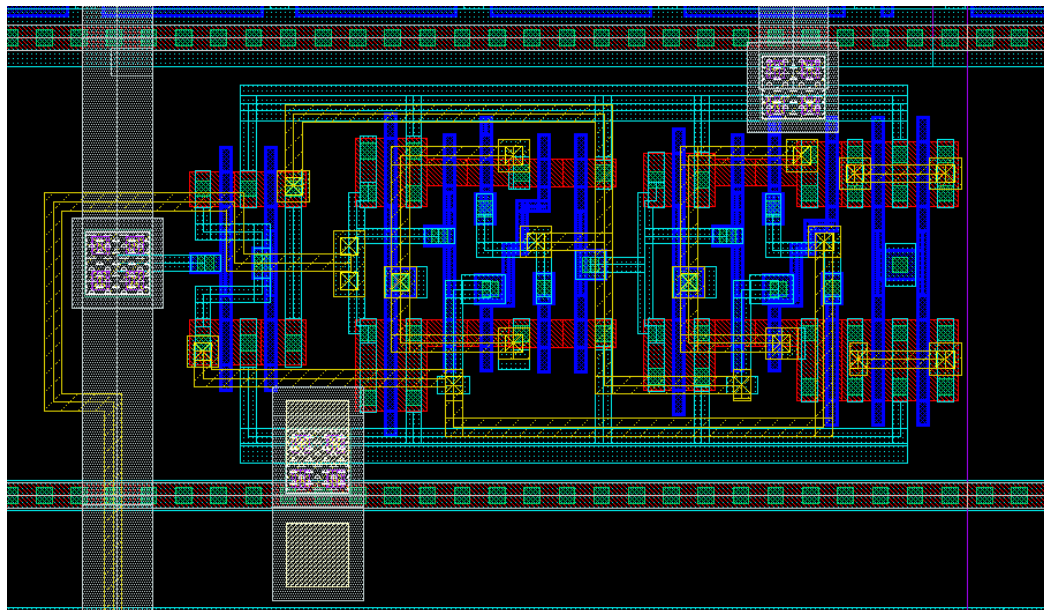
Resistive Interpolation and Drivers

- Get down to 3ps bins
- Drivers: tapered buffers, each driving 32 FFs
- Calibration separate for each half

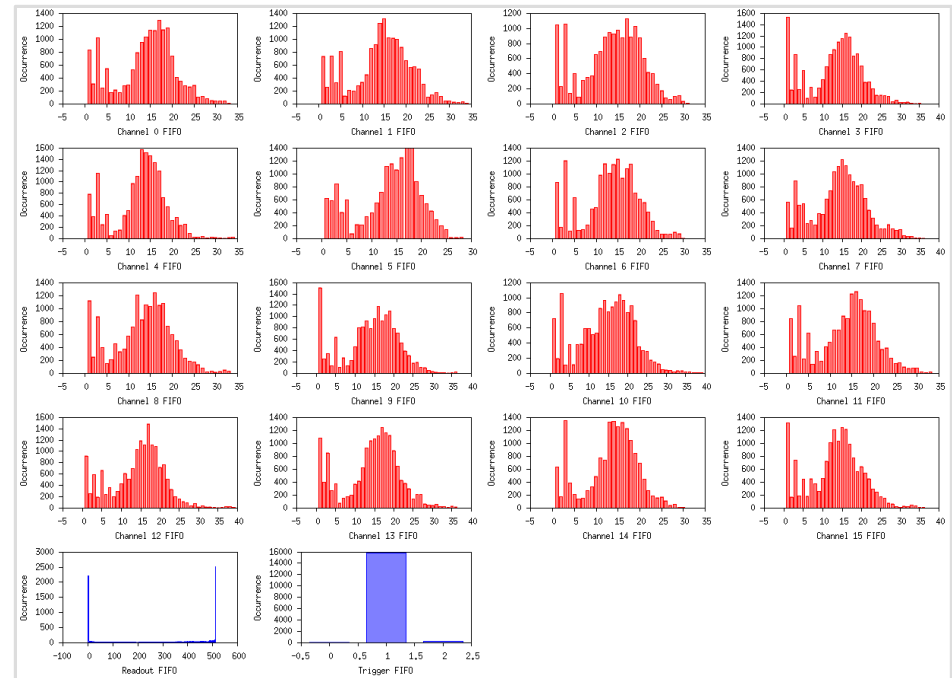
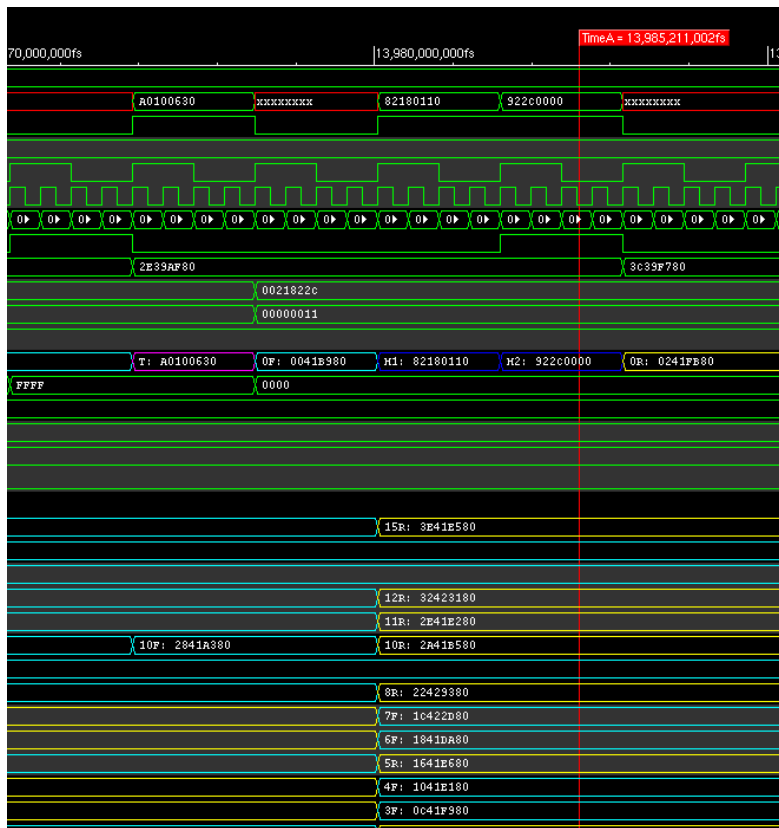


Capture Flip Flops

- Revisited design, timing vs. power very critical, 16k capture Flip Flops running @ 1.28GHz
- Highly optimized M/S Flip Flop followed by standard cell Flip Flop for metastability resolution
- Monte Carlo simulations show a mismatch of 800fs RMS, noise influence of 240fs RMS



Verification Environment



```

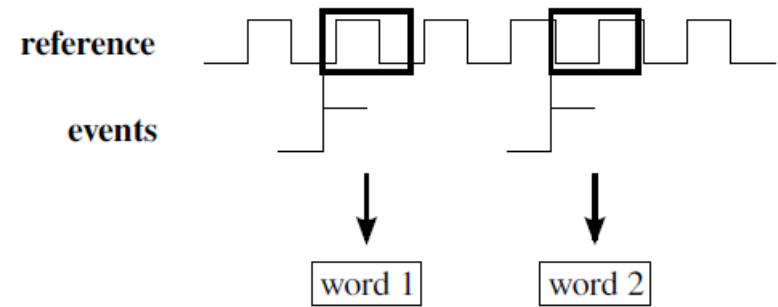
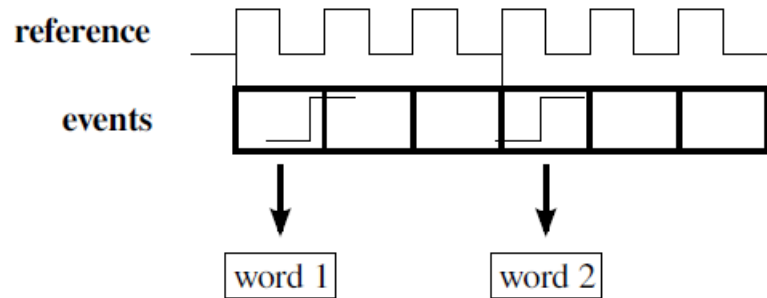
Matching trigger header: 911 27
Matching trailer: 27 101 hits
Matching trigger header: 925 28
Matching trailer: 28 107 hits
Matching trigger header: 942 29
23573019ps: Missing Rising hit at channel 1
23591087ps: Missing Falling hit at channel 5
23595000ps: Missing Rising hit at channel 10
    
```

- Verification in SystemVerilog
- Use cases can be defined and automatically tested, visualization of buffer occupancy, lost hits etc.

Verification Features

- Environment supports and verifies all TDC features
 - Triggered / untriggered
 - Rising / rising&falling / TOT
 - Different counter and reset settings
- Extensive test cases
 - High / low / burst hit rate
 - High / low trigger rate, overlapping triggers
- Specific use cases can be defined, verified

Capture Scheme



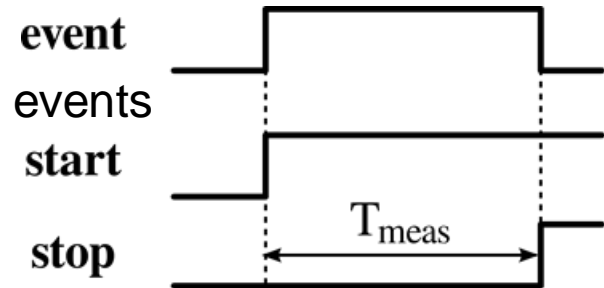
Synchronous

Asynchronous

Time Measurements

Start - Stop Measurement

- Measure relative time interval between two local events
- Small local systems and low power applications



Time Tagging

- Measure “absolute” time of an event (Relative to a time reference: clock)
- For large scale systems with many channels all synchronized to the same reference

