DAQ and FEE Architecture for COMPASS Beyond 2020

Igor Konorov

COMPASS Beyond 2020

DAQ/FEE/Trigger Workshop

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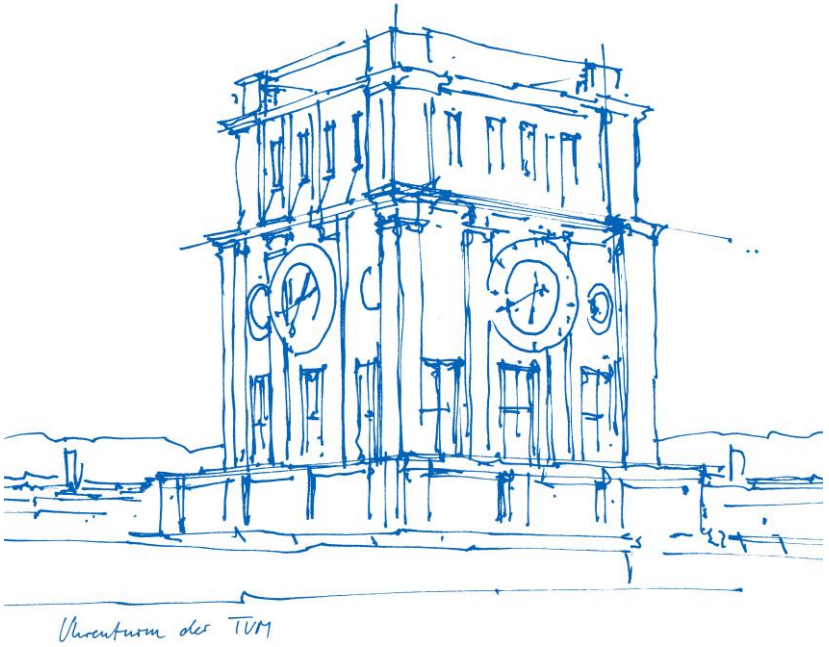


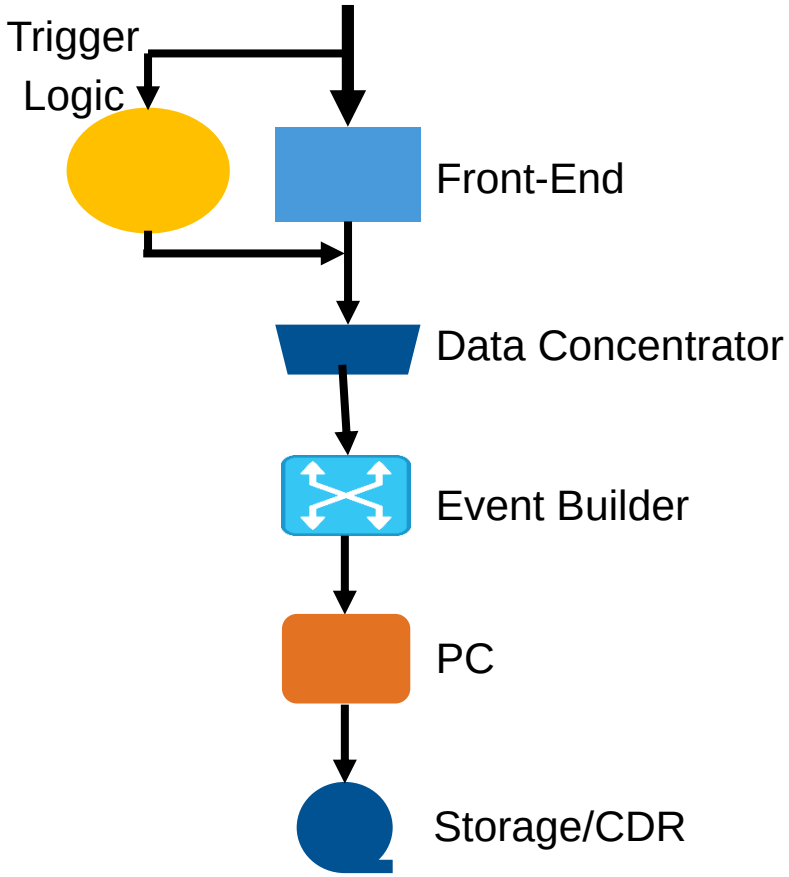
General Comments

Requirements for new developments of DAQ, FEE and Trigger

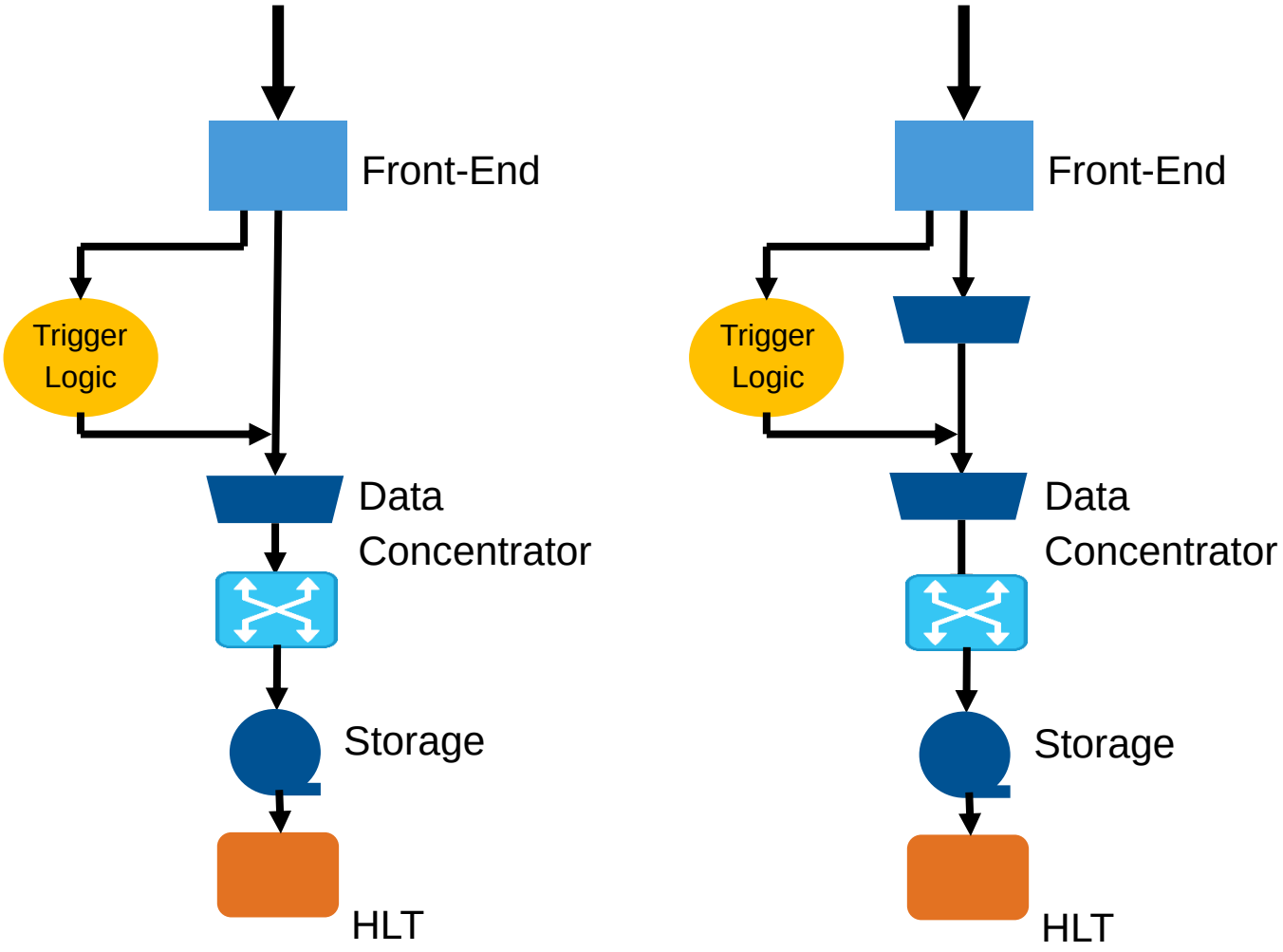
- Most of foreseen measurements require 100kHz trigger rate capable DAQ
- Proton radius measurement requirements are tuned towards DAQ capability and
- We may get new requirements

New FEE hardware developments can be done to fulfill trigger less requirements without big cost penalty … I think

COMPASS 2 DAQ Architecture



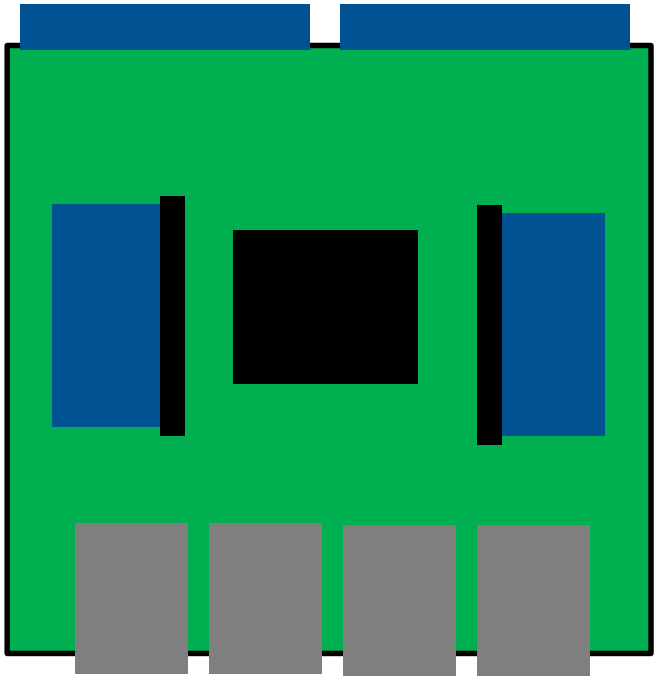
Possible DAQ Architecture



Development of Kintex UltraScale DAQ Module

Technical parameters :

- XCKU095-A1156
  - 1.2 M logic cells
  - 60 Mbit Block RAM
  - 64 x 16Gb/s
- **2 x 16 GB DDR4 SODIMM, combined data throughput 10 GB/s**
- AMC connector Interfaces
  - TCS
  - Ethernet(IPBUS)
  - 15 x 16Gb/s
- Front panel interfaces
  - 48 x 16Gb/s



Applications : Data Concentrator, Event Builder, Trigger

Strategy for New Developments

FEE :

- Trigger less capability : triggered and not triggered read out streams
- Data of any detector can be used for triggering
- Local buffering limited in size to overcome data rate fluctuations, no requirements to store data for trigger decision
- FEE Interface based on Serial links with UCF protocol
- IPBUS for slow control and monitoring

Strategy for Trigger Logic

Switch to Digital Trigger Processor
Complete development of configurable digital trigger logic
Use UCF protocol for data transmission
IPBUS for configuration
Common hardware between DAQ and Trigger Logic

Preferable Standards for New Developments

ATCA Shelf

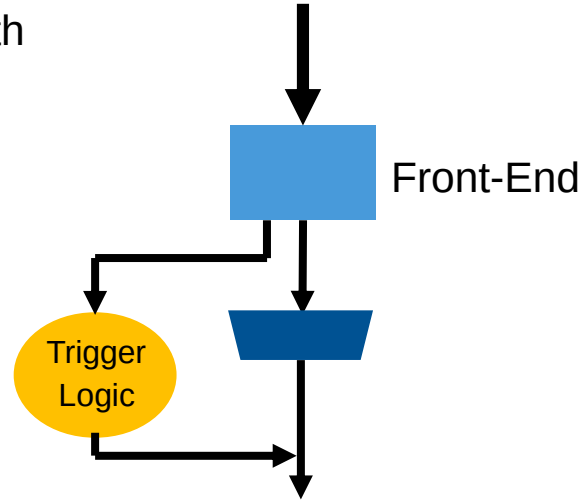
- Relatively cheap
- ATCA carrier card - should be common
- AMC plug-in cards of different sizes
- Controlled cooling power
- Simple redundant power supply of 48V
- Quite complex IPMI technology for power and temperature monitoring. Optional !
- Time cons

ATCA card developed
by our group for Belle2

Possible solutions for trigger less read out

1. No trigger at frontend level
   - T0 – beam trigger
   - Time slices
     - Data divided in time slices of equal length in the order of 10us to 1ms

   event == time slice
     - Data divided at big time intervals between triggers dT0 > 0.5 us
   - Front end module provides data blocks for each time slice
     - Block header : absolute time with a precision of slice length
     - Hit : channel # and hit time within time slice
   - Data on borders are copied to both time slices
2. Data buffering within FPGA
3. Possibility to buffer data in DHmx module until Trigger
4. Two stages of data reduction
   - FPGA HLTrigger 0
   - Software HLrigger 1



Data rate estimation (very preliminary)

COMPASS event size : 30kBytes
With assumption that one event covers 0.5us time interval => 60GB/s

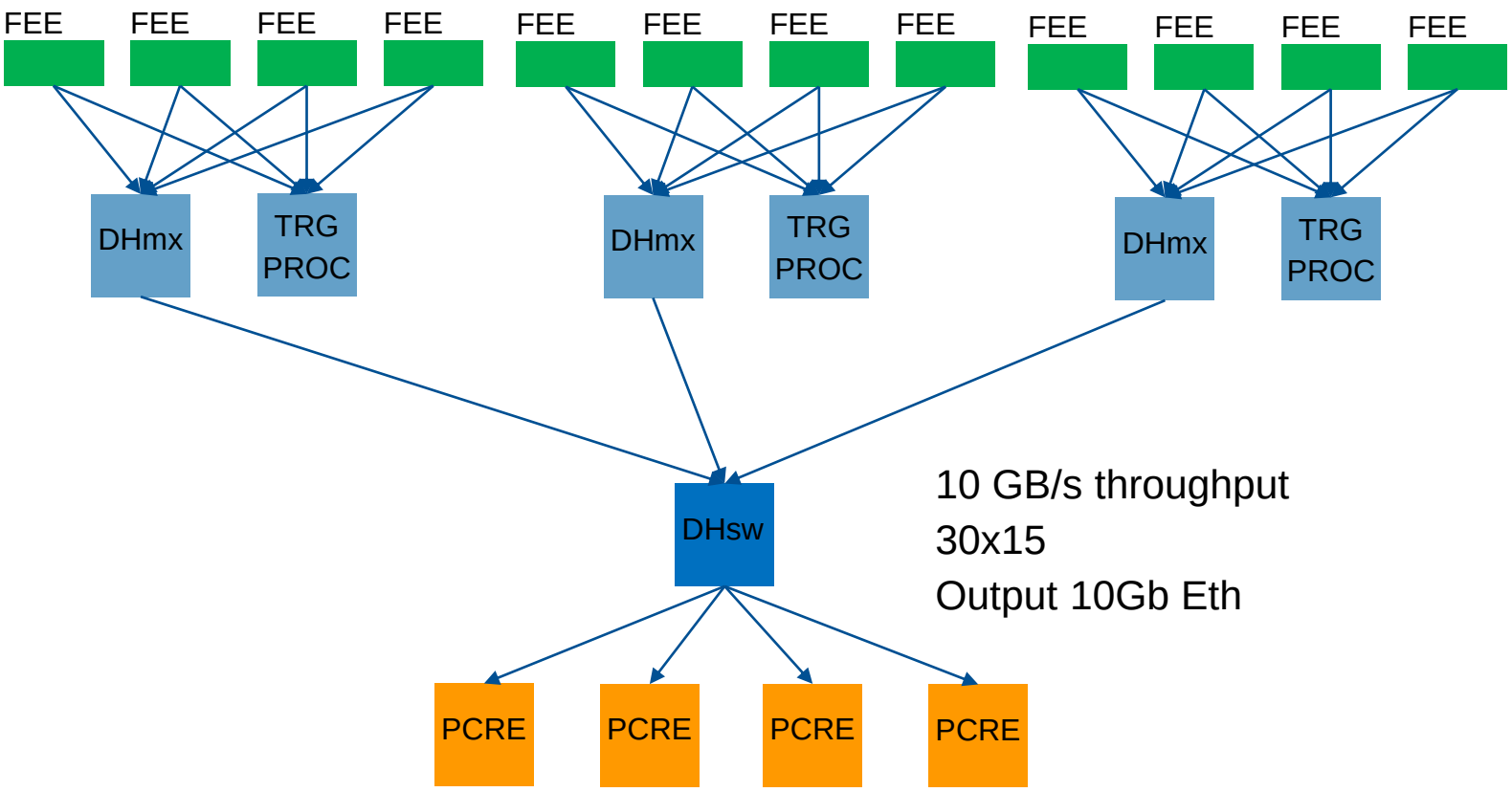
Possible data reduction at FE :

- Calorimeter :
  - Substitute 32x12 samples by Time and Amplitude => 32 bit word. Reduction factor 16.
  - More efficient zero suppression algorithm. Additional factor 2
- TDC :
  - More efficient data encoding => factor 2

Reduced event size 5kBytes => 10GB/s within spill or 5GB/s sustained

CDR is capable to store more than 1 GB/s => missing factor 5.

Read Out Architecture



Questions and Tasks

Shall we start development of new FEE ?

List of Tasks

Development of prototype FEE, DAQ and Trigger modules

- Fine time TDC – Freiburg
- TDC for wire chambers – TUM, Torino
- DAQ/Trigger – TUM, Meinz
- Silicon -- TUM
- GEM/MM – Saclay, Bonn

Feature extraction for calorimeter – Warsaw

DAQ Hardware - TUM

DAQ software - Prague, Dubna

Problem with man power

THANK YOU