Proposal for a possible recoil tracker based on double side Si-microstrip detectors

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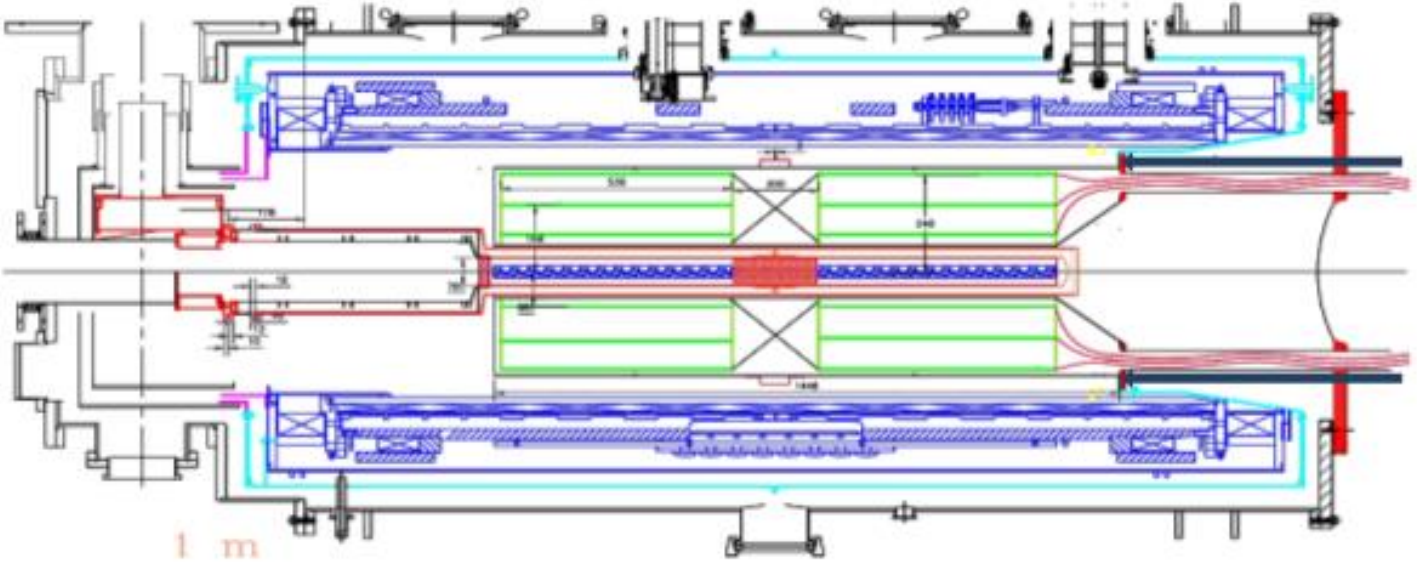
(on behalf LHEP Silicon group)

The possible design of recoil tracker system based on Double-Sided Silicon Detectors is proposed. A coordinate plane consists of 10240 measuring channels, pitch adapter and readout electronics. Each element was tested and assembled into a coordinate plane. The first tests of the plane with ^{106}Ru source were carried out before installation for the BM@N experiment (JINR,LHEP).

BM@N conceptual design report, 2012.
Datasheet-VATAGP7.1, Integrated Detector Electronics AS, 2015.

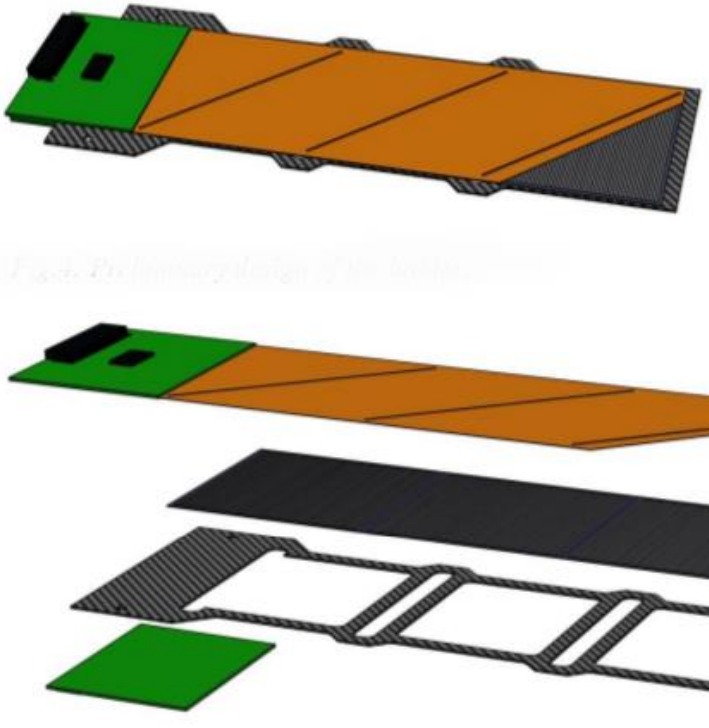
PT modification

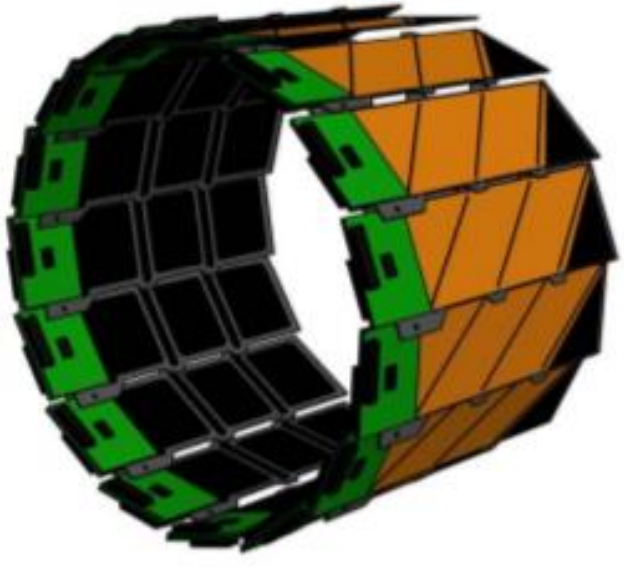


The version of the modified MW-cavity is presented in Figure above. In this option, the silicone detectors are located in the separate blocks. These blocks can be assembled outside of the target. They can be warmed up to about 70 K and protected by heat shields from the helium environment of the target volume with a temperature of about 5K.

The last modification is preferable:
(i)it does not limit the acceptance in the forward direction,
(ii)the length of cables will be minimized and
(iii)“worm” chips can be fixed on the outside surface of the flange at the room temperature and lengths of the target cells can be increased up to 75 cm each.

View of Silicon detector

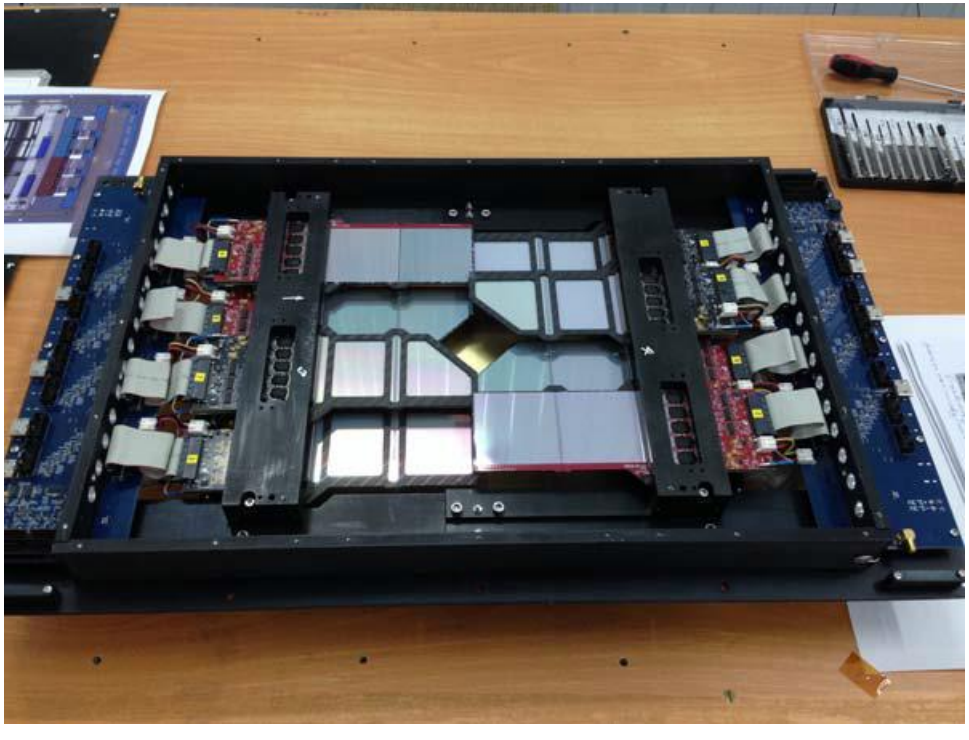




The signals from the Silicon can be delivered by cables to preamplifiers placed somewhere in the downstream, part of the target at the nitrogen or room temperature and then again by cables to the chips outside of the target.

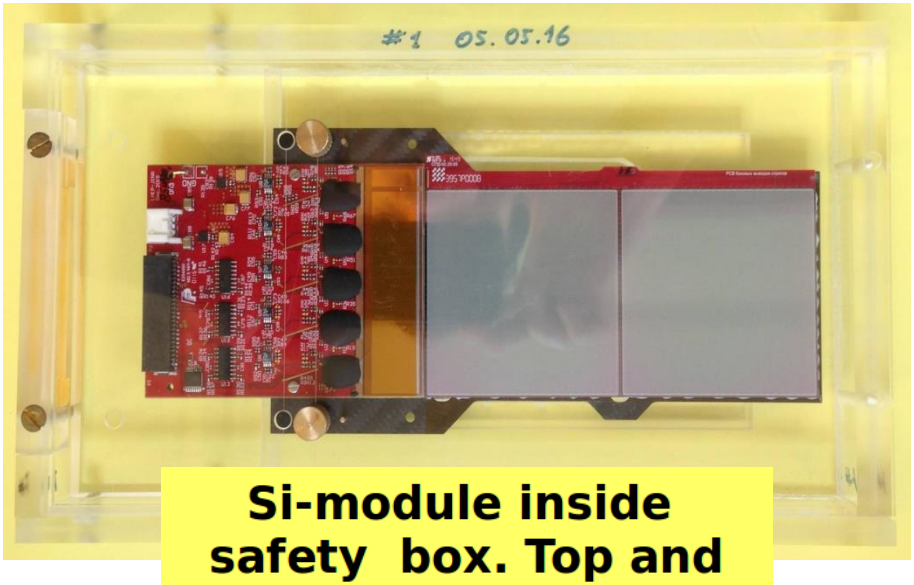
The length of the cables between the Silicon ladders and preamplifiers will be about 1-1.5 m.
Flat capton multilayered flexible boards are to be considered as candidates
(talk by M.Protsenko).

The coordinate plane

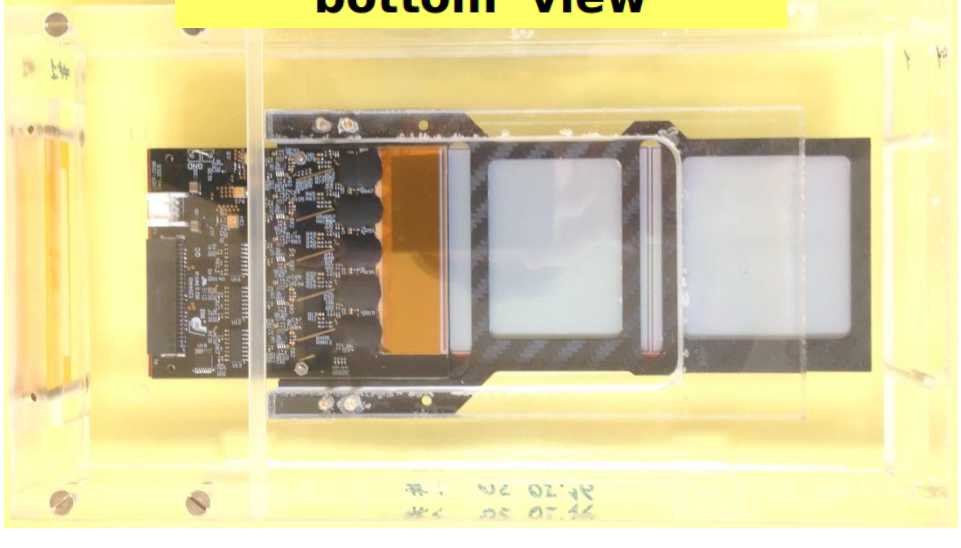


The coordinate plane consist of 8 detector modules with 10240 strips (measuring channels) is assembled on a mechanical frame and placed in a box which is light and electromagnetic shielding. In the center of the plane the inner 4 modules form have a square hole with a side of 50 mm, intended for the beam pipe. All electrical signals – control, information, low voltage (LV), detector bias (HV) are transmitted to the modules and received from the modules through short micro cables to two cross-boards. Each of two cross-boards is responsible for upper and lower half of the coordinate plane of 4 modules by 5120 strips. Analog signals from the output of multiplexer of each chip are transmitted from the cross-board by cable length about 20 m to the inputs of analog-to-digital converters (ADC).

The coordinate plane

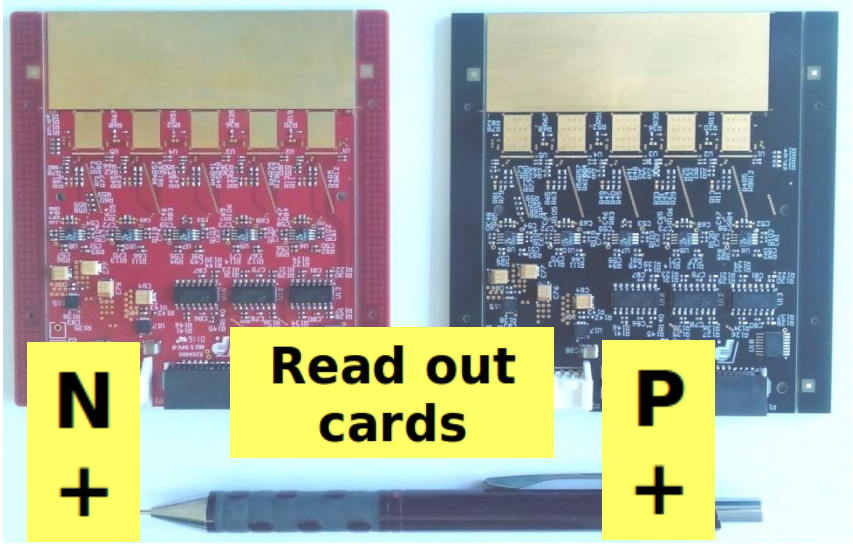


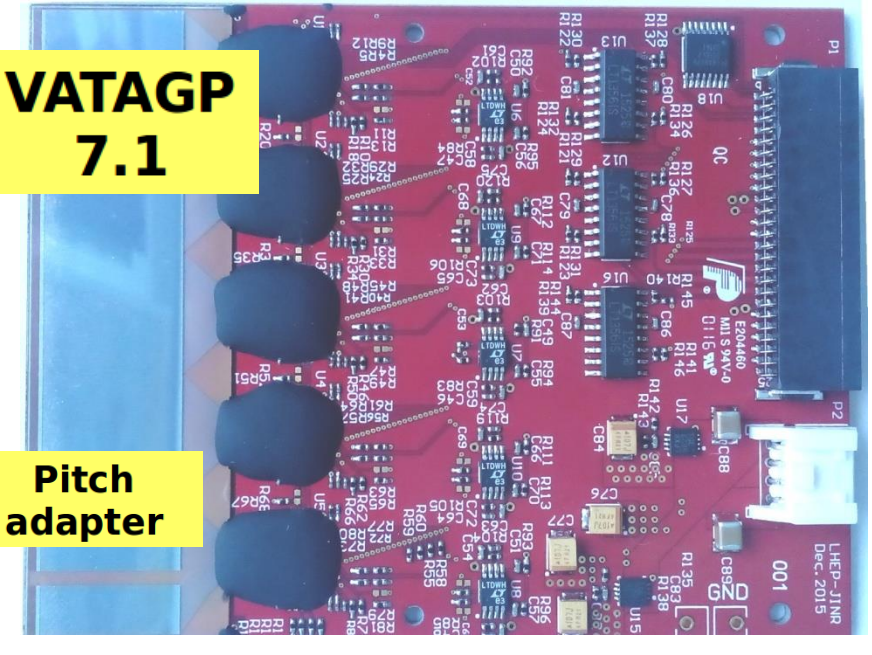
Si-module inside safety box. Top and bottom view



The module consists of two square shape silicon microstrip detector, two electronics read-out cards (one on each side of the detector) and a mechanical frame for precise module positioning, assembling of detectors and read-out cards. Each side of detector has strips, which are continuation of each other, are electrically connected by ultrasonic bonding. DSSD have two types of geometry – square and pentagon. Dimensions of silicon detectors are 63 × 63 mm2, the sensitive area of detectors is 61 × 61 mm2, and the thickness of detectors is 300 μm. Detectors are made on four inch FZ n-type conductivity silicon wafers with resistivity ρ>8kΩ × cm. The total dark current of detectors is < 1μA/120V, full depletion voltage is 40V. Each detector has 640 p+ strips with 0˚ and 640n+ strips located at an angle of 2.5˚. The pitch of p+ strips is 95 μm and the pitch n+ is 103 μm. The capacity of each strip (bulk + interstrip) is 8 pF.

The readout electronics





- Read-out electronics based on VATAGP7.1 ASICs from IDEAS company.
- Each readout card combined of 5 ASICs which give 640 readout channels.
- Each Si-module has two read-out cards.
- One is for N+ side of sub-detectors and other is for P+ side
- Special pitch adapter (SOI- poly silicon resistors 2 MOhm and integrated capacitors 150pF x 150V) on sapphire substrate have been designed for direct connection detector to readout card.

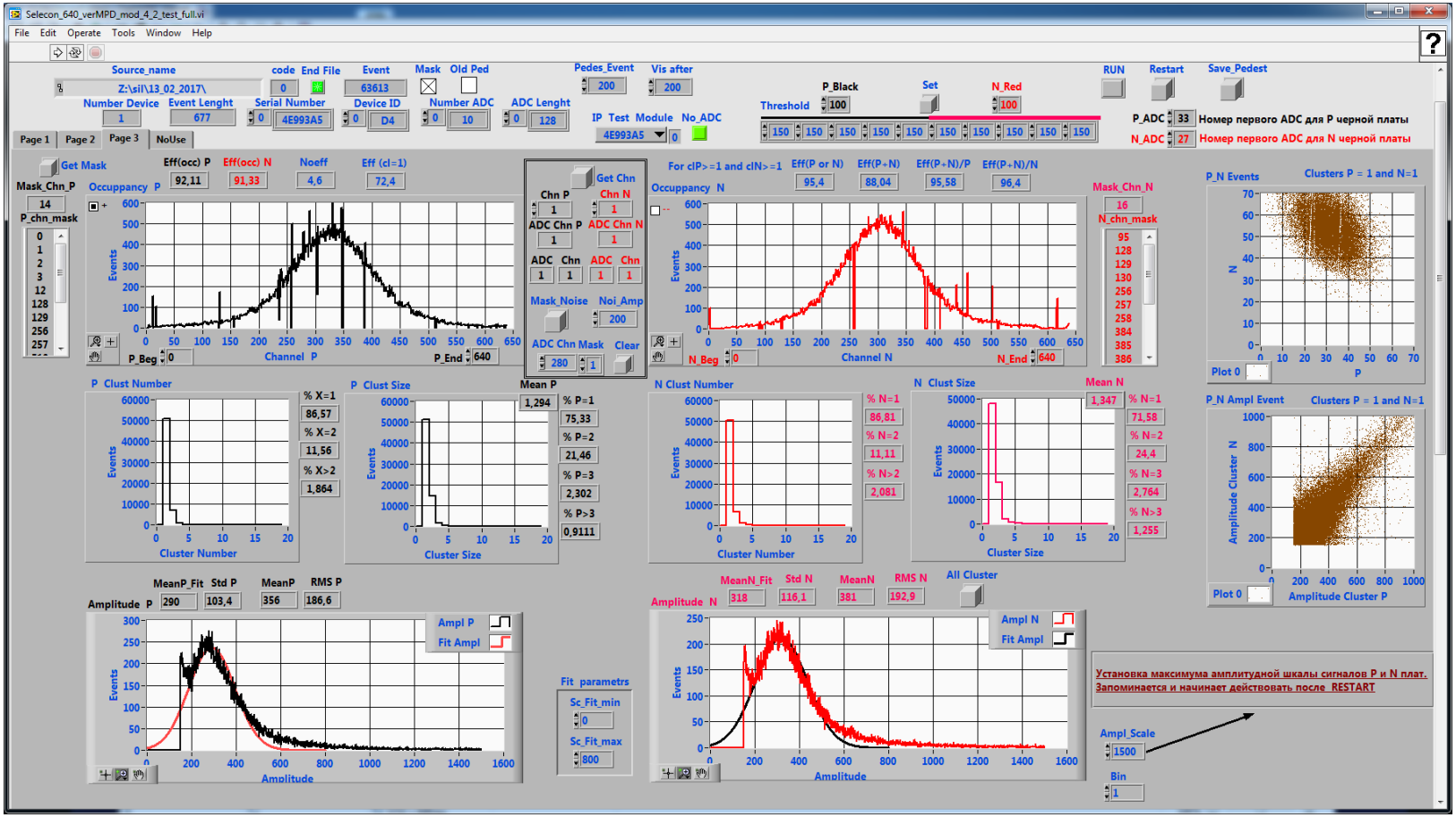
The VATAGP7.1 is a 128-channel charge sensitive amplifier. Each channel features low-noise/low power buffered preamplifiers, shaper with sample/hold, multiplexed analogue readout. In addition, each channel has a fast shaper that gives a trigger signal. Analog specification:

- 128 input analog channels
- Gain – 16.5μA/fC
- Dynamic range ±30fC
- Peaking time (slow shaper) – 500ns typically
- Peaking time (fast shaper) – 50 ns typically
- Electronic noise (zero input capacitance) – 70 e^-
- Electronic noise, slope – 12e^-/pF

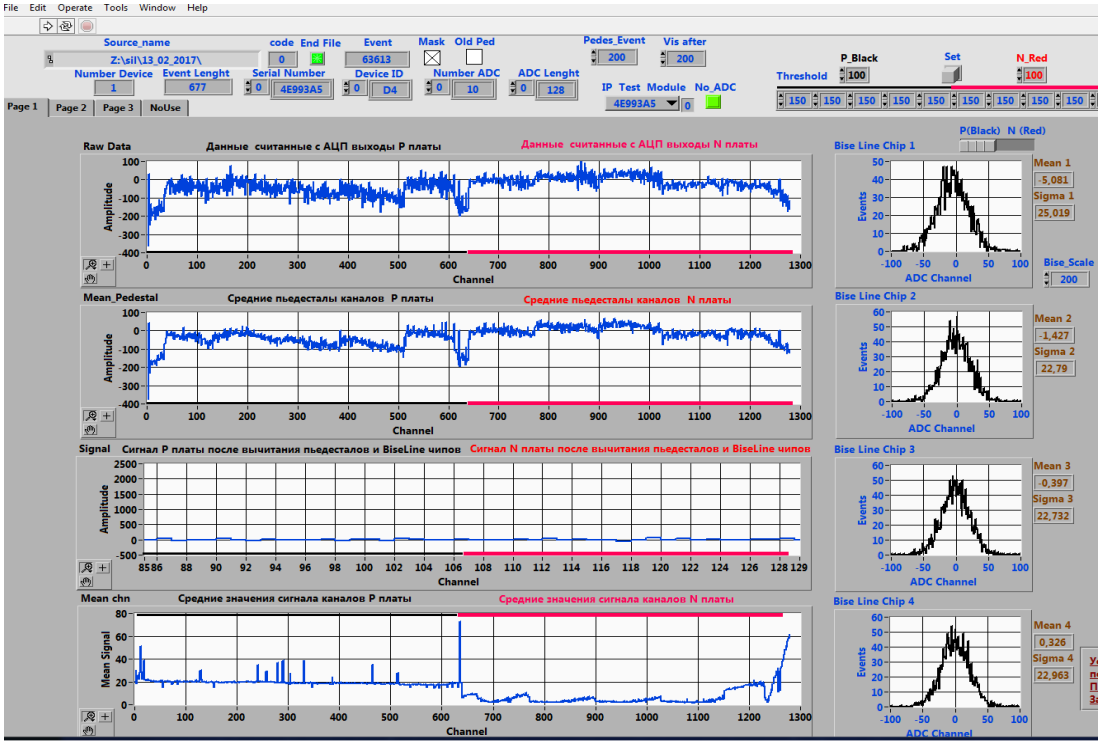
VATAGP7.1 has three different readout modes : serial readout, sparse readout and sparse readout with neighbor channels.

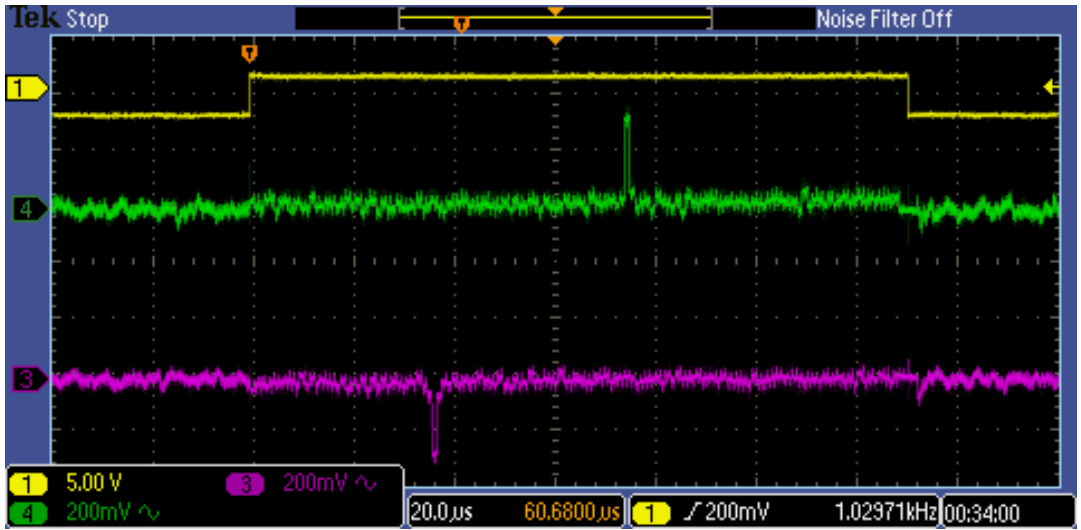
The first tests with ^{106}Ru

- Black colour shows the histograms relating to the X coordinate.
- The red colour shows the histograms relating to the Y coordinate.
- In the upper part of the figure below shows the occupancy from the ^{106}Ru source in coincidence with the scintillation counter, which generates a “trigger”.
- Noisy channels (peaks) and inefficient channels (dips) are less than 3%.
- The lower part of the figure shows the total spectrum of ionization losses for each coordinate.
- Right corner plots give dependence of amplitude of clusters on X-strips from amplitude of clusters on Y-strips.



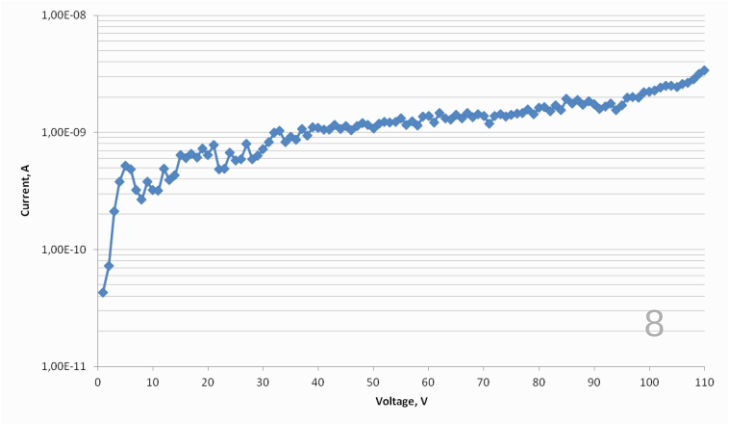
The first tests with ^{106}Ru



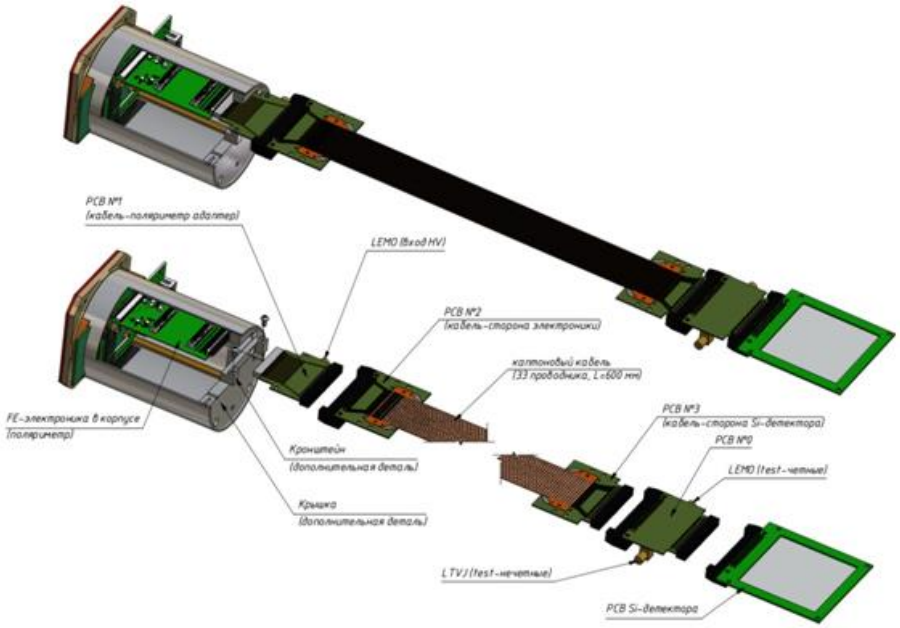


For the DSSD ionization signals from the passage of charged particle induce the same amplitude signal on both p+ and n+ strips. The numbers of the X-coordinate strips go from left to right, and the numbers of Y-coordinate strips go from right to left. The oscillogram shows two track events which demonstrates that the ionization losses of one track significantly exceed the ionization losses of the other track (the Landau distribution).

Total capacitors leakage current vs HV voltage.
Pitch adapter #9, 640 capacitors



The tests with multilayered flexible board



The tests of Si-detector with multilayered flexible boards can be performed in three stages:

- with normal conditions,
using test boards from LTU and equipment of BM&N
(December 2017- under preparation)

- with cryo systems,
possible setup shown below,
need help and supports from COMPASS teams

- using test beams.
need help from COMPASS collaboration

Conclusions

Si-detector developed in LHEP JINR can be as good candidate for Recoil Detector inside COMPASS Polarized target (RTwithRD):

- **main characteristics are met with RTwithRD requirements;**

- **developed and tested in real experimental setup (BN&M);**

- **production is not expensive in comparison with other ones**
  ~ 3K$ for Si detector with sizes – 6.3x6.3 cm^2

Tests with multilayered flexible boards are under preparation

Materials and plots are prepared by JINR LHEP Silicon team,
Leader N.I.Zamyatin