



#### Xilinx 9500/9500XL CPLD Testing CNGS 2009 Update 3.09



TE/MPE/MI

Radiation Working Group

3<sup>rd</sup> September 2009

B.Todd, M. Zerlauth, I. Romera, A. Castaneda





#### MI has installed a Radiation Test Bench "CIRX" which is in CNGS 32 x XC9500 (5V) 32 x XC9500XL (3.3V)





TEY

32 x XC9500 (5V)

9 glitches

15/08/2009 03:12:08.0289 - Beam ON 16/08/2009 15:33:13.7339 - Beam ON 17/08/2009 18:35:46.0737 - Beam ON/OFF 20/08/2009 05:55:53.3168 - Beam ON 22/08/2009 00:40:03.1329 - Beam ON 23/08/2009 05:17:16.3159 - Beam ON 01/09/2009 08:11:19.3216 - Beam ON 01/09/2009 11:15:13.6641 - Beam ON 02/09/2009 08:27:47.7136 - Beam ON

one event doubtful there was beam – will have to look at logging shot-by-shot Could be EMC...

































#### A look in our stock showed:

Device: XC95288 XC95288	Package: HQ208 HQ208	has Pb: Yes Yes	Circuit Revision: A A	Wafer Fabrication Location: E M	Geometry: M M	Year: 05 06	Veek: 13 49	Assembly: A A	Full Lot Number: 1352012A 1433121A	Speed Grade: -10 -10	Temperature: Commercial Commercial
XC95144	PQ100	Yes	A	M	M	03	45	F	1287020A	-15	Commercial
XC95144 XC95144	PQ100	No	A A	M	M	06	45	F	3052264A	-10	Commercial
XC95144	PQ100	No	A	M	М	06	45	F	3031762A	-10	Commercial
XC95144	PQ100	No	A	M	M	07	09	F	3065279A	-10	Commercial
XC95288XL	TQ144	No	A	W	N	09	05	D	3631628A	-6	Commercial

Wafer Fabrication Location Codes:

E = UMC, 8" F = UMC, 8" G = UMC, 12" K = Seiko M = UMC, 8" N = Toshiba P = Philips, MOSIV R = ST Micro W = He-Jian, China Geometry CodesAssembly Codes:H = 1.00umAssembly Codes:J = 0.60um (3-layer CMOS)A = AMKOR KoreaK = 0.85umB = IBM, CanadaM = 0.50um (3-layer CMOS)D = SPIL, TaiwanN = 0.35 (4 metal)D = SPIL, TaiwanP = 0.35-0.25 HybridF = AMKOR PhilippinesS = 0.18-0.22 HybridS = STATS ChipPACT = 0.18-0.15 HybridT = 0.18-0.15 Hybrid

#### Sylvie (EPC) will arrange to have the plastic taken off, so we can inspect





Next steps:

1 . Keep going Want to get figures for Total Dose too

2. Contingency preparation for moving the BIC away from radiation UA63/67





FIN





TE)



#### Principle for Test-bench "CIRX"







### Principle for Test-bench "CIRX"



TE)





(TE)



#### Principle for Test-bench "CIRX"











XC95144 x 32 XC95288XL x 32



### Testbench Electronic Functionality







XC95144 x 32 XC95288XL x 32





(TE)













ТЕ





TE)













TE)







### Testbench Electronic Functionality



TE)



## **Testbench Electronic Functionality**







## PIC LabVIEW



- 96-Channel Digital I/O Board used for detecting changes on:
  - Critical Path (3 Beam Permit signals)
  - Monitoring Part (CRCs, Glitch Counters, Versions....)
- Change detection on Inputs detected with events (no polling is used = less processor usage)
- Address lines (Outputs) change every 300 seconds
- Log-file written in case of inconsistency in the outputs of CPLD (XNORs)











- 96-Channel Digital I/O Board used for :
  - Scanning all 32 CPLS for frequency detection when all User\_Permits are TRUE
- Log-file is written in case of inconsistency in Beam\_Permit frecuency

iguration		Output lines								State Machine	
										Current State	
FAM DEDMIT OUT		LATCH_REARM	UP_13	UP_11	UP_9	UP_7	UP_5	UP_3	UP_1	SCAN ALL FOR BEAM	PERMIT FALSE
Longelanderson		LATCH_INIT						TMS	SOFT_RST	Current Board	
% PALI Side4/porce/imes										Board 2	
		•	۲	0	۲	۲		۲		Comment COM D	
OUTPUT PURTS		DEV_SEL_1	B_SEL_1	MODE						Current CPLD	
ATCH_INIT-REARM	BEAM_I-TDI									JCPLD 6	
PX11Slot4/port6/line0	PX11Slot4/port9/line1								-	REARM ALL	BEAM I Ton
JP_13	UP_14	•									
PXI1Slot4/port6/line1	PX11Slot4/port9/line2		BEAM_I	UP_14	UP_12	UP_10	UP_8	UP_6	UP_4	INIT ALL	•
JP_11	UP_12		IDI						ILK	A	
PXI1Slot4/port6/line2	PXI1Slot4/port9/line3									COST DECET ALL	
JP_9	UP_10		0	0	0					SUFT_RESET_ALL	
PXI1Slot4/port6/line3	PX11Slot4/port9/line4	UP_2	DEV_SEL_2	DEV_SEL_O	B_SEL_C	1					
JP_7	UP_8	HARD_RST								HARD_RESET_ALL	
PXI1Slot4/port6/line4	PX11Slot4/port9/line5									J 🔮	
JP_5	UP_6	Input lines									
PX11Slot4/port6/line5	PX11Slot4/port9/line6									יייין ר	
JP_3-TMS	UP_4-TCK							Frea. de	etected		
PXI1Slot4/port6/line6	PXI1Slot4/port9/line7				<b>O</b>			6			
JP_1-SOFT_RST	UP_2-HARD_RST			BEAM	1_PERMIT	_0UT			-		
PX11Slot4/port6/line7	PX11Slot4/port10/line0									-	
DEV_SEL_1	DEV_SEL_2									BP PASS	
PXI15lot4/port7/line0	PX11Slot4/port10/line1									A 0000	000
SEL_1	DEV_SEL_0	Frecuency BP	(Hz)								
PX115lot4/port7/line1	PX11Slot4/port10/line2	2									000
10DE	B_SEL_0									0000	0000
PXI15lot4/port7/line2	PX11Slot4/port10/line3									0000	000
		Results of last tes	ts								
PXI-6509 delay time	(ms)	BOARD	1	BOAR	D 2		BOARD 3		BOARD 4		
200			-	0			0				



#### Machine Interlock Systems



- TEY
- 3 'events' in MONITORING PART have been observed since re-start of CNGS with beam, NONE in the safety critical part
  - 15.August 2009 (03:12:08.0289 ) According to Logbook & TIMBER with beam in CNGS (2E13)
  - 16.August 2009 (15:33:13.7339) According to Logbook & TIMBER with beam in CNGS (2E13)
  - 16.August 2009 (18:35:46.0737) According to Logbook WITHOUT beam in CNGS (since 20 minutes)
- Events seen more likely to be due to EMC problems (longer cables, especially the 5m flat cable in CNGS using TTL, shielding issues of NE48 as observed by PO)?
- Will continue to improve SW and exclude problem sources to have clarity (maybe small intervention in tunnel during next shut-down)



Machine Interlock Systems

31 of 27

#### benjamin.todd@cern.ch 🖂



- Have seen constant events in the log-file since 15:00 on day of installation
- False Beam Dumps
- Missed Beam Dumps
- Periods without beam in SPS = no errors...

	5	5 G 1 1					ation	Output lin	es		
1 1	5:00	Lou	is, Rene		E	c	📮 Copy (2) of TEST - Notepad	1.			
2 1	6:01	3 No	beam, transmitter	3 tripped, afte	r reset ok	r.	File Edit Format View Help				
3 1	6:05	Bea	m back beam		e	c	19/08/2009 16:11 3 19/08/2009 16:14 0 19/08/2009 16:14 1 19/08/2009 16:14 3	5 2 4 5	FAILED FAILED FAILED FAILED	INIT ALL REQUIRED SOFT RESET REQUIRED SOFT RESET REQUIRED SOFT RESET REQUIRED	BEAM PERMIT TC BEAM PERMIT TC BEAM PERMIT TC BEAM PERMIT TC
. 5 1	6:57	Bea	m back beam		с сл	c cr	19/08/2009 16:16 2 19/08/2009 16:16 2 19/08/2009 16:16 3 19/08/2009 16:16 3	0 1 0 5	FAILED FAILED FAILED	SOFT RESET REQUIRED SOFT RESET REQUIRED SOFT RESET REQUIRED SOFT RESET REQUIRED	BEAM PERMIT TC BEAM PERMIT TC BEAM PERMIT TC BEAM PERMIT TC
6 1 7 1	7:092 7:11	2 2 <sup>no</sup> Bea	m back		ء در	ca.	19/08/2009 16:19 3 19/08/2009 16:19 3 19/08/2009 16:21 2 19/08/2009 16:24 0		FAILED FAILED FAILED	SOFT RESET REQUIRED SOFT RESET REQUIRED SOFT RESET REQUIRED SOFT RESET REQUIRED	BEAM PERMIT TC BEAM PERMIT TC BEAM PERMIT TC BEAM PERMIT TC
			e mand and a second	Faul	ts		119/08/2009 16:46 AL		PASS	NO ACTION REQUIRED	SCAN_ALL_FOR_E
#Gro	oup F	ault	Element	Description	Begin		19/08/2009 16:48 AL	L ALL	PASS	NO ACTION REQUIRED	SCAN_ALL_FOR_E
1 CI	PS L	INAC2	Linac Intervention	20020	19/08/2009 16:23:09		19/08/2009 17:07 0 19/08/2009 17:07 0 19/08/2009 17:09 2	7 5	PASS	REARM REQUIRED SCAN	_ALL_FOR_BP_TRUE _ALL_FOR_BP_TRUE
. <mark>2</mark> B	T Ki	ickers	MKD status		19/08/2009 17:09:54		19/08/2009 17:09 3	1	PASS	INIT REQUIRED SCAN	_ALL_FOR_BP_TRUE
3 R	F,	RF	TRX3	1.1.1.1.1.1.	19/08/2009		<u></u>				
					Sucal intranet						

- Software will be further optimised to get rates/ratios





TEY

TE/MPE/MI take the radiation issue seriously

Dedicated testbench designed

Considerable effort

1. We need some time in the next access window to check our equipment

2. XC9500XL = one event every 3 minutes (this is in a BIC VME Chassis)

3. XC9500 = one event every 2 days (this is in a PIC and User Interface Chassis)

4. Enhance software

5. Establish rates and ratios





#### **CIBU** : User Interface Locations

IR1	IR2	IR3	IR4	IR5	IR6	IR7	IR8	other
SR1	SR2	SR3	SR4	SR5	SR6	SR7	UA83	CCR
US151	UA23	UJ33	UA43	UJ56	UA63	UJ76	UA87	
USA151	UA27		UA47	USC55	UA67	TZ76	UX85	
USA152			SX4	RR53	US65	RR73	US851	
RR13			CR4	RR57	US651	RR77		
RR17			US451					
UJ14								
UJ16							"criti	cal areas"
BIC :	Beam Int	erlock <b>C</b> o	ntroller Lo	ocations				
IR1	IR2	IR3	IR4	IR5	IR6	IR7	IR8	other
US15	SR2	SR3	UA43	UJ56	UA63	SR7	SR8	CCC
	UA23	UJ33	UA47	UCS55	UA67	TZ76	UA83	
	UA27						UA87	





FIN





- 4x8 = 32 CPLDs on dedicated CIRP boards installed
- Identical SW as used in the LHC devices, with dedicated remote monitoring/readout facility (RS485 line drivers and PXI chassis in control room)
- LabView program will change every 300s address lines and input states of the CPLD (throughout all possibilities as used in LHC)
- Setup is constantly comparing against each other the outputs of all 32 CPLDs and will detect and log any output change (along with the current input settings)
- Readout of critical path (Beam Permits) separated from Monitoring part







particles pass through consecutive boards

K. Rooed simulations show 20-30% error in fluence due to this