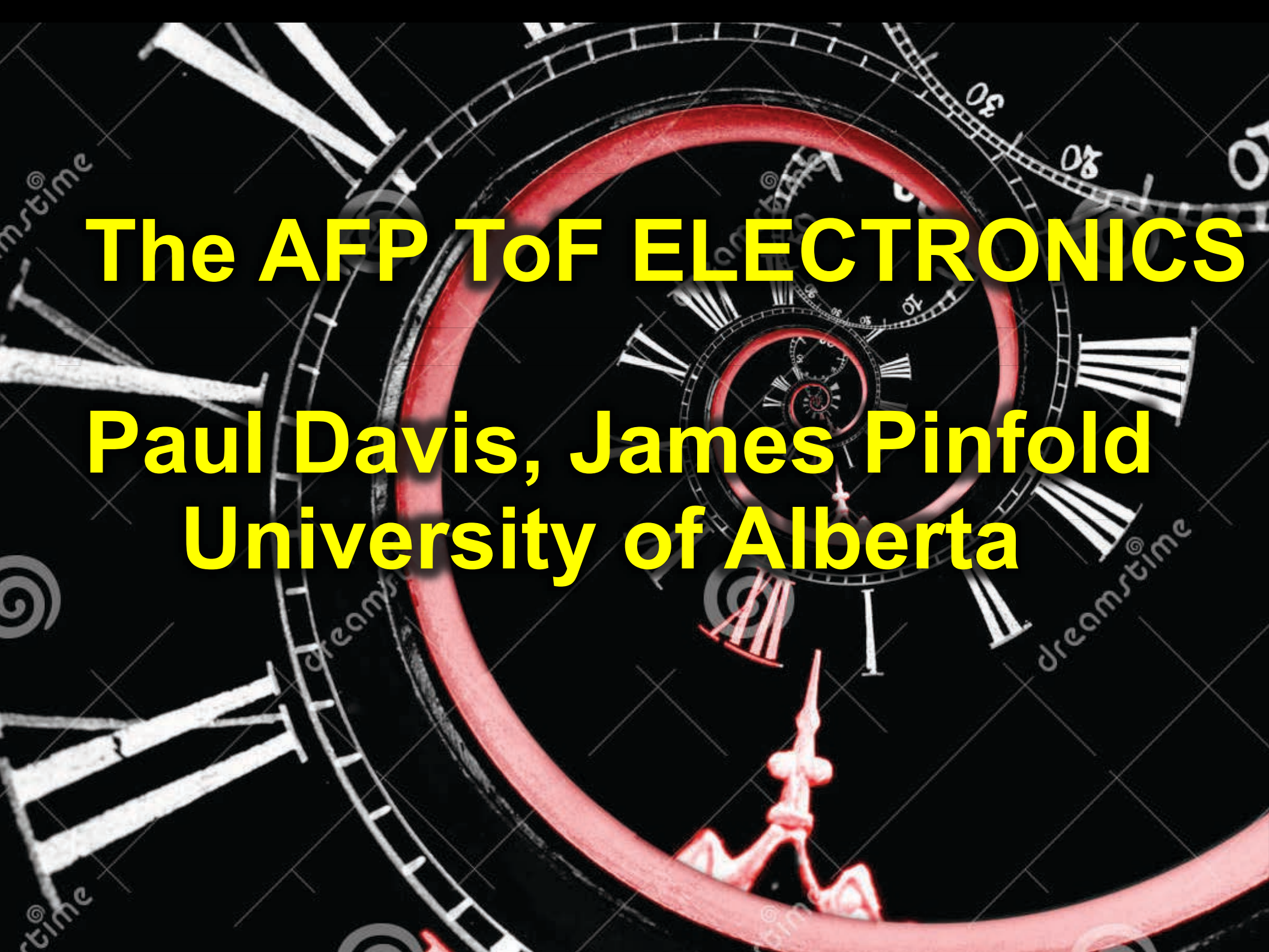
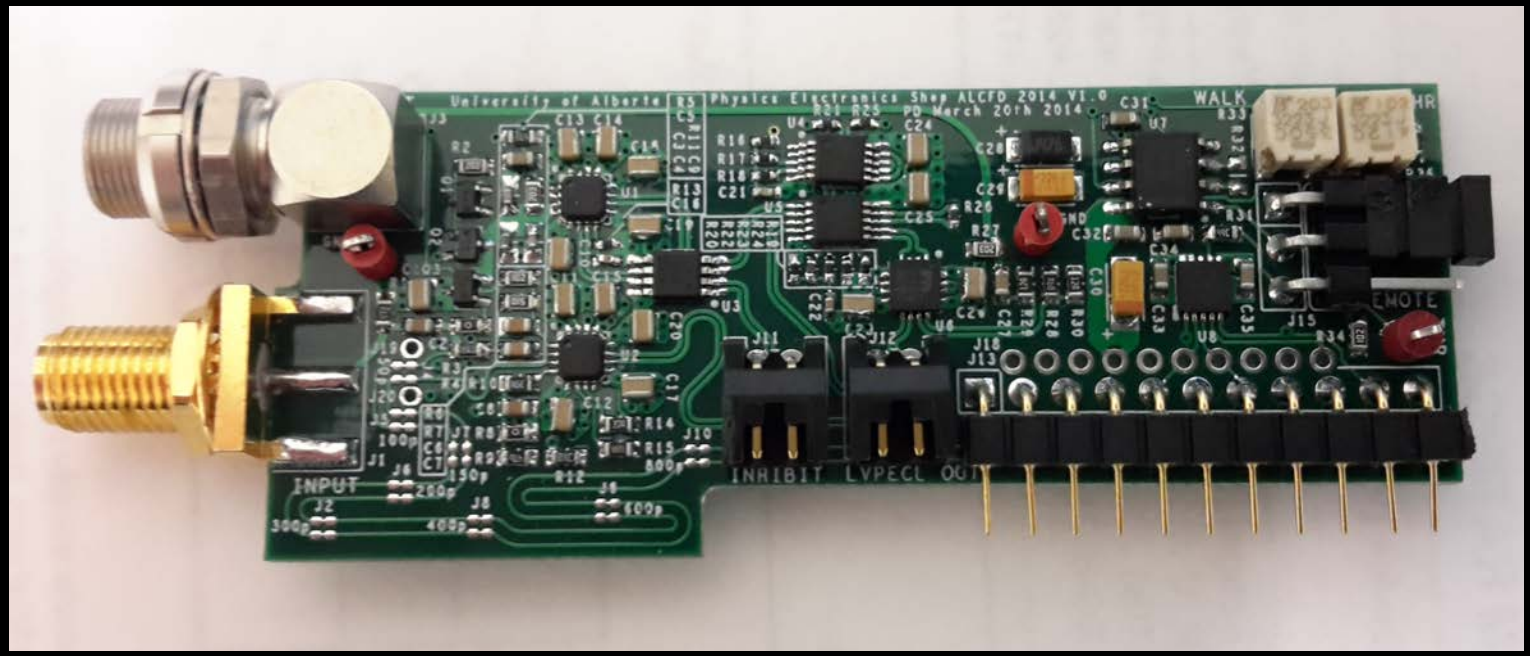


The AFP ToF ELECTRONICS

Paul Davis, James Pinfold
University of Alberta

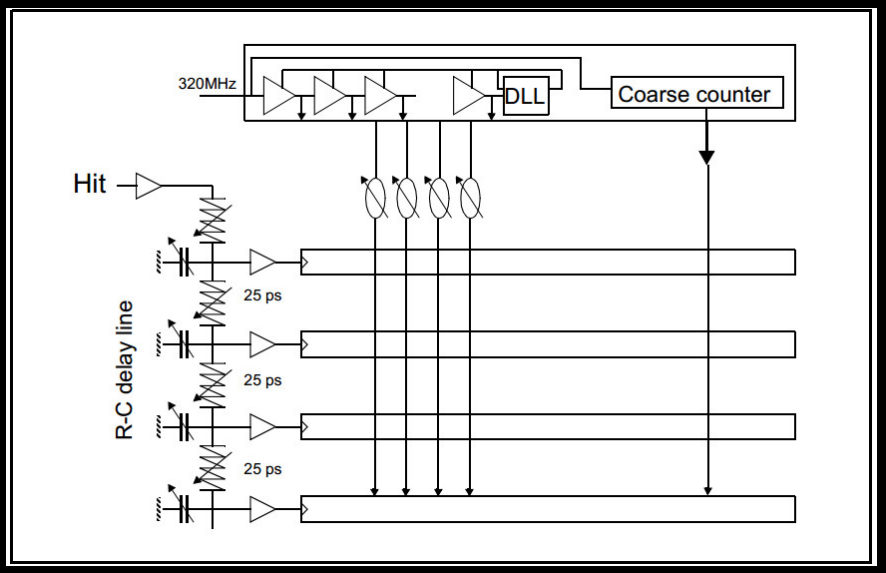
Constant Fraction Discriminators (CFDs)

CFDs worked well during 2017 running except for a few infant failures the cause of which still need to be investigated. Threshold can be set remotely. Time walk ~3psrms



AFP HPTDC

- *12 channels with 25ps binning and ~15ps resolution*
- *I^2C output controls CFD thresholds and trigger board settings and can read out monitoring information*
- *Calibration muxes allow alternate signals to be injected into the hit inputs for test and calibration purposes*
- *Trigger output formed from coincidence of hit signals (4ns window)*



High Performance Time to Digital Converter Manual
Version 2.2, March 2004, pg8. Jorgen Christiansen

Current TDC upgrade (1)

- *Current TDC FPGA chip has SEUs in configuration RAM at a much higher frequency than expected.*
- *Originally planned mitigation, reset on SEU, would cause too much ATLAS busy. Current mitigation has potential for undetected errors.*
- *FPGA is being changed to a more radiation tolerant version.*
  - *Final part has not yet been determined but will either be the same technology with config scrubbing, flash based, or antifuse (no possibility of firmware update)*

Current TDC upgrade (2)

- *Add extra general purpose inputs/outputs for trigger muxing/ Test beam use*
- *Add output for PMT calibration LED*
- *Rerouting signals and redesign of output driver for reduced trigger latency.*
- *Improved power supply noise (improved snubber)*
- *Firmware changes for extra trigger information in data stream*
- *Firmware for combining spare channels for better resolution*

PicoTDC upgrade

- *A 64 channel <3ps rms TDC chip is being developed at CERN by Moriz Horstmann and Jorgen Christiansen.*
  - *Development is delayed. The chip should be available in 2018.*
  - *We hope to test the new chip during a 2018 test beam with installation in the last technical stop or EYETS depending on availability.*
- *PicoTDC uses a similar scheme for timing as current TDC but uses higher clock speed and resistive interpolation of the DLL instead of channel interpolation*

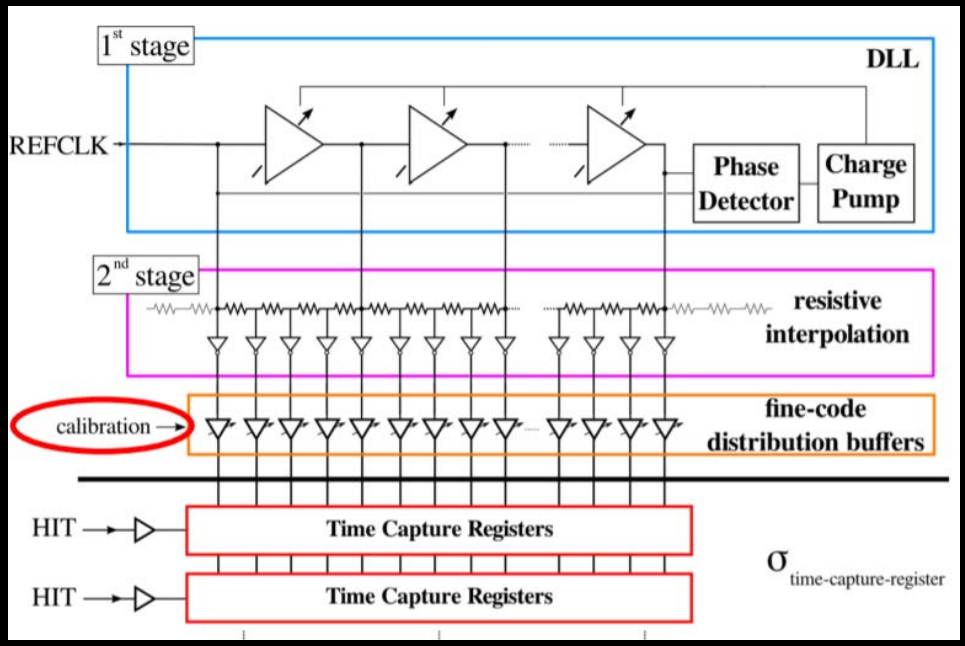


Image from picoTDC: Pico-second TDC for HEP, Jorgen Christiansen, Morit Horstmann, Lukas Perktold, Jeffery Prinzie, 2005