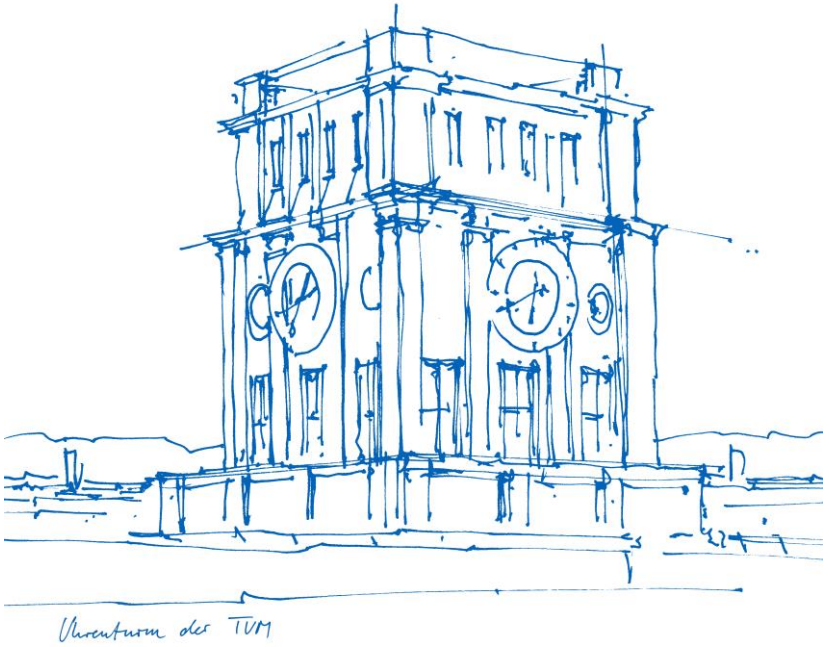
Summary of DAQFEET Workshop

Igor Konorov on behalf of DAFEET participants

COMPASS TB Meeting

CERN Geneva December 4-th

https://indico.cern.ch/event/673073/



Introduction to DAQFEET 2020 WS

Important phase of COMPASS experiment :

- 2018 is last year of COMPASS 2 data taking
- Next possible run in 2021 right after LS2
- Collaboration is working on physics program BEYOND 2020
- 2 years without data taking in a view of physics program after 2020
- Very exciting opportunity to start to build next generation read out system

Workshop goal:

- Learn about future physics programs and requirements for read out electronics
- Review existing read out and trigger system
- Look at the developments carried out within COMPASS
- Learn about developments done for future experiments

- Define needs and strategy for further development
- Identify interested groups within collaboration to participate in this R&D
- Distribute tasks

Modern ASICs

- Damien : SACLAY SEDI Microelectronics group
  ASICs for MPGD, ASICs for solid detectors, High Speed serial links
- Giulio Dellacasa, Gianni Mazza : Torino ASIC lab
  TDC, SDD, SEED, High Speed serial links
- Christian Lippmann:
  SAMPA ASIC for ALICE TPC
- Moritz Horstmann : CERN
  Pico TDC

Many ASICs feature trigger less read out, high speed serial link data transmission, internal digitization.

Trigger less read out solution exists for every detector type.

Conditions for future programs

Additional questions: trigger latency?
Hardware (FPGA) or software trigger?
Earliest possible realization?

(*) or list of detectors to be included in trigger logic

Program	Type / set of detectors baseline: COMPASS w/o RICH1	Beam energy [GeV]	Rate on target [sec^{-1}]	Trigger rate (est.) [kHz]	Trigger signature (*)	Trigger challenge factor
d-quark Transversity	RICH1	160	3×10^6	25	As 2010: IT, MT, LT, OT, CT, LAST	
Proton radius	active hydrogen target, silicon (2+1) or SciFi (2+2) telescopes	100	4×10^6	<= 100	~~beam trigger?~~ scattered-muon trigger? (recoil-proton trigger?)	
GPD E	recoil detector around transpol polarized target	160	10^7	10	MT, LT, OT, LAST. If higher beam intensity: photon or proton trigger?	
Drell-Yan conventional	vertex detector	190	$0.2\text{-}6.8 \times 10^7$	25	As 2015: MT+LAST, OT +LAST, LAST 2mu	
Drell-Yan RF-separated	vertex detector, larger tracking detectors?	~100	10^8	25-50	As above + ? new hodoscopes for SAS-SAS trigger	
Primakoff RF-separated	RICH1	~100		>> 10	ECal2 ΔE>threshold	
Prompt photon prod.		>= 100	5×10^6	10-100	ECal0, ECal1 ΔE>threshold, or "true pT" trigger	
Anti-matter x-section	RICH1 (RICH0?)	50 100 190,..	5×10^5	25	As 2012 Primakoff: (a)BT, VI, ΔECals>threshold	
Spectroscopy anti-p	target spectrometer: tracking & calorimetry, RICH (RICH0?)	12 20			CEDARs?	

Proton Radius Measurements

Active Target

- pressurized hydrogen TPC
- readout plane perpendicular to beam
  - with inactive area for beam
- $\mathcal{O}(20)$ μs drift time
- $\mathcal{O}(10-100)$ channels

trigger on ionization signal in TPC

- for low Q^2 (smaller than $10^{-3}\,\mathrm{GeV}^2/c^2$)
  - recoil protons are immediately stopped
  - no trigger within inactive area
- simpler for higher Q^2
  - protons can travel a significant path
- long latency for trigger decision
- not compatible with (at least) APV frontends

The Baseline

- current spectrometer set-up
- no modifications to frontends or DAQ
- beam intensity of $2 \cdot 10^5\ \mu/s$
- beam trigger rate $1 \cdot 10^5\ \mu/s$ ($\times \frac{1}{2}$ by veto detectors)

- measurement with current COMPASS set-up is possible
- trigger on protons
  - for low Q^2 not compatible with current FEE
  - for high Q^2 rather "simple"
- trigger on muons
  - suppress non-interacting beam for reasonable trigger rate
  - but: can we trust in the simulations to understand systematics

Kink Trigger

- dual read-out of silicon planes possible (APV and ???)
- integrated chip available?
- novel trigger logic (for COMPASS) to be developed
- use scintillating fibers instead of silicons for triggering
  - available with 200 μm width off the shelf
  - all lengths scaled by factor $\times 4$
  - in the end similar amount of work required to develop FEE (for fewer channels)

preliminary simulations (for silicon option)

- elastic scattering events
  - 94 % acceptance at $Q^2 = 10^{-4}\,\mathrm{GeV}^2/c^2$
  - stable > 98 % acceptance for $Q^2 > 10^{-3}\,\mathrm{GeV}^2/c^2$
- completely removes events without interaction in target

Proton Radius Measurement

TPC issues

- TPC read out shall be trigger less due to long drift time
- No inactive area because of u-beam size
- How to associate recoil proton with muon, is phase space sufficient ?

TRIGGER LOGIC

Summary of the current Trigger System:

- Muon Trigger:
  based on target pointing / energy loss
  760 channels for PMTs
  276 channels for Meantimer
  9 Matrix Boards (7 Bonn-Matrix / 2 FPGA)
- Veto System:
  62 channels for PMTs
  18 channels for Meantimer
- CALO System:
  based on energy threshold in HCAL cells
  208 4x4 Sums for two thresholds (HCAL1)
  80 4x4 Sums for two thresholds (HCAL2)

In total: 1404 TDC channels in use with 9 matrix boards

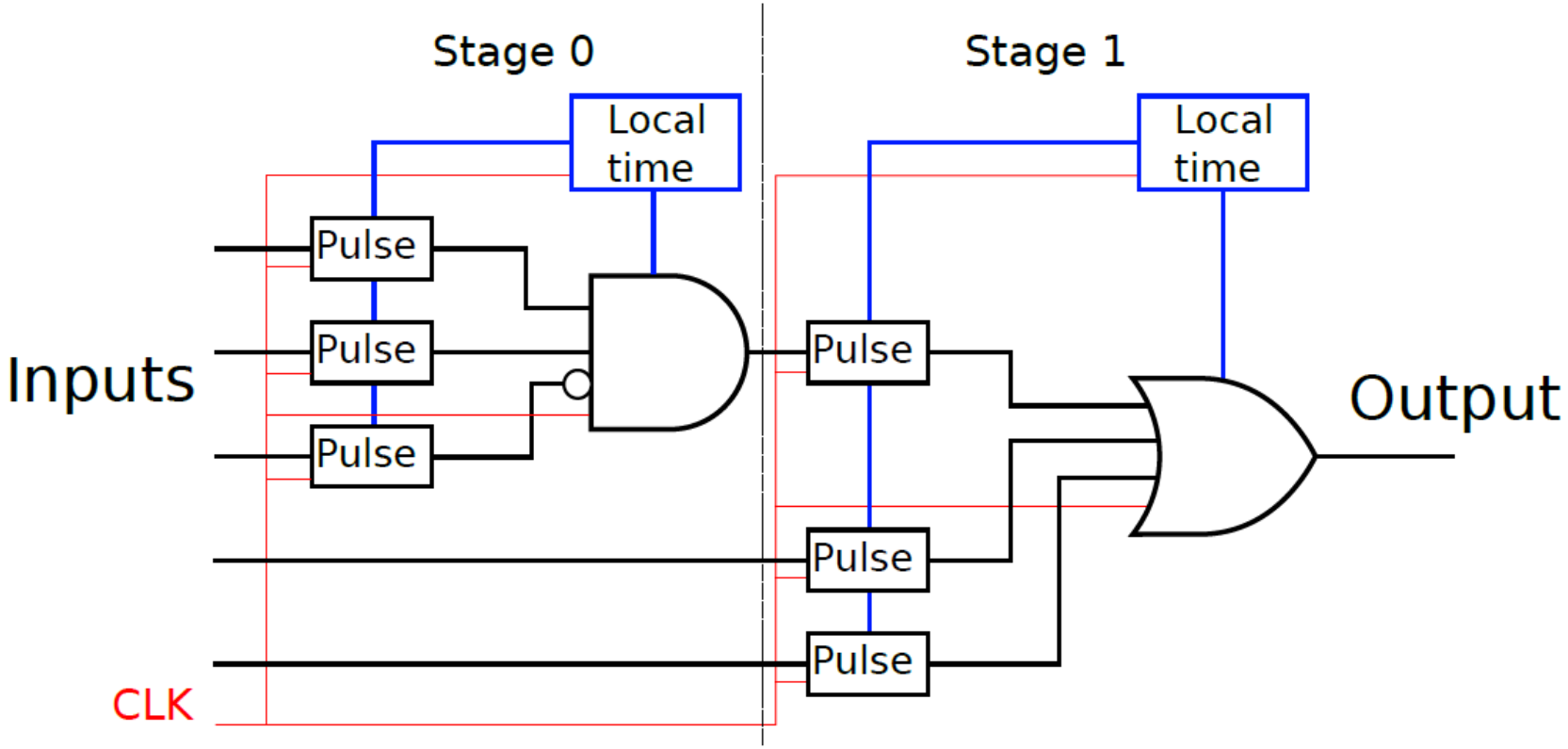
Main Trigger Logic Element is Analogue(in time) coincidence
Employs NIM logic
Limited Flexibility

New Trigger Logic Developments

FPGA-based Digital Trigger Logic

- Was developed in 2010-2011 as a student project for evaluation of the FPGA-based trigger architecture with integrated TDC
  - Project stopped at the simulation stage
- Cores to process hits in pipeline
  - Local time processing
  - Pulse processing
  - Coincidence/Anti-coincidence (logic AND), aggregation (logic OR)
- Configuration of the trigger logic layout out of the available cores independent of implementation
- Software for automatic generation of VHDL code from the configuration file
- Requirement:
  - all hits are assigned a timestamp using the global time
  - Hit time format:
    - Coarse time: timestamp from the global time
    - Fine time: sub-system clock resolution from the measurement

Trigger Logic Layout



Configuration of the Trigger Logic Layout

- Trigger logic model with high-level primitives
- Define trigger logic layout
  - logic blocks
  - processing stages
  - channel alignments
  - gate lengths
- Write XML file with the description of the trigger logic

Read Out Electronics

Micro pattern detectors
- Silicon Detectors
- GEM, PGEM, PMM

APV25

Scintillating Detectors
- SciFi, BMS, Hodoscopes — **F1**
- CAMERA — **GANDALF**

Wire Chambers
- DC, Straw, W45
- MWPC, RW, MW1, MW2

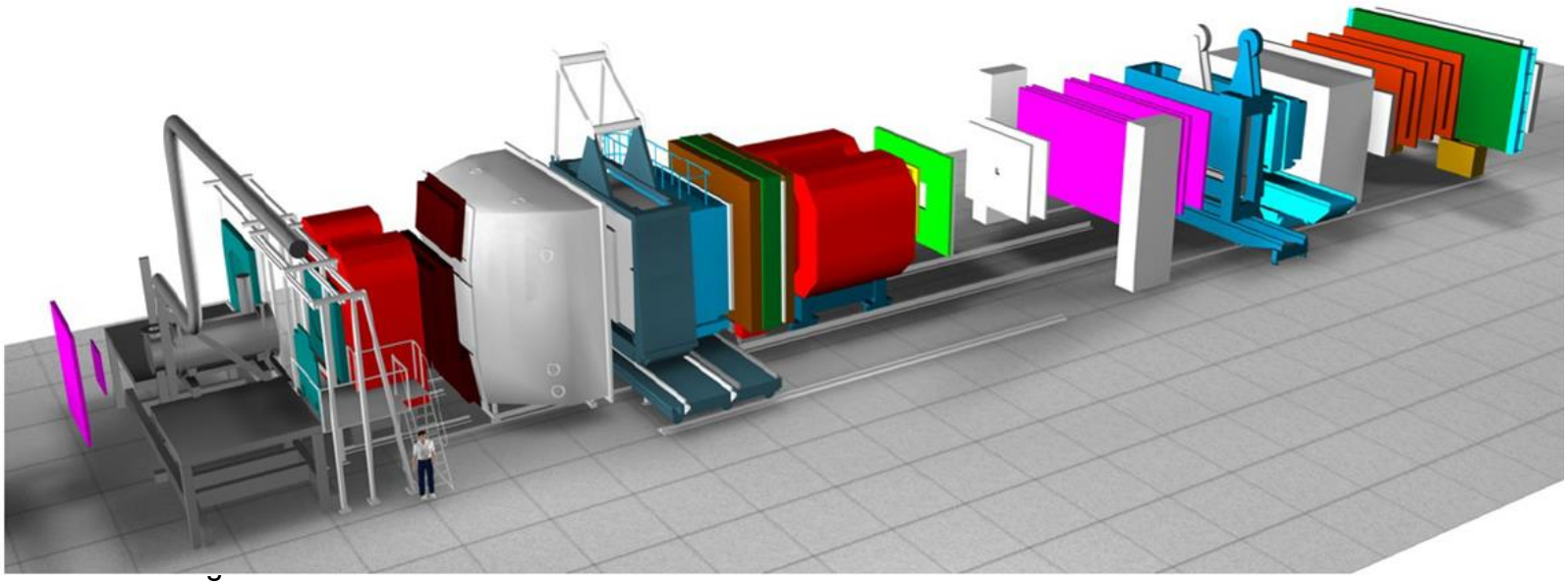
F1

- DC05 — **FPGA TDC**

Calorimeters
- HCAL1,2
- ECAL0,1,2

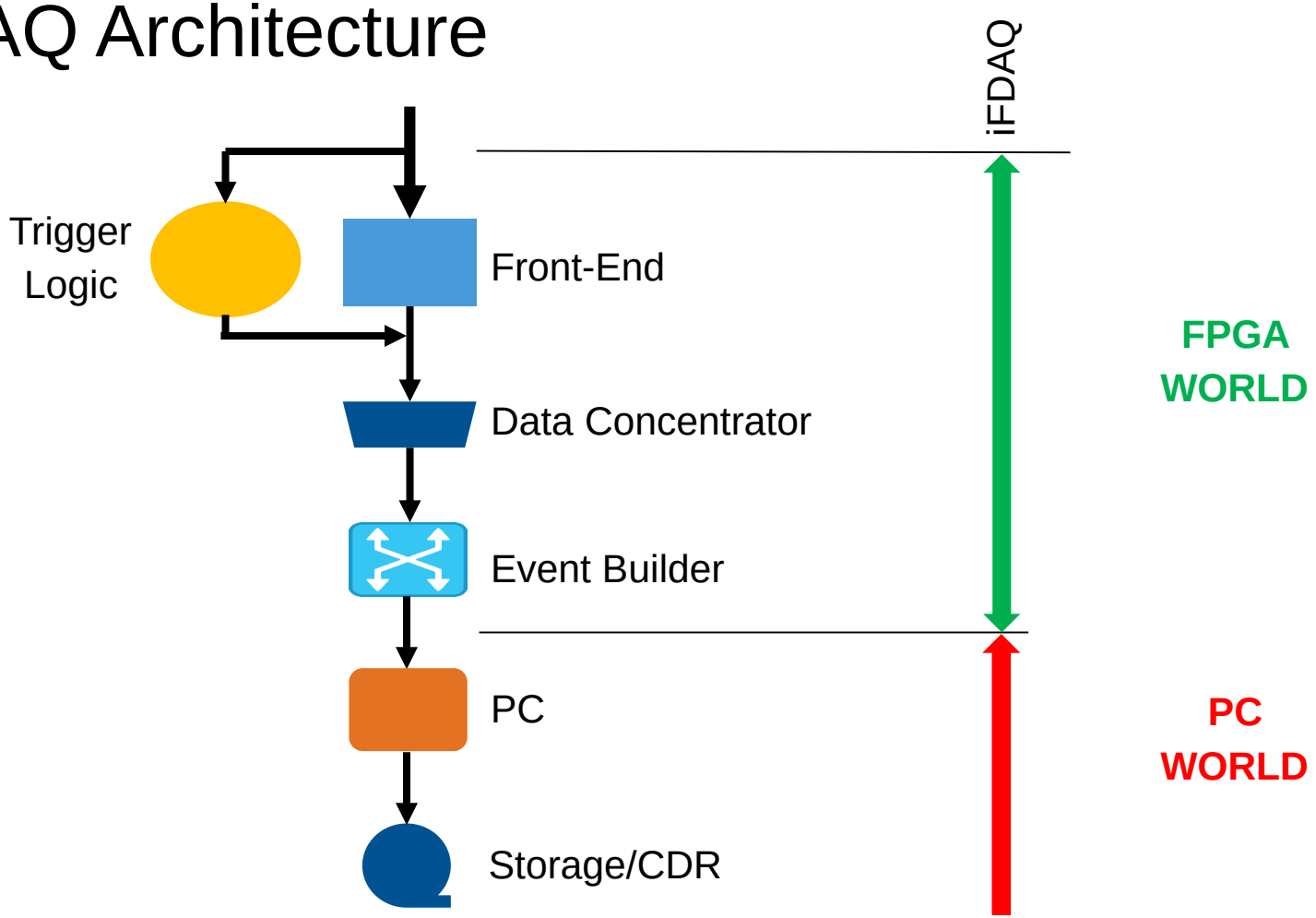
MSADC

RICH
- MAPMT — **F1**
- MWPC, THGEM — **APV25**



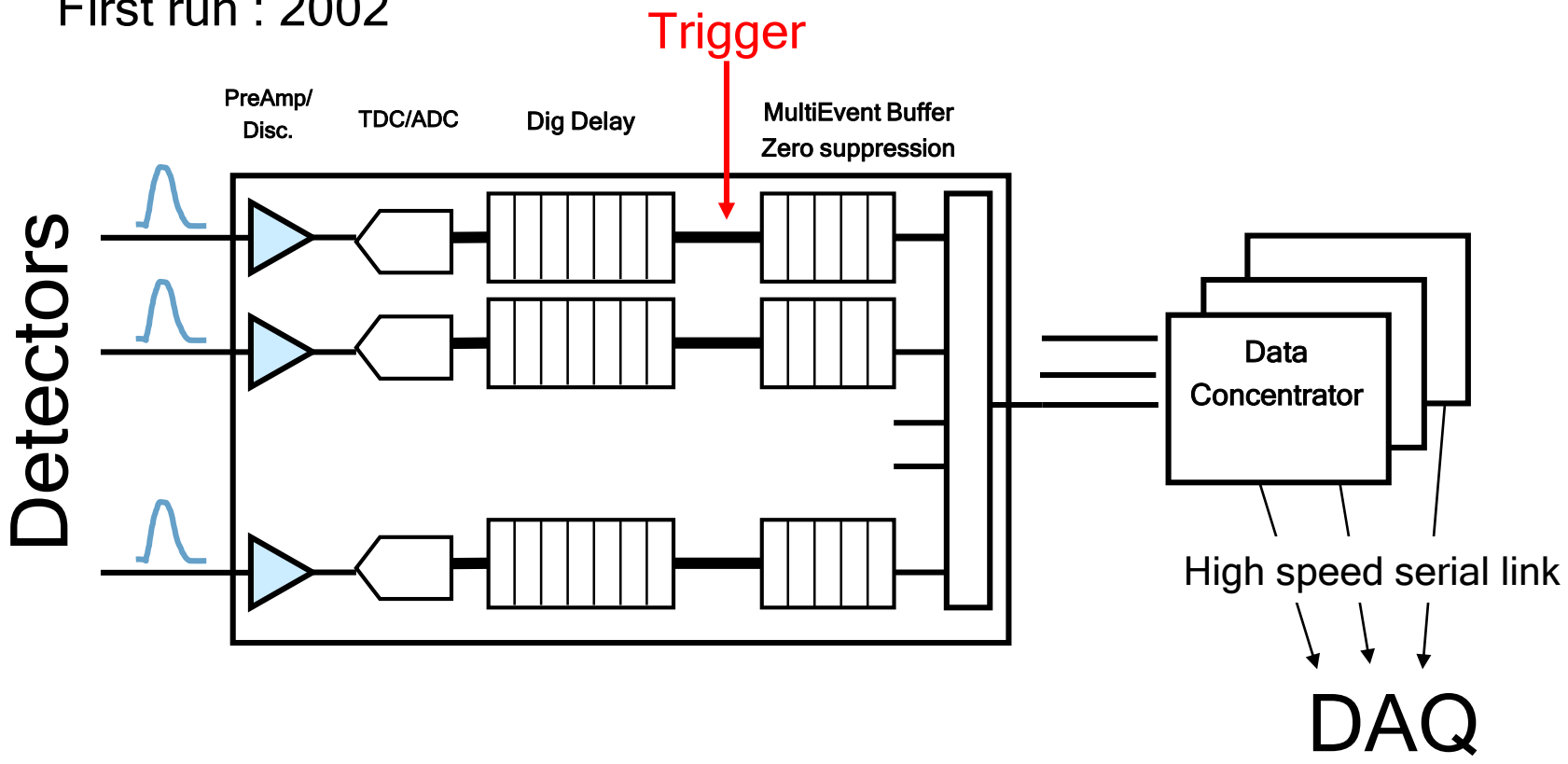
COMP

DAQ Architecture



Pipe-Line Read out Architecture

First run : 2002



FEE Performance :

Trigger rate	aimed :100kHz	real : 40kHz
Dead time	0 %	10-20%

Limits of Current Read Out System

F1 TDC

- Trigger latency limited by size of derandomization buffer and depends on hit rate - 3us
- Trigger rate depends on detector occupancy, reliable conditions 40-50kHz

MWPC

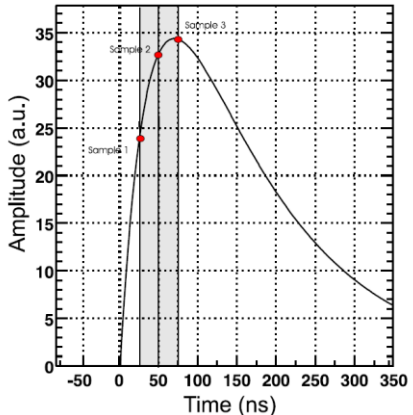
- Cross talk in time : data transmission induces noise in following trigger
- Minimum time interval between triggers 4us

APV25 : Silicon, Gem, PGEM, PMM, RICH

- 4 us maximum trigger latency
- Trigger rate 40kHz@20MHz readout, 90kHz@40MHz readout
- Silicon and GEM detectors are running with 20MHz read out
- Data rate limit : @40kHz average occupancy <= 10%

Possible improvements :

- firmware upgrade to 40MHz read out => 90kHz trigger rate
- Read one sample instead of 3 samples => 200 kHz trigger rate



Limits of Current Read Out System

HCAL1, HCAL2, ECAL1 – SADC 10bit 80MSPS

- Highly inefficient zero suppression algorithm
- One channel provides 32 samples or 44 bytes of data
- Trigger latency 5us
- Maximum trigger rate limited by interface bandwidth of 20MB/s/32 channels
- 100 kHz @10% occupancy

ECAL0, ECAL2 – MSADC 12bit 80MSPS

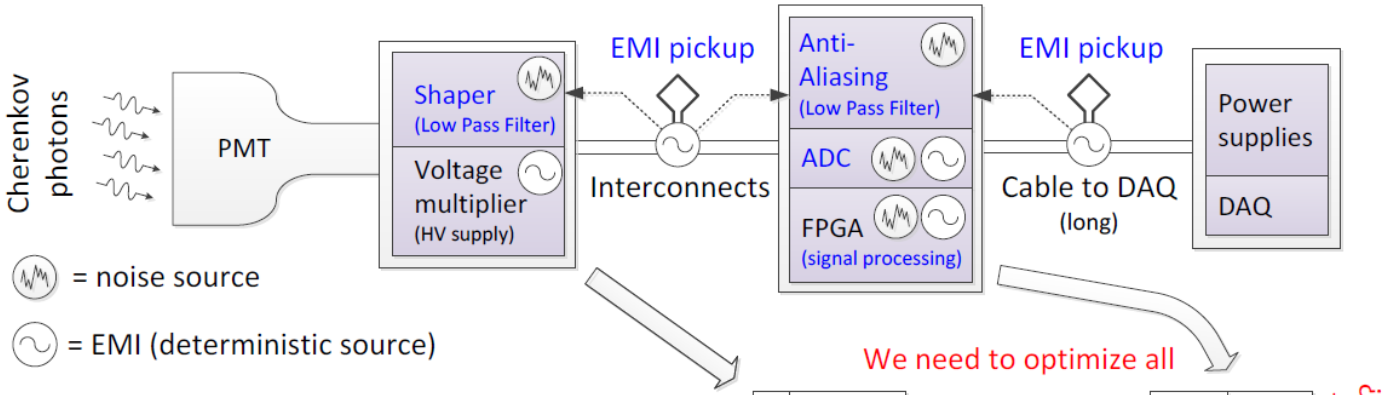
- One channel provides 32 samples or 68 bytes of data
- Trigger latency 5 us
- Maximum trigger rate limited by interface bandwidth of 20MB/s/64 channels
- 45 kHz @10% occupancy

Possible improvements :

- feature extraction algorithm to extract Amplitude and Time => 4 Bytes/channel

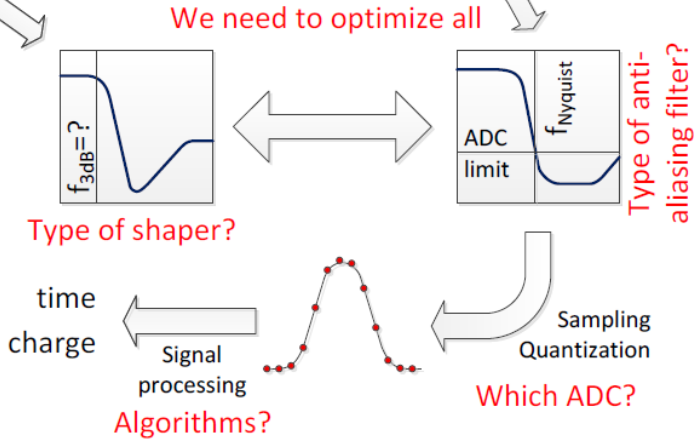
Marcin : Data Filtering for Calorimeter

Signal Chain (Water Cherenkov Detector)



CRITICAL DESIGN CHOICES:

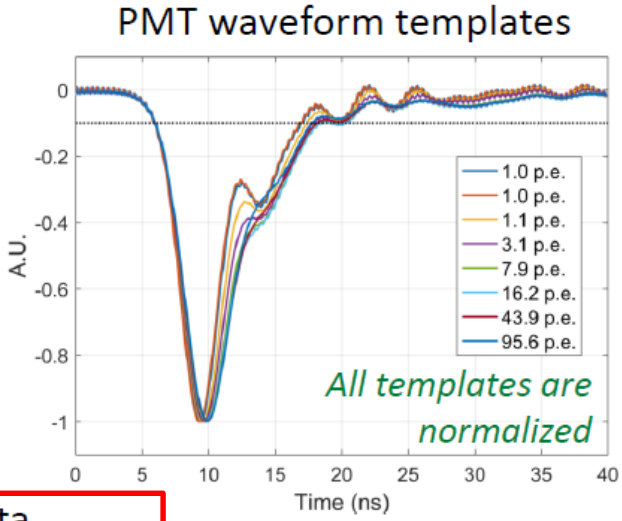
- Type of shaping filter:
  - Limited by what is possible to implement in hardware, as an analog low-pass filter
- ADC parameters:
  - Speed, precision → actual SNR achievable by the ADC
- Signal processing
  - Different processing for time and charge estimation



Sharing of signal processing between DAQ and FPGA?

Summary

- Investigated digital constant fraction algorithm
  - Simple & effective, but requires good SNR
- FIR filters:
  - Implemented, optimized and tested Digital Penalized Least Mean Squares (DPLMS) method for synthesizing FIR filters (by Gatti E., et.al.).
  - Implemented pulse timing by finding maximum response of matched filter.
  - Investigated optimal parameters for FIR DPLMS method using MATLAB optimizers.



- Developed models, got relatively good match to data.
  - Good match for digital constant fraction discriminator at SNR $\geq$ 20 dB.
  - Good match for FIRs over whole SNR range
- Still to do:
  - Try FIR synthesis using CDMF method (Constrained Digital Matched Filter) – authors claim it may be better than DPLMS.
  - Check charge resolution.
  - Try different filters for shaping (in simulation). It is believed that tested shapers were sub-optimal shaping (too slow).
  - Check how FIR behaves if pulse shape changes (as is the case with PMT and single- and multi-p.e. pulses – see picture with normalized PMT waveform templates).
  - Investigate behavior in case of overlapping pulses.
  - Try combining ADC & TDC data (check if better timing is possible at low SNR)

A comparative discussion of bus/crate standards and their use at CERN

Markus Joos

CERN

Putting it all together - 1

So, what is the right standard for your project?

This obviously depends on your requirements:

- Power & cooling
- Bandwidth & latency
- Availability of commercial products
- Existing infrastructure (S/W and H/W) and expertise in your collaboration
- Start and duration of the project
- Scalability requirements
- Reliability and availability requirements

- CERN has a large legacy of VMEbus and, to a lesser extent, of other crate and systems standards
  - Much of this equipment will be around for at least another ~10 years
  - Engineers will be needed to keep these systems alive and to plan the migration to newer technologies
  - "Old" technologies will not be excluded for "new" projects if they fit
- xTCA will play an important role in the future (accelerator and experiments)

New Developments

DAQ Upgrade

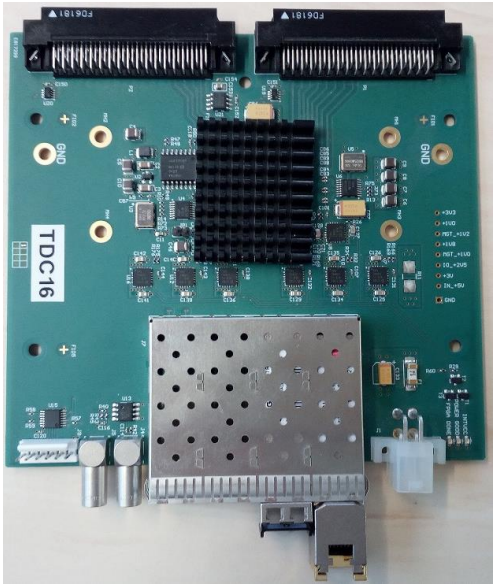
- IPBUS interface developed for CMS
  - UDP based protocol
  - Direct Ethernet connection to FPGA to access internal registers , memories
- Software development
  - Dialog library
  - DAQ Debugger
  - Command line interface
  - Event size monitor

FPGA TDC - iFTDC

iFTDC

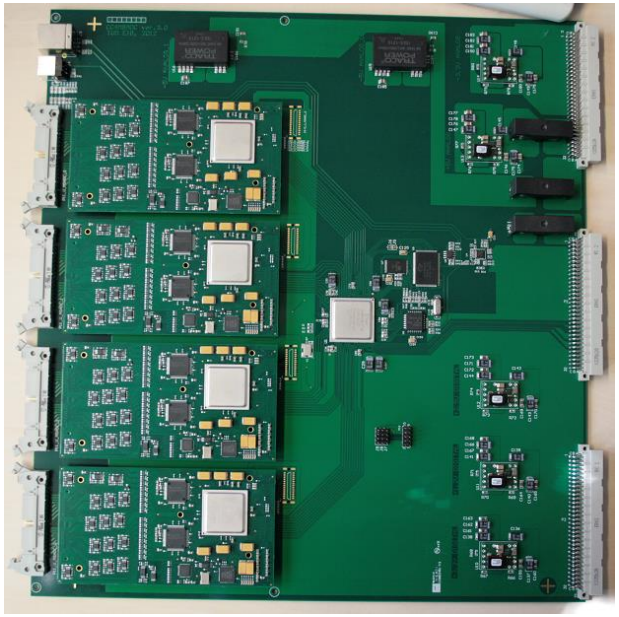
Features

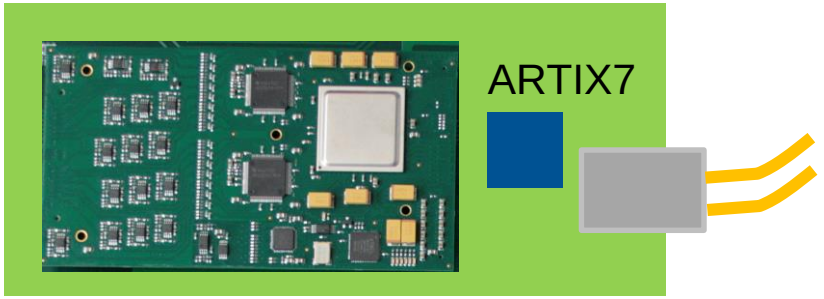
- ARTIX7 FPGA
- 64 TDC channels
- **Bin size : 1 ns, 0.6 ns, 0.3 ns (32 channels)**
- **Time resolution : 300ps, 200 ps, 100 ps**
- PCB exists for MWPC, DC00-DC04
- One TDC card was installed on MWPC and was successfully in the last week of 2017 run
- It's planned to use 4xTDCs(128 channels)
- for CEDAR in 2018



- **Trigger less capable data flow**

Trigger Less MSADC





Summary I

Limitations of present readout system :

- 3us trigger latency, 40 kHz trigger rate

Possible improvements :

- upgrade of Silicon and GEM firmware to 40 MHz => 90 kHz trigger rate
- Change 3 sample read out to one sample => 200 kHz trigger rate
- Implement feature extraction algorithm in SADC and MSADC to over come bandwidth limits

But

- COMPASS electronics will be 20 years old in 2021
- We can’t expect that it will run stably for next decade (bad HotLink connections, limited spares)
- There are not many spares of NIM and VME crates

If we want to work after 2021 for few more years we should develop new electronics

Strategy for New Developments

FEE requirements :

- Trigger less capability : FEE can run in triggered and not triggered mode
  - Trigger less capability does not give a big cost overhead if any
- Data of any detector can be used for triggering
- FEE Interface based on Serial links with UCF protocol instead of SLink
- IPBUS for slow control and monitoring => no VME CPU

Trigger Logic Requirements

- Move logic to Digital Trigger Processor
- Complete development of configurable digital trigger logic
- Use UCF protocol for data transmission
- IPBUS for configuration and monitoring

$\Rightarrow$ Common hardware between DAQ and Trigger Logic

System shall foresee online data processing

The FEE electronics can be used as replacement of existing FEE

Trigger less Data rate estimation (preliminary)

COMPASS event size : 30kBytes
With assumption that one event covers 0.5us time interval => 60GB/s

Possible data reduction at FE :

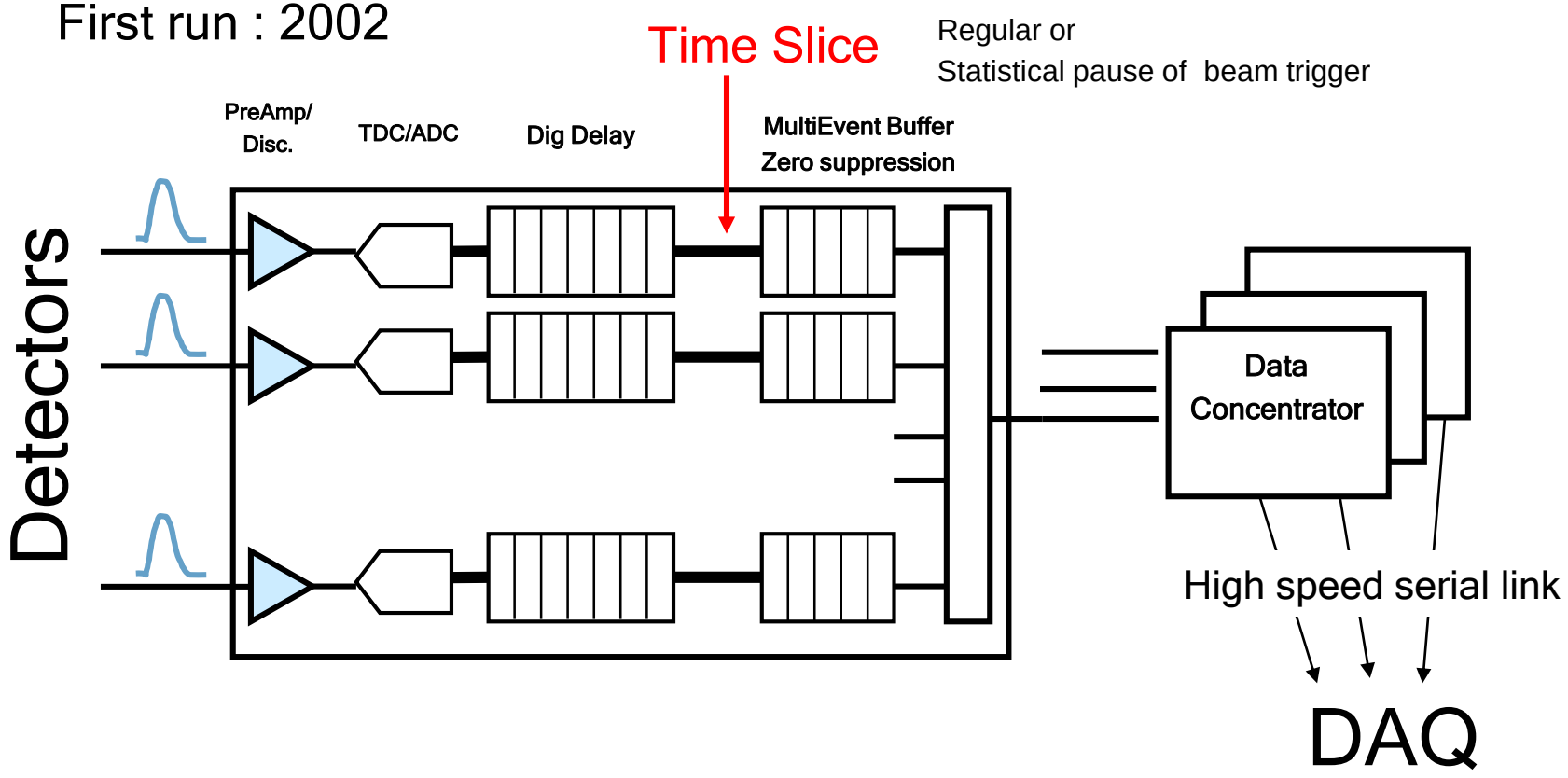
- Calorimeter :
  - Substitute 32x12 samples by Time and Amplitude => 32 bit word. Reduction factor 16.
  - More efficient zero suppression algorithm. Additional factor 2
- TDC :
  - More efficient data encoding => factor 2

Reduced event size 5kBytes => 10GB/s within spill or 5GB/s sustained

CDR is capable to store more than 1 GB/s => missing factor 5.

Trigger Less Read out Architecture

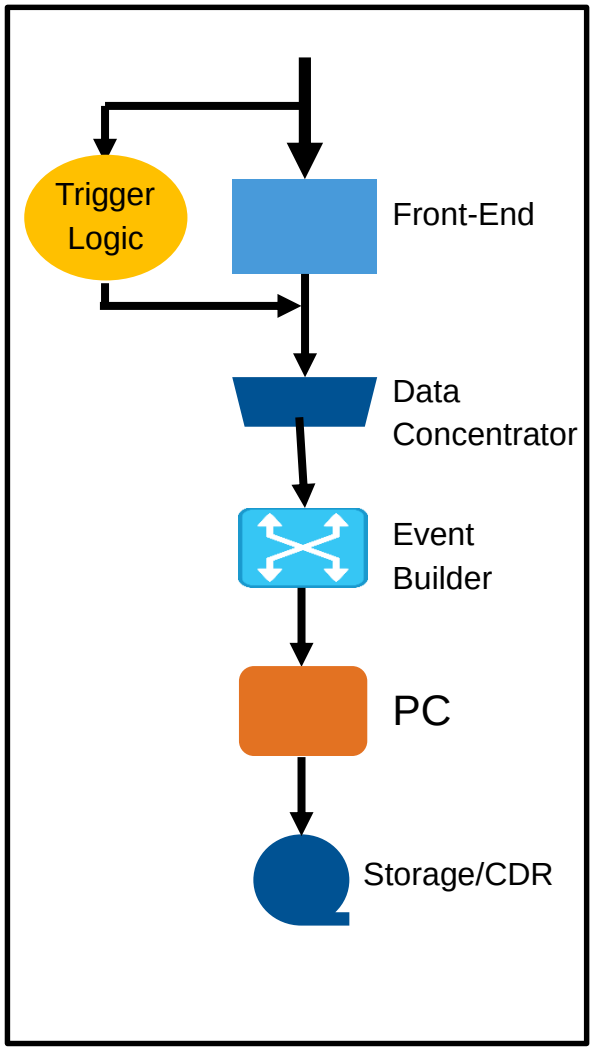
First run : 2002

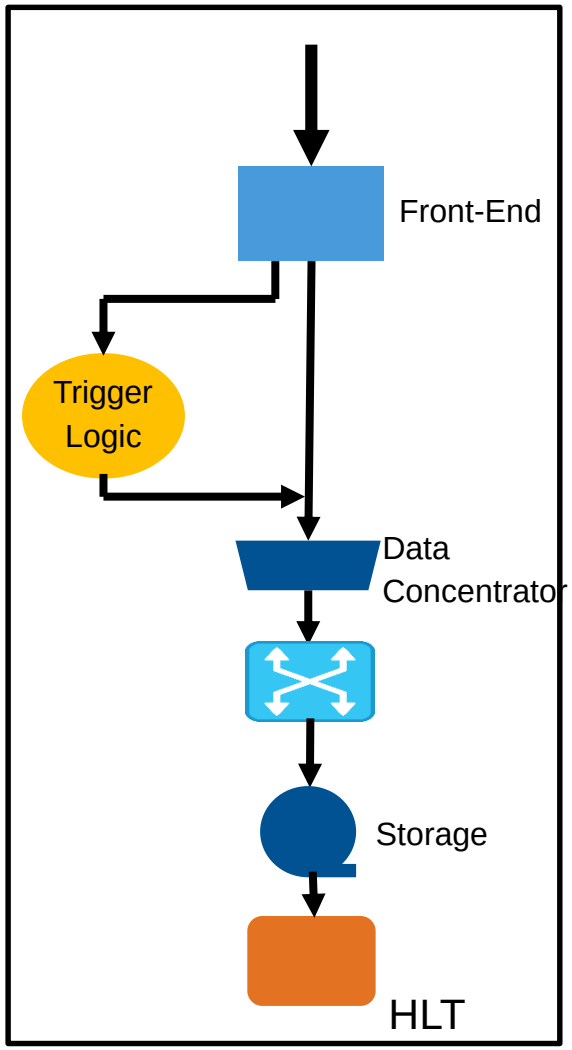


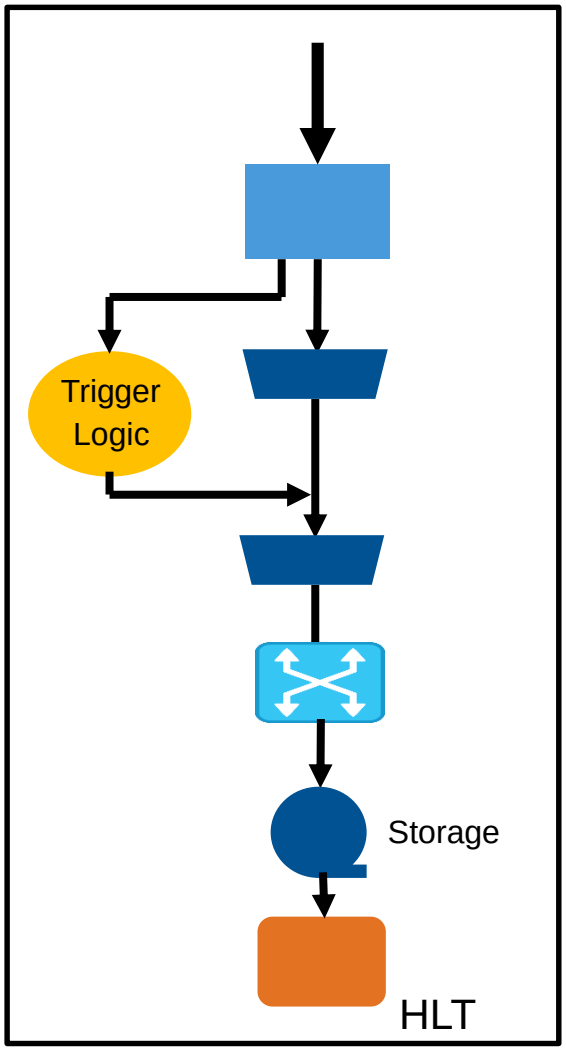
FEE Performance :

Trigger rate	aimed :100kHz	real : 40kHz
Dead time	0 %	10-20%

Evaluation of COMPASS DAQ Architecture







Firs Outcome of the Workshop

We have a group of people who is very motivated to work on future DAQFEET towards trigger less read out

Development of prototype FEE, DAQ and Trigger modules

- Fine time TDC – Freiburg
- TDC for wire chambers – TUM, Torino
- DAQ/Trigger – TUM, Mainz
- Trigger less MSADC - TUM

Feature extraction for calorimeter – Warsaw

DAQ Hardware - TUM

DAQ software - Prague, Dubna

Discussion Outcome

It’s important to start developments of new type of FEE and Trigger Logic compatible with trigger less readout :

- It will be profitable for all physics programs because it will provide more advanced trigger logic and online filtering
- take advantage of already developed technology within DAQ
- develop new technologies to evaluate and validate trigger less read out on prototype level

Problems discussed : needed online alignment

Identifying projects which we can be started now when physics program not approved and funding is limited

Starting projects :

- **new generation of TDC FEEs for Wire chambers and SciFis**
- **Digital Trigger**
- **Feature extraction for Calorimeters**
- **Trigger less data handling concept**
- **Analysis software**

What is Next ?

TB :

- Express an interest to launch R&D
- Define development priorities
- Request to provide R&D plan
- Form a group

Collaboration :

- Provision of PHD students (comment: TUM expects one PHD position for HW development)
- Provision of funding

THANK YOU

Front-End and DAQ Electronics

Detector type	**# of channels**	**Current electronics**	
Calorimeters ECAL0, ECAL2	4.800	12b ADC@80MHz	
Calorimeters HCALs, ECAL1	2.200	10b ADC@80MHz	
Silicon, GEM, PGEM, PMM	~100.000	APV25 ASIC	
RICH, MWPC	60.000	APV25 ASIC	
RICH, MAPMT	12.000	F1 TDC	
SciFi	~2.600 ?	F1 TDC GANDALF TDC	
Beam Momentum Station	640	F1 TDC	
Hodoscopes, VETO	500	F1 TDC	
Wire Chambers	~60.000	F1+FPGA TDC	
Recoil Detector	96	14b ADC@0.5(1.0)GHz	