VMM and the SRS - update

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Presentations at the last Collaboration meeting in September

Lara Bartels: Analysis of VMM3 test beam data

→ Detector with 3 VMM3 hybrids in SPS beam

Manuel Guth: VMM3 Slow Control Software

→ New software to control the SRS + VMM

Me: VMM and the SRS - update

→ General update: Master/Slave, hybrid design, powering

→ need additional ADC on hybrid for calibration and online monitoring

→ finalise design of hybrids and DCards

What happened since September

New student from University of Bonn for about 2 months

→ Lucian, working on VMM cooling (see his presentation) and test beam analysis

RD51 test beam in October

→ continue VMM3 tests at SPS beam, four hybrids (see Dorotheas presentation)

Hybrid firmware change for CKBC (coarse time measurement)

→ high (logic 1) has to be < 20 ns and > 12.5 ns, otherwise no correct time measurement

I2C test of new ADC for hybrid

→ understand and test I2C implementation in current firmware, test if an ADC can be operated on the hybrid

BrightnESS test beam in December

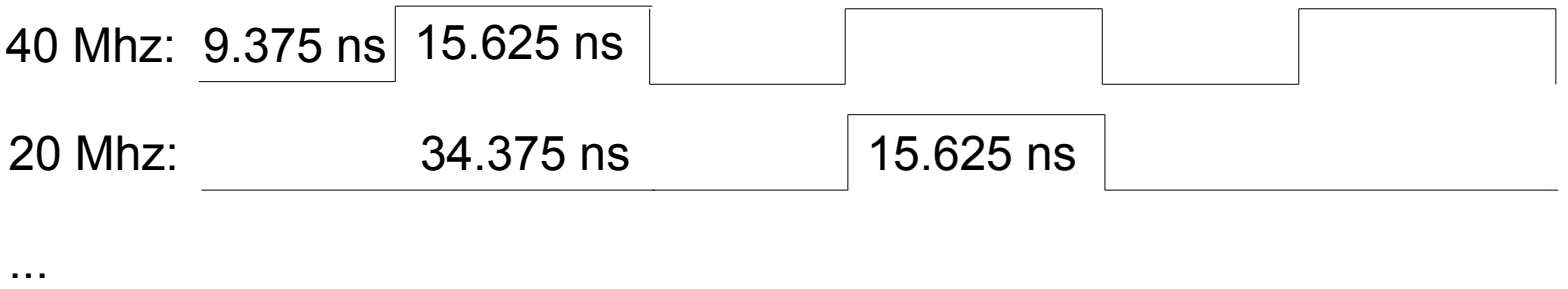
→ first neutron test beam with VMM3 hybrids (four) and better software (see Mortens presentation)

CKBC firmware change

High (logic 1) has to be < 20 ns and > 12.5 ns

- CKBC can be set: (2.5, 5, 10, 20, 40, 80, 160, 160 inv.) MHz
- With the requirement: CKBC ≥ 80 MHz not possible
- Use high of 15.625 ns for all clocks up to 40 MHz

  → asymmetric clock

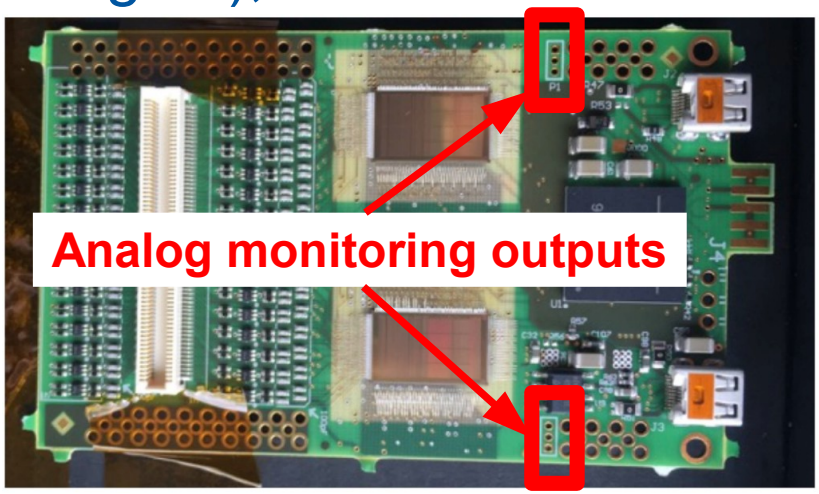


New ADC

Necessary to read monitoring outputs

- M0: Can be set to output global threshold DAC, pulser DAC, temperature sensor level, band-gap reference

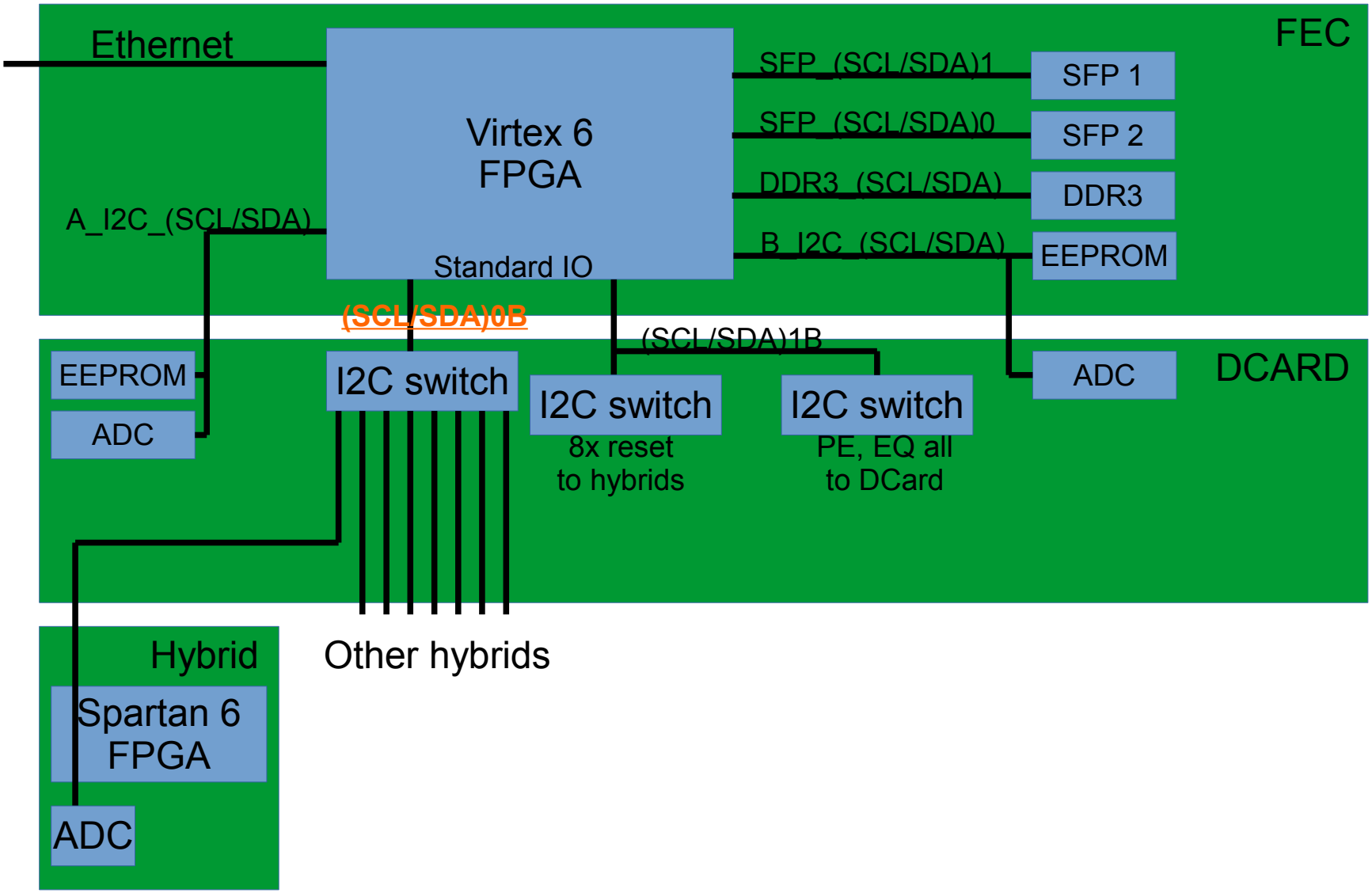
  and for every channel: baseline (and signal), threshold level
- tdo: baseline and ramp
- pdo: baseline and pulse amplitude



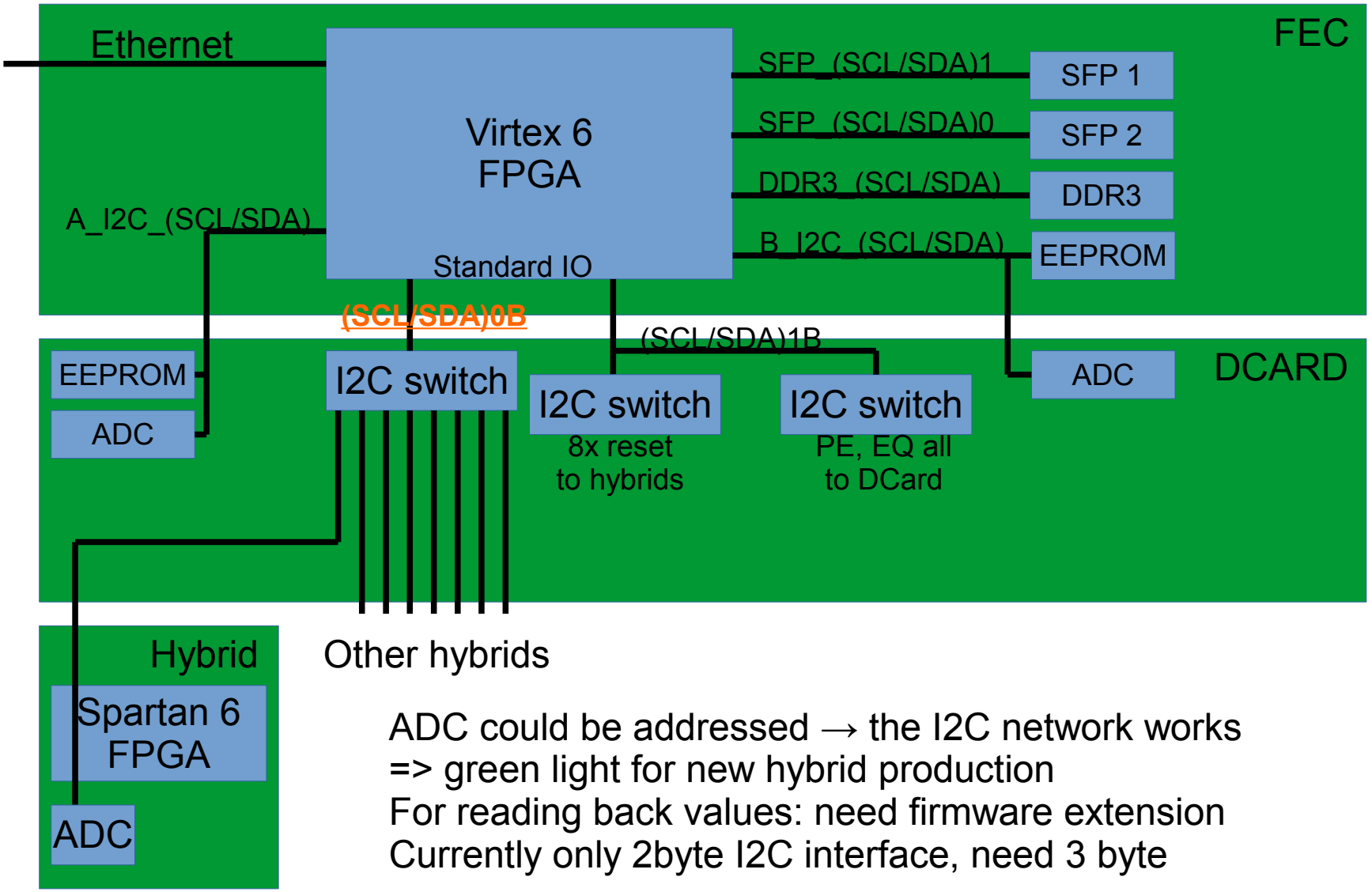
For fast signals (ramp, pulse), ADC is to slow

We need it for calibration of baselines and thresholds

I2C network


FEC
Ethernet
Virtex 6
FPGA
SFP_(SCL/SDA)1
SFP 1
SFP_(SCL/SDA)0
SFP 2
DDR3_(SCL/SDA)
DDR3
B_I2C_(SCL/SDA)
EEPROM
A_I2C_(SCL/SDA)
Standard IO
(SCL/SDA)0B
(SCL/SDA)1B
EEPROM
ADC
I2C switch
I2C switch
8x reset
to hybrids
I2C switch
PE, EQ all
to DCard
ADC
DCARD
Hybrid
Other hybrids
Spartan 6
FPGA
ADC

I2C network



ADC could be addressed → the I2C network works
=> green light for new hybrid production
For reading back values: need firmware extension
Currently only 2byte I2C interface, need 3 byte

How you can support the SRS+VMM development

Send a student! (master/PhD, should stay at least for two months)

Good experience so far:

- Freddy Fuentes (Universidad Antonio Nariño, Bogotá)
- Lara Bartels (University of Göttingen, CERN summer student)
- Manuel Guth (University of Freiburg, CERN summer student)
- Lucian Scharenberg (University of Bonn)

Win-win-win situation:

You: Student brings back experience with operating the SRS + VMM setup

We+You: Student advances the project

Student: Stay at CERN

How you can support the SRS+VMM development

Send a student! (master/PhD, should stay at least for two months)

Proposed projects:

1. Advance slow control: implement automated calibration, extend user friendliness

→ preferably stay of 6 months, should know C++, Qt, also work in the lab for testing

2. Implement useful triggered readout in firmware

→ at least 2 months with knowledge of FPGA programming (> 3 month only basic knowledge)

3. Improve readout speed from VMM to Spartan-6 FPGA

→ at least 2 months with knowledge of FPGA programming (> 3 month only basic knowledge)

4. Understanding the VMM readout and documentation for users

→ no prior knowledge required

5. VMM hybrid characterisation for user references

→ some experience with working in the lab, using instruments

Summary

SRS + VMM project is advancing very well

⟶ see other talks

- Four test beams with VMM3 hybrids
- Cooling is addressed
- Very fruitful exchange with the ATLAS NSW electronics team, e.g. for CKBC issue (thanks George for all your input)
- New hybrid with ADC will go in production soon
- Support from interested groups is appreciated

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