VMM3 Test beam

VMM3a Status

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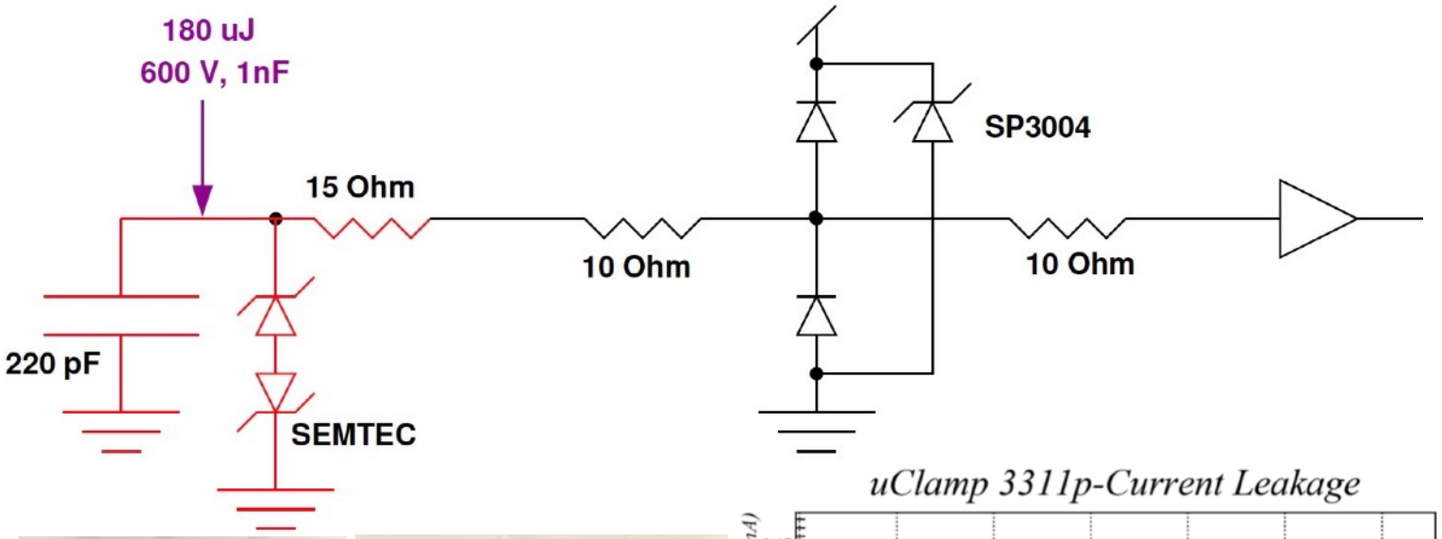
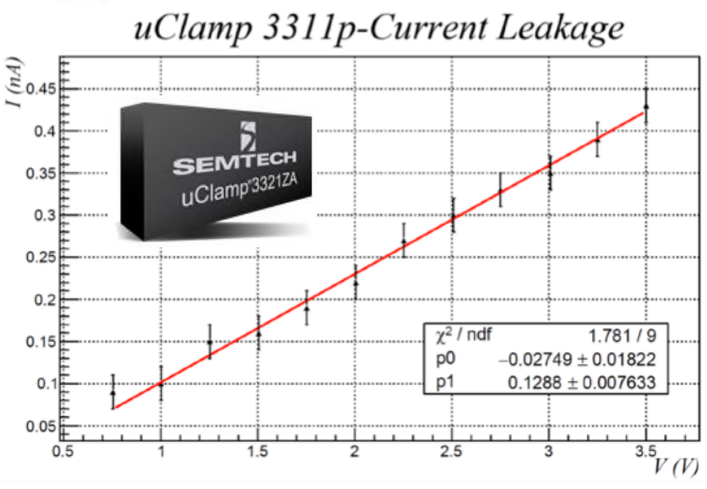
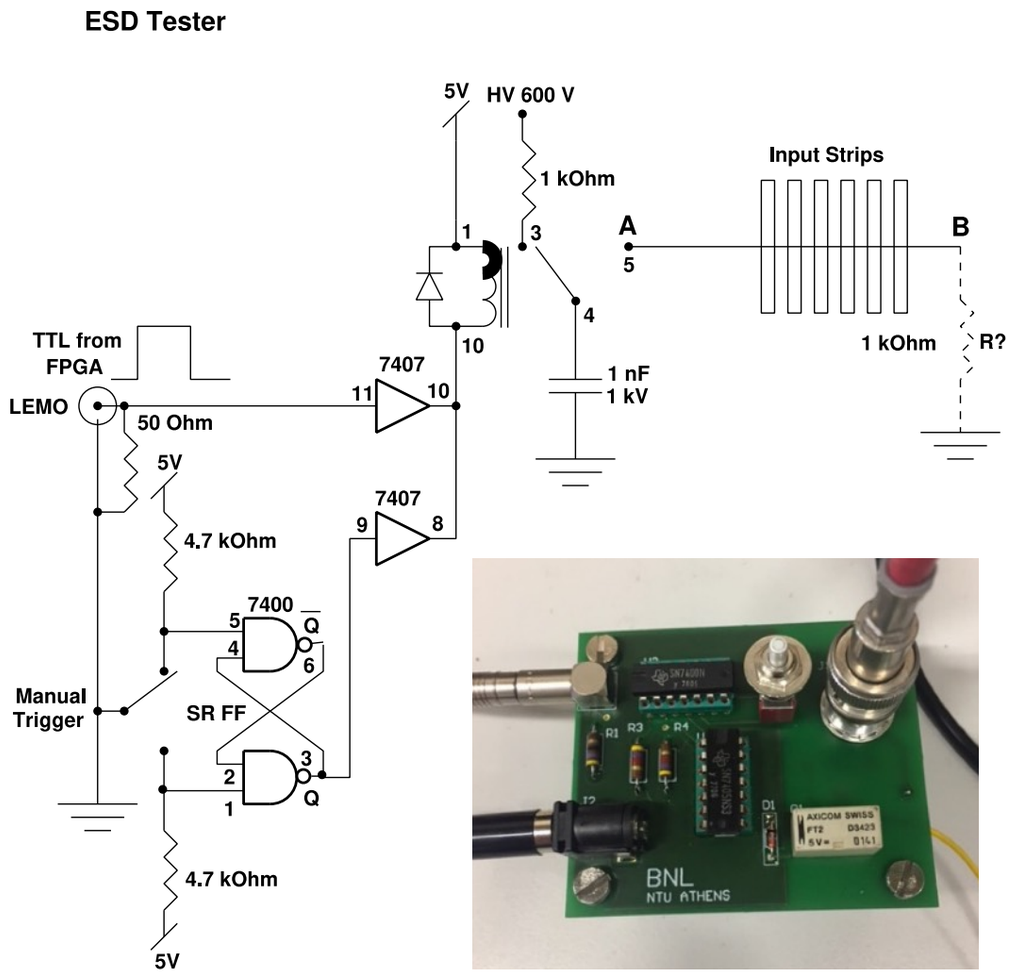
ESD Protection

- Since the VMM2, we have experience major channel (initial NUP4114 issue). Moving to 130nm technology made the requirements on input protection higher. Current protection scheme based on the SP3004 seems inadequate to protect the VMM front ends
- We lunched a dedicated ESD testing procedure which allowed us to systematically tested the input of the VMM.
- Understanding has improved a lot during the last months understanding this issue
- We developed a VMM board (MMFE1) with Panasonic connector and a VMM socket to perform systematic tests. On top we built a Panasonic based connector daughter-board to test different protection schemes and different footprints.
- 220 pF capacitor emulates typical MM strip capacitance, a channel like this survived repeated discharges while without protection is dead after a single discharge. Then survived zapping overnight (>30,000 discharges)

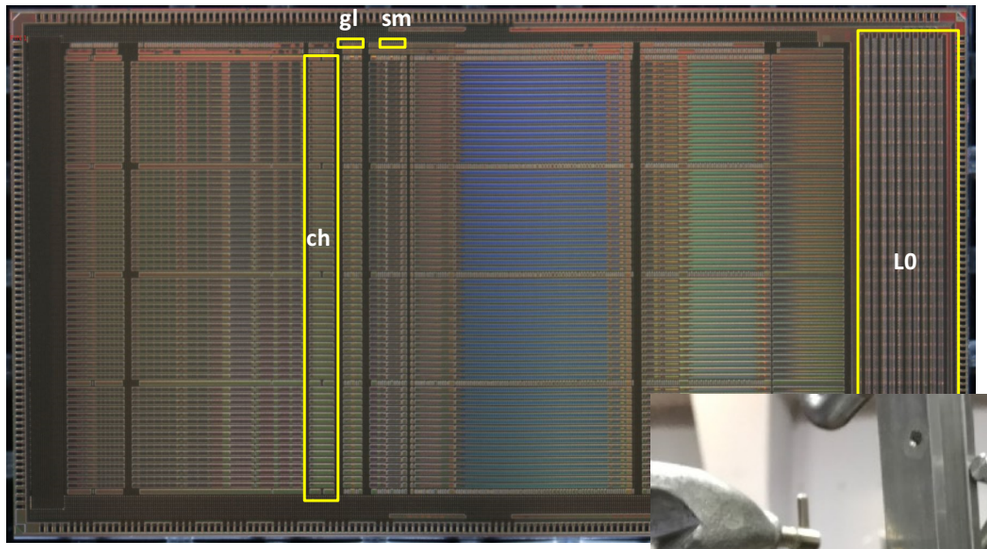


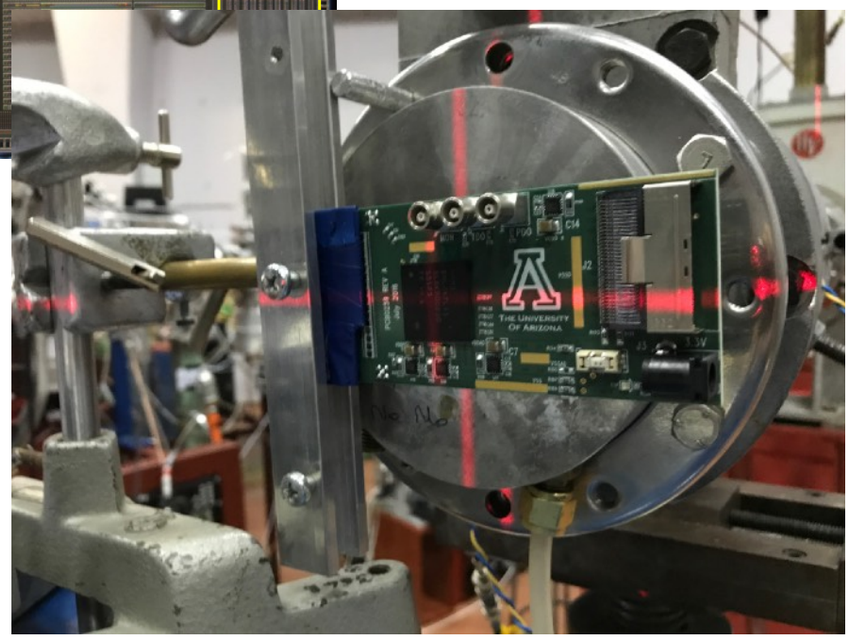




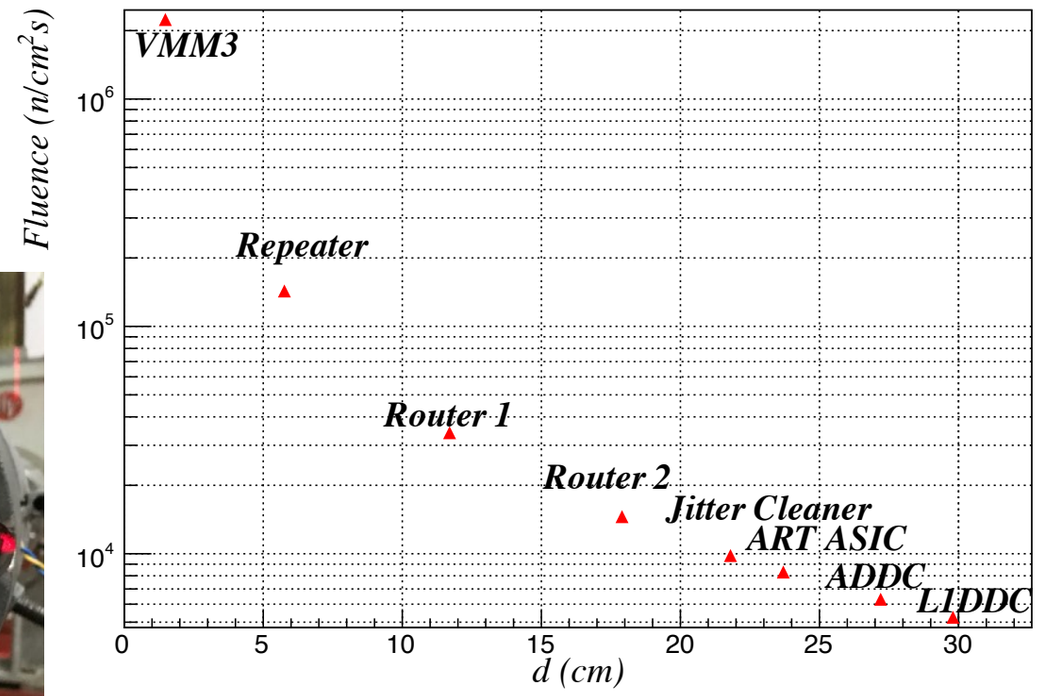
SEU Protection

- VMM3 there are two types of storage elements that require SEU protection, the configuration register which use Dual Interlocked Cells (DICE), and the state machine control logic which uses Triple Modular Redundancy (TMR)
- For the non-L0 registers and non-L0 state machine the on chip location is well defined
- For L0 an automated place&route was used and the registers may be scattered all over the L0
- VMM3 accumulated a total dose of 2.28×10^{11}, 20MeV neutrons in 34.7h.
- The SPI was readout every 12 sec
- There were periods were the chip was readout in continuous or L0 mode for stability tests. For these periods the chip was not re-configured.
- No problems observed in configuration
- Readout was stable all the time.



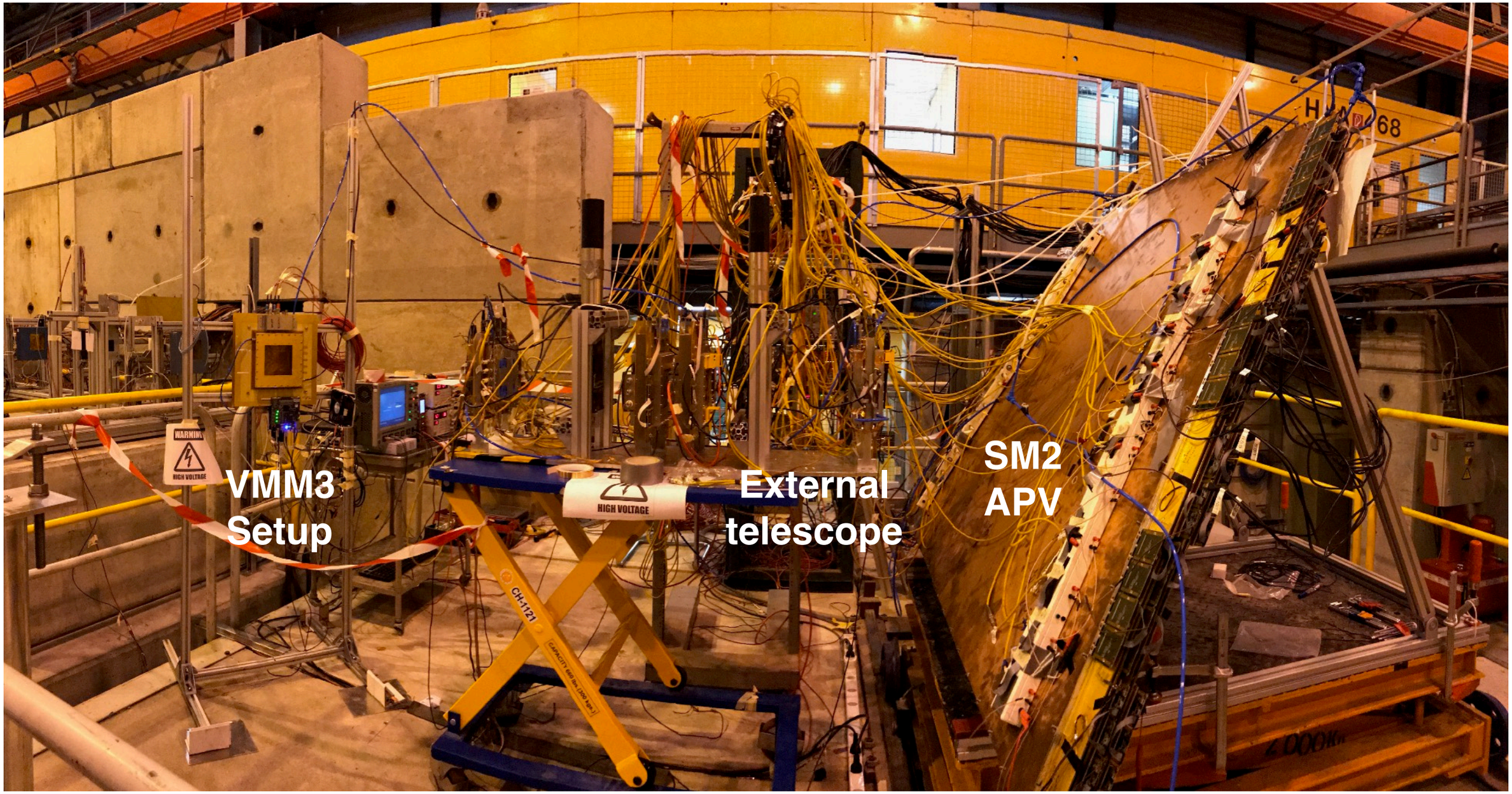


Neutron Fluence (10mmx10mm)



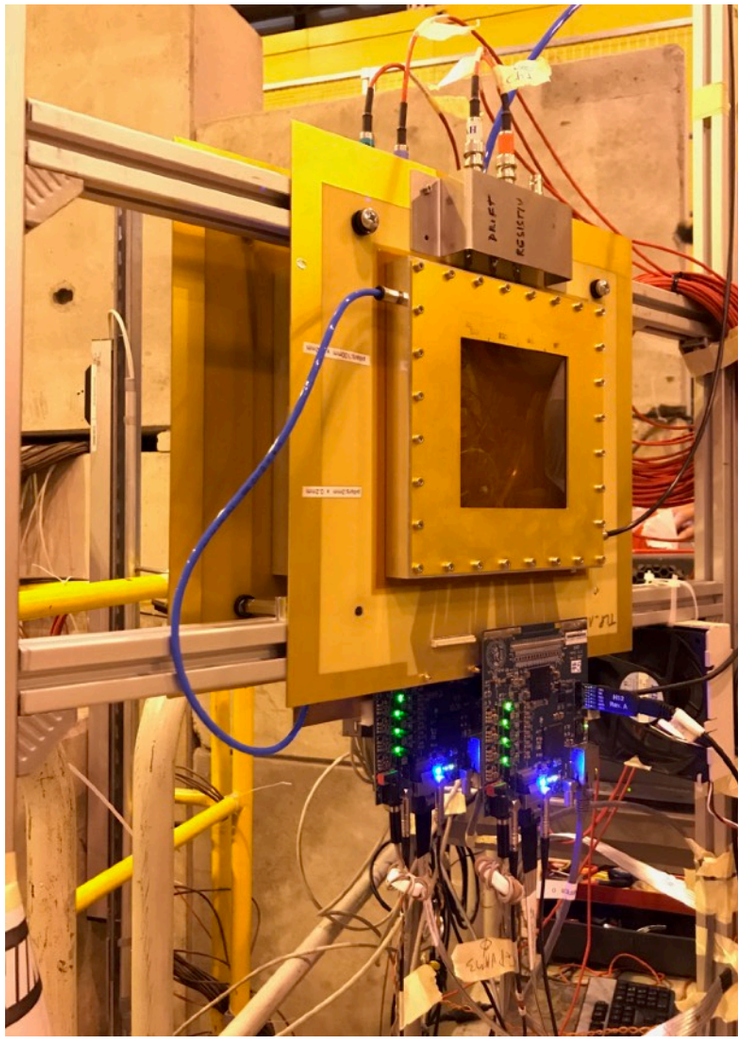
Setup (1/2)

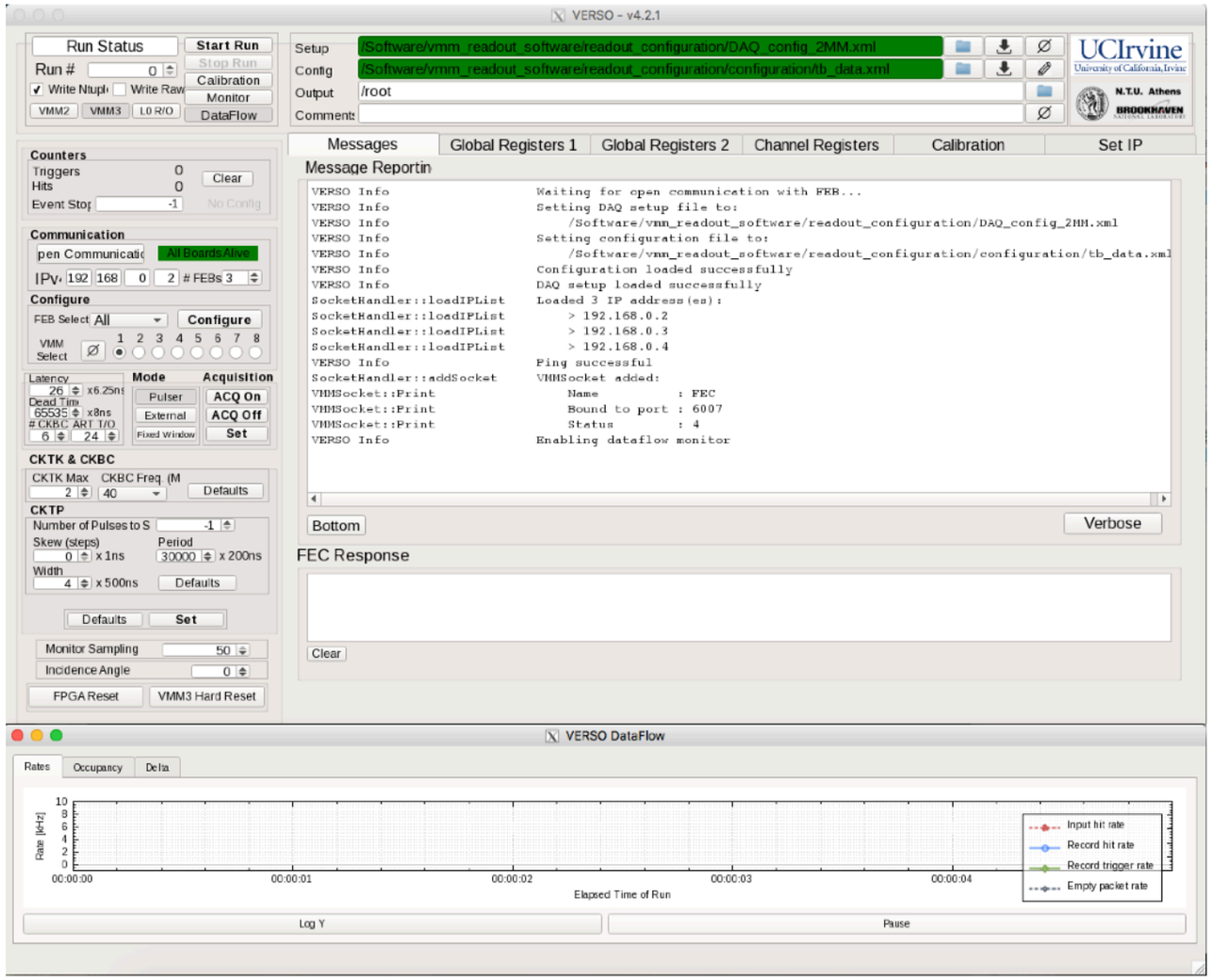
- We run for ~3 weeks at H8C during August. Main goal of the testbeam was to evaluate the performance of the VMM3 on Micromegas detectors and see if there were issues that needed to be corrected before VMM3a submission.
- VMM setup consisted of 2x MMFE1s on 2x T type chambers (T4,TLP) (64 channels each).
- SM2 with APV25 and GEM telescope with APV25 (not relevant to this talk).
- External scintillator trigger as a trigger system.



Setup (2/2)

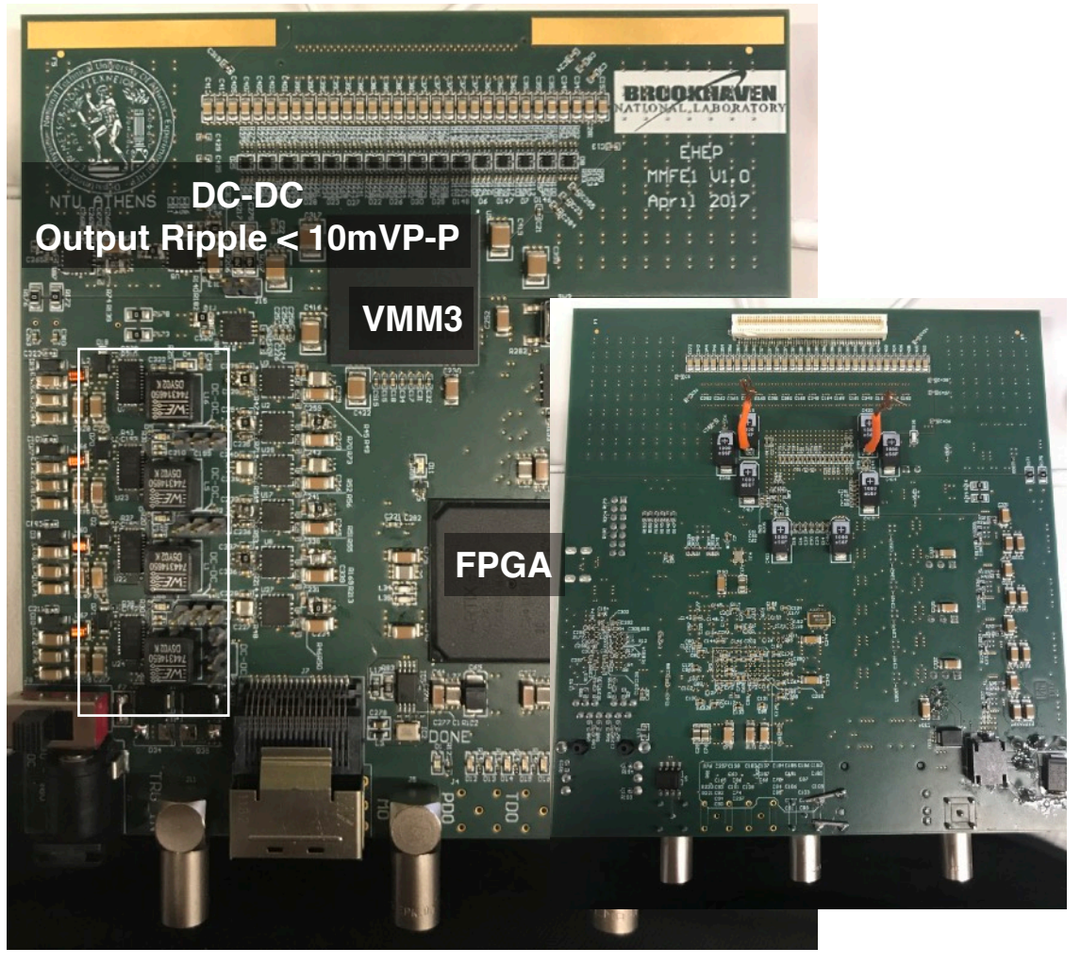
- VERSO was used to readout the data and the firmware was developed such to control the CKBC which allowed precise timing measurements along with ART measurements.
- Data taking efficient after few iterations. We achieved easily ~20KHz/channel readout - 200K events / spill or more. Few million events per run in few minutes. Data with more than 200 Millions of events. Analysis is slow since there is not much available time.
- The chambers were mounted on an aluminium frame that allowed rotation independently of the rest of the setup.
- Common trigger to all the system provided by 3 scintillators. This is a control signal for the VMM TAC (more later).

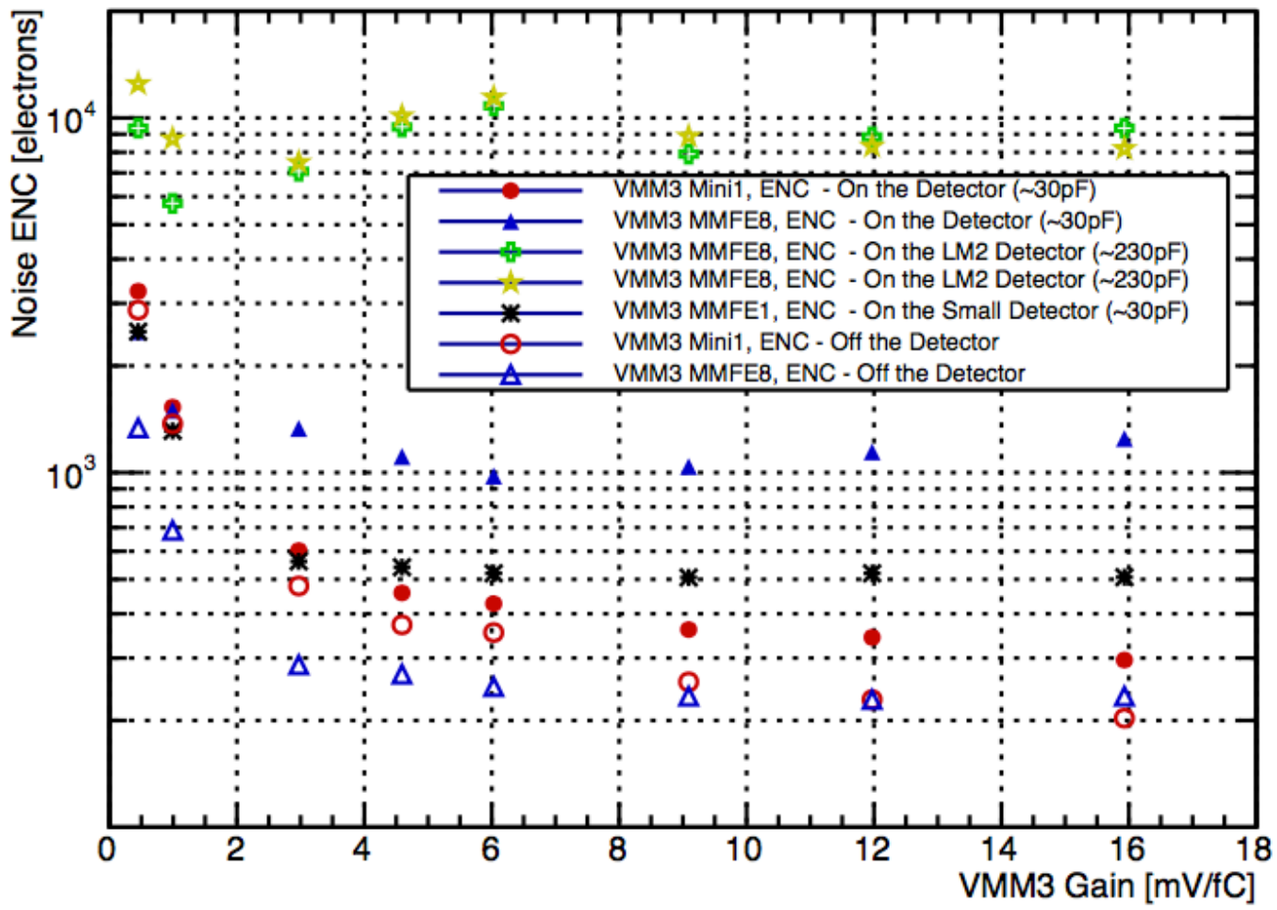




The MMFE1 - Noise measurements

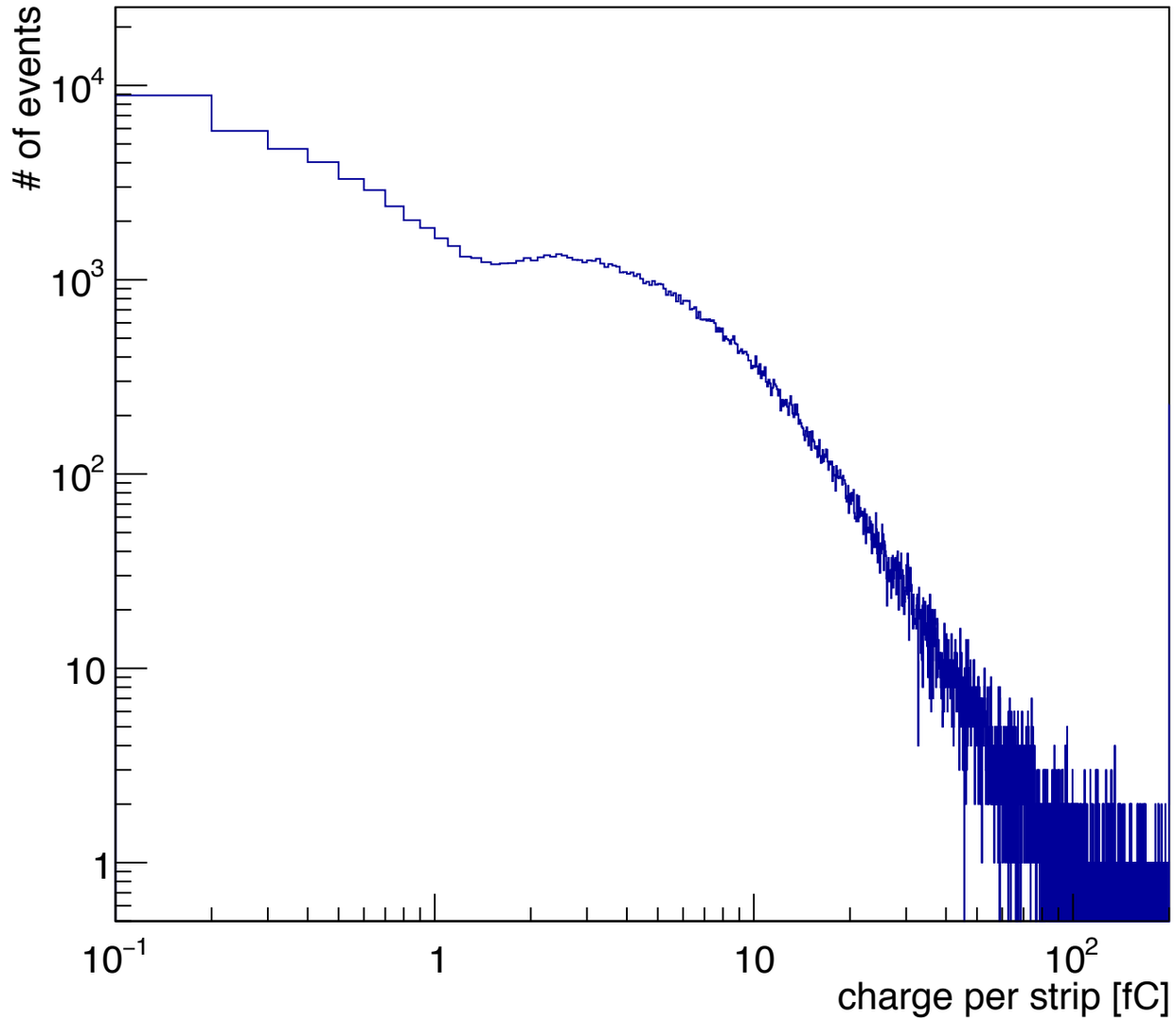
- The MMFE1 is a board on which 1x VMM exists along with FPGA and ethernet readout
- The board has commercial DC-DC converters with <10mV ripple (as specified in the datasheet)
- The board was designed to get external clock and trigger.
- Noise measurements on the board itself showed ~30% more noise with respect to the mini1 board on which we achieve noise levels almost intrinsic to the VMM3 theoretical noise.
- It was considered good enough to perform tests. What was found is that the ground connection to the chamber needs to be the shortest possible one.
- Automated measurements of noise with xADC was compared with measurements on the scope and was found ~1.5x more. This is understood since it is the RMS of the waveform and not the RMS of the peak-to-peak.





Charge on Micromegas strip - simulation

- If someone assumes a worst case for NSW of tracks under 30º on which the charge spreads over a number of strips (mean value at ~6 strips) then someone can study the charge profile of a strip.
- Below is a charge profile for a strip independent of its position in a cluster for 150k events under an angle of 30 degrees with a gain of 10^4. This includes ionisation fluctuations, secondary electrons, gain fluctuation.
- Claiming that we need to detect one electron actually means nothing. The point we need to achieve is the best signal to noise ratio. That means minimising the noise and keep the detector gain high enough.



- If we consider several cases:
  - Small chambers with an ENC of 300e will lead to a small loss of the order of ~10%.
  - In the larger detectors this becomes more and more essential as in case of ENC~3000e the signal that cannot be distinguished from noise is 32.65%. This along with degradation of timing performance due to capacitance will deteriorate the uTPC performance.
  - Scenarios of running detectors with a gain of the order of 10^3 I believe are not realistic.

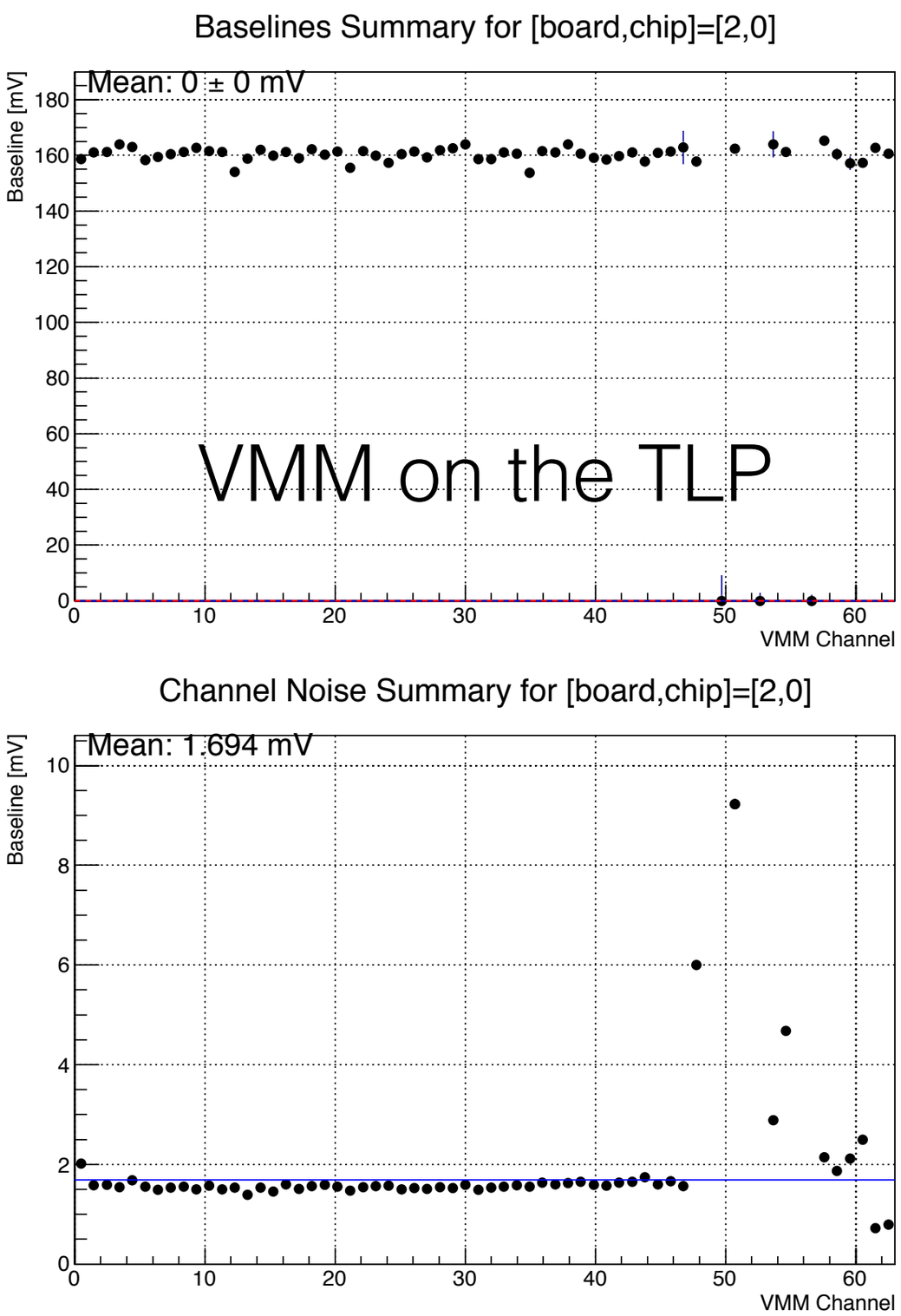
Developments

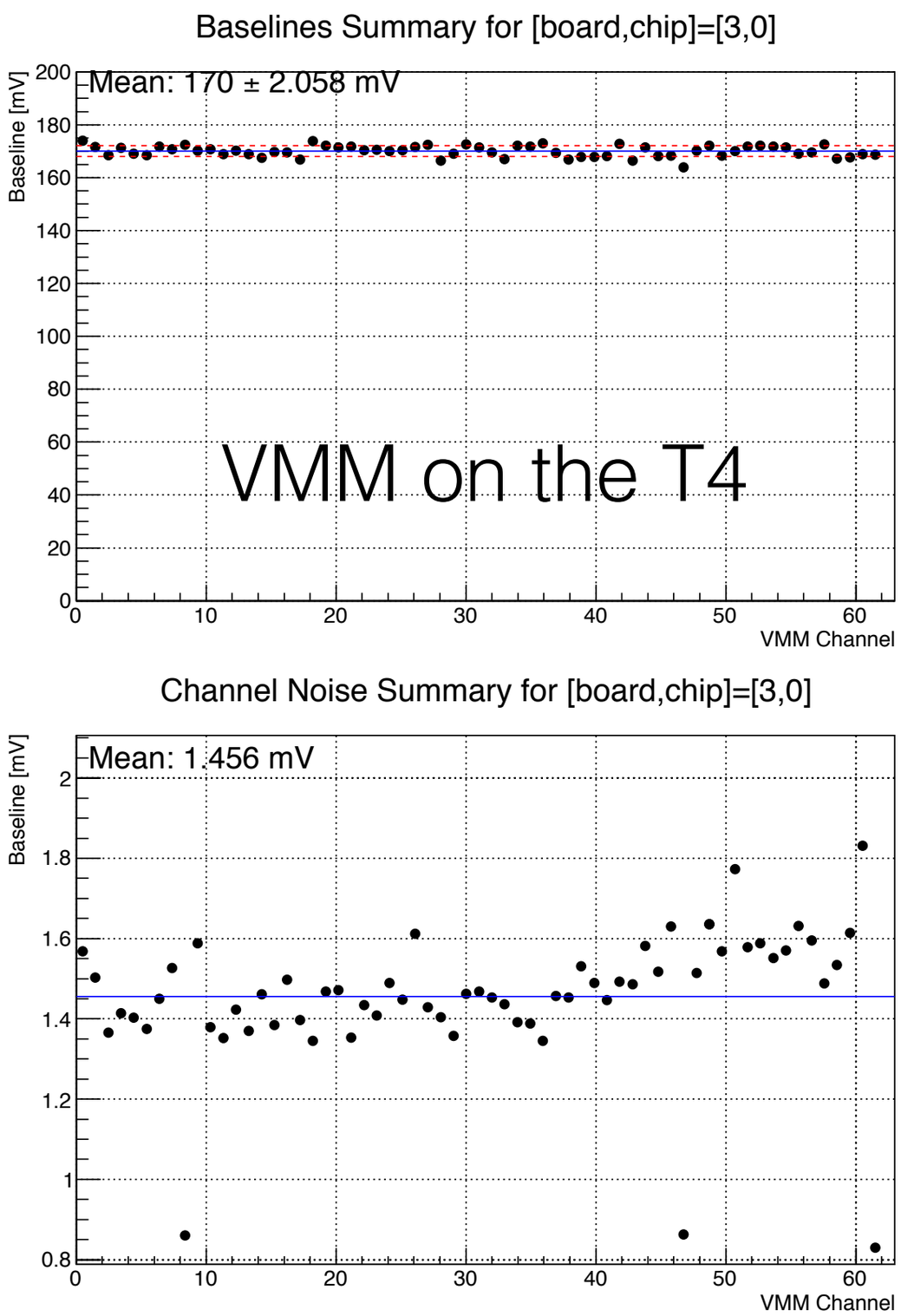
- The external scintillator system provided the trigger through a fanout to all the boards, but VMM knows nothing about the trigger, a clever way was needed to do timing studies in an non-synchronous environment like the testbeam.
- The boards were synchronised with an external 40MHz clock coming from the CTF and a soft reset was initiated from the control room through the CTF card. This allowed the BCID counter to be reset before the run and to be synchronised along the boards.
- A clever busy system was implemented through an interconnection (hdmi) between the boards blocking triggers in case the readout hasn't finished.
- The readout mode was done by selecting only relevant to the trigger events:
  - The trigger latency was measured.
  - Then the CKBC was not running continuously but it was started at a fixed time after a configurable latency (+trigger latency) and for a configurable clock ticks to stop the TAC.
  - It was followed by a fixed time allowing digitisation
  - Channels fired outside this timing window were reset (stcr bit on VMM).
  - UDPs formed were readout by the VERSO which built events on a common trigger counter.
- The readout of the ART was implemented in a similar to the ADDC way.
  - The first ART was readout.
  - If for a configurable amount of time there was no trigger, the ART was discarded and then the next one was captured.
  - If a trigger occurred, the ART was stored along with each timestamp of 160MHz clock to the event and readout with the offline data.

Testbeam program

- First week - Second week
  - Setup detectors along with services and trigger system
  - Debugging the system, we found that got out of sync wrt the trigger counter. Implemented a busy system that solved the issue. This must be solved for future testbeams in a better way in case many boards are involved.
  - Both T and SM2 setup observed high amount of events with multiple hits on the detectors. After investigation the issue found to be high threshold applied on the scintillators. After fixing the issue we achieved clean data taking.
  - We were able to get high statistics and do:
    - Gain scan (both detector and electronics),
    - Peaking time scan, TAC scan,
    - Neighbour and hysteresis functionality runs,
    - muon or pions runs,
    - Calibration of DACs, TAC, gain, threshold/trimming scan and noise tests.
- Third week
  - Angular scan by testing all the above conditions for uTPC, runs from 10 to 30 degrees.
  - Timing at threshold or peak runs, limited by the nature of the setup and the external trigger latency.
  - Debug the ART. We had an issue to synchronise the ART with the data. Issue was a missing CKBC on the readout of the event. After fixing that we were able to get synchronous data including the ART. The ART was measured with a clock of 160MHz.
  - Tests on SM2 and noise measurements were limited at the time due to lack of time devoted for debugging.

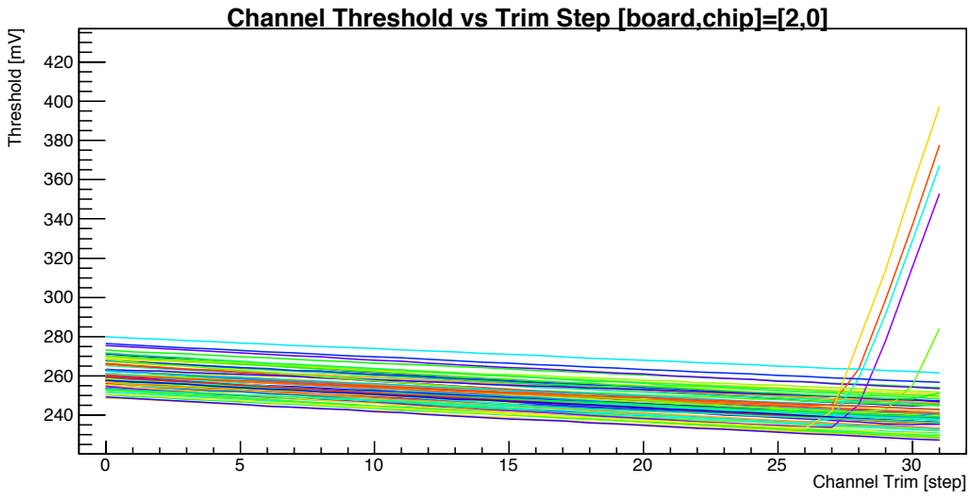
Calibration - Pedestals & Noise with xADC

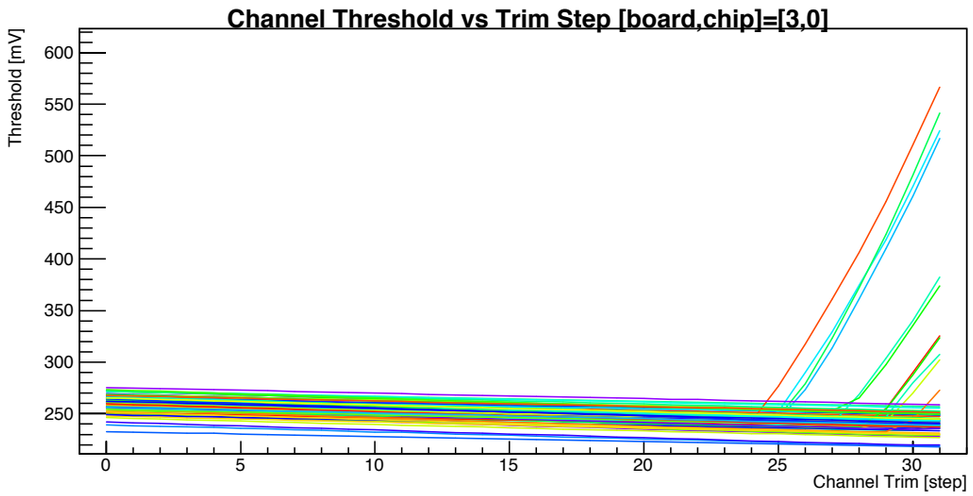


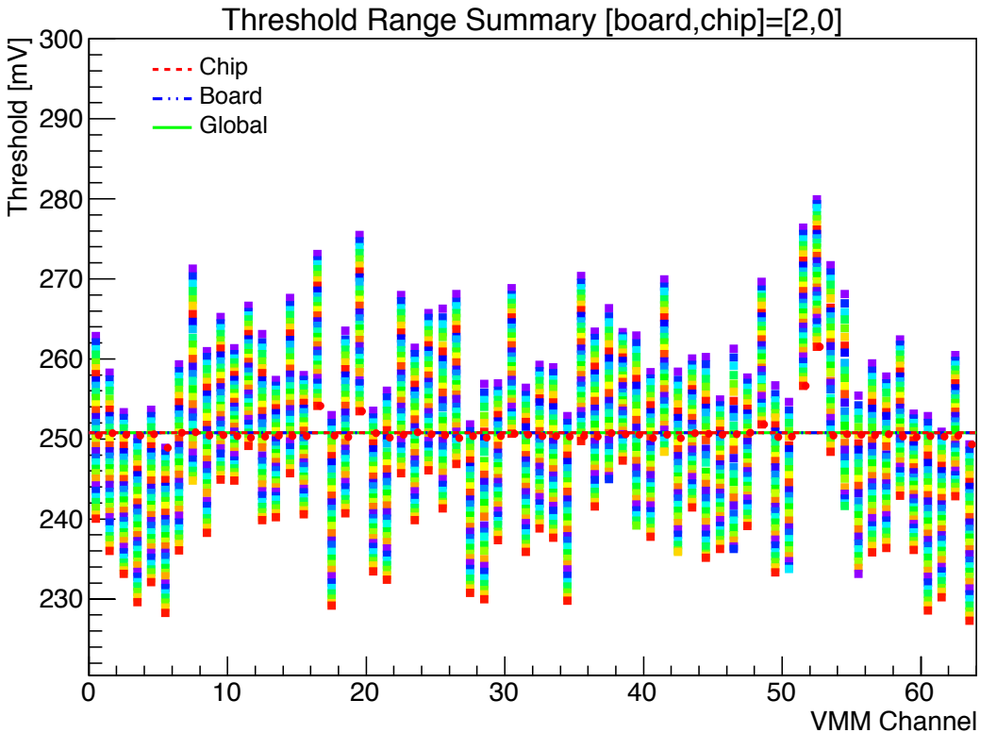


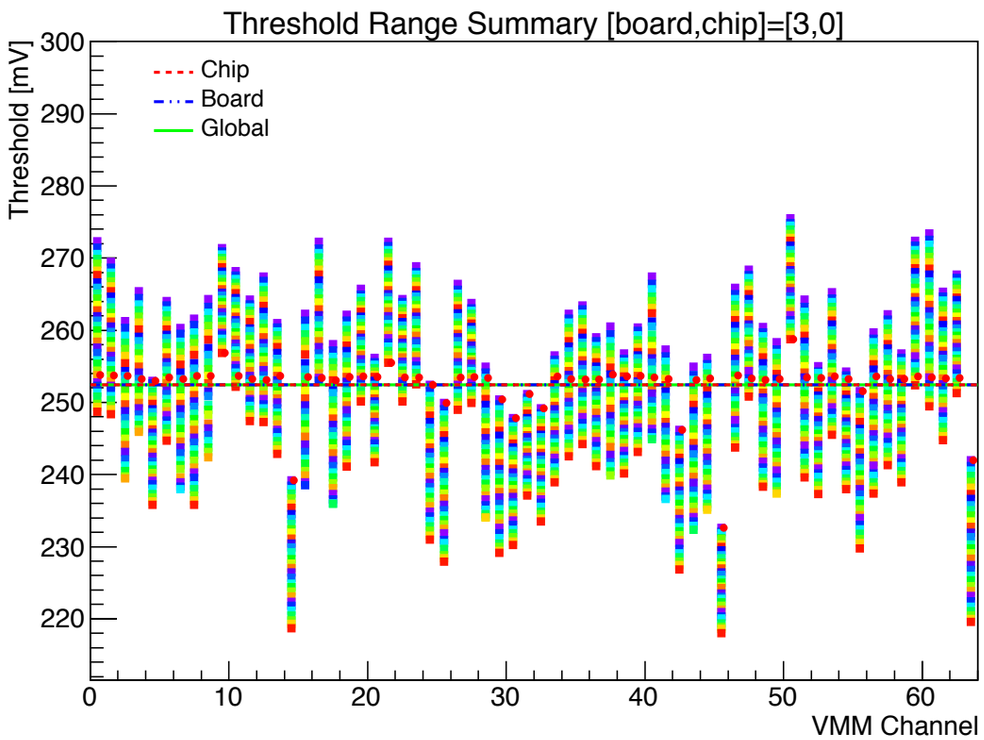
Calibration - Pedestals & Noise with xADC

- For data taking we have calibrated the individual channel thresholds with respect to the global threshold. Due to known bug on the VMM3 trimmers, the full range couldn't be used so we used the best we could achieve. Method used is the finding the level were most channels can be equal.
- This is essential to achieve uniform response of all the channels.





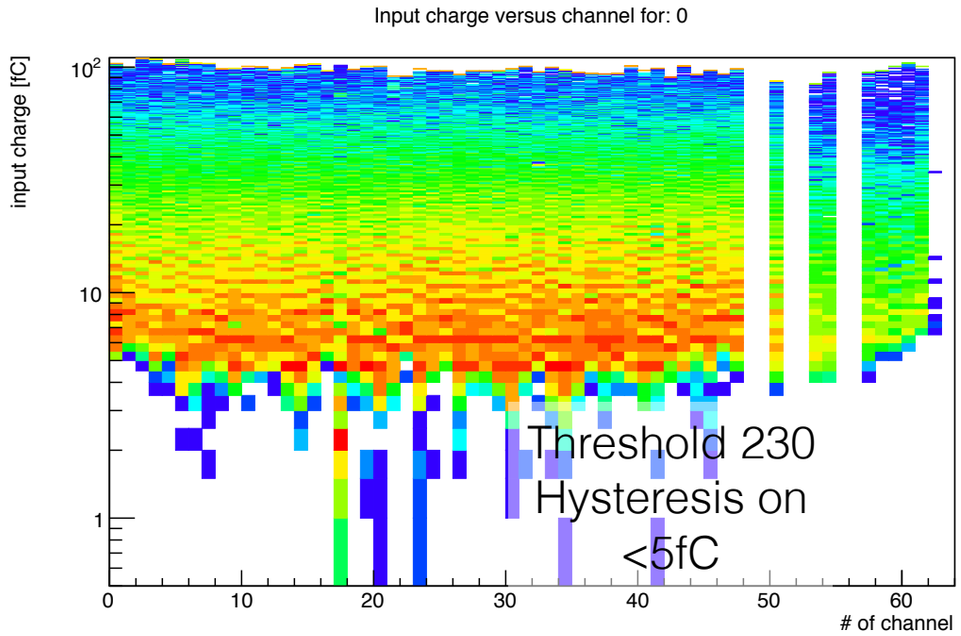


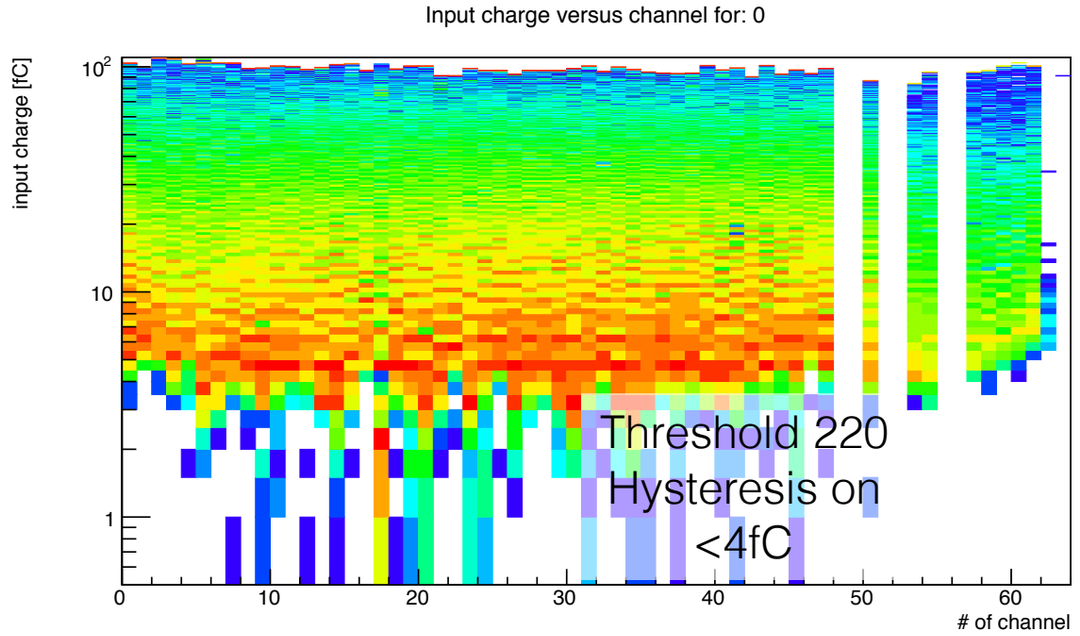


Calibration - Thresholds and hysteresis

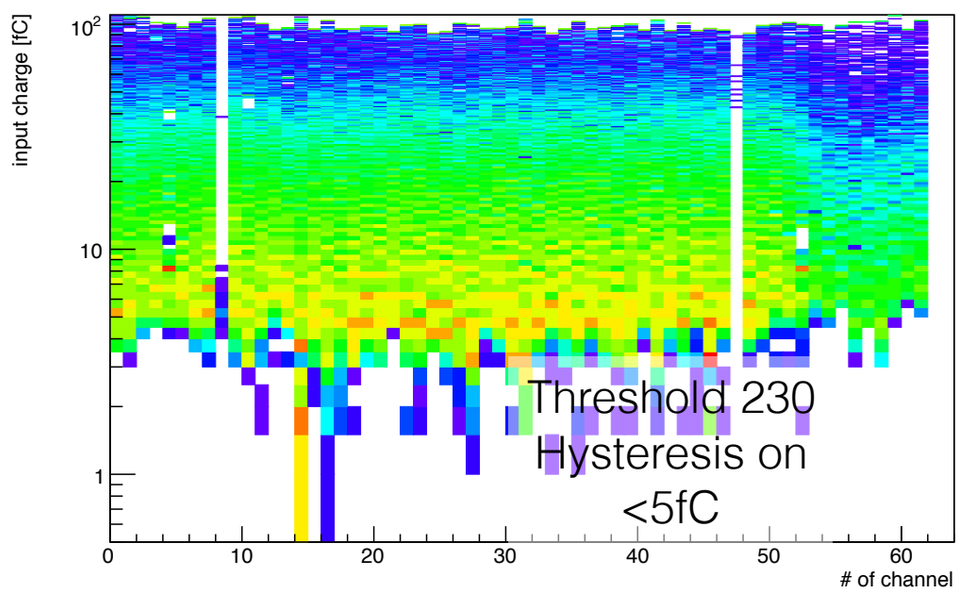
- We went down to 230mV and 220mV until we captured some noise. We found out that the best threshold for data taking was at 230-240mV with the hysteresis on.
- You can see that the signal spreads as expected from the simulation but the theoretical threshold cannot be easily achieved

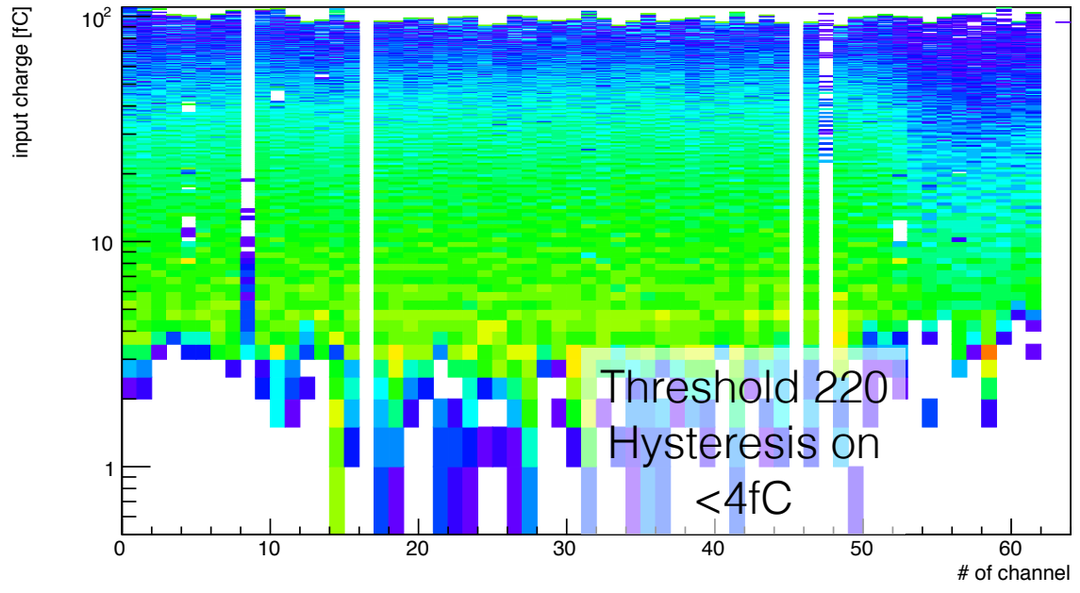
TLP





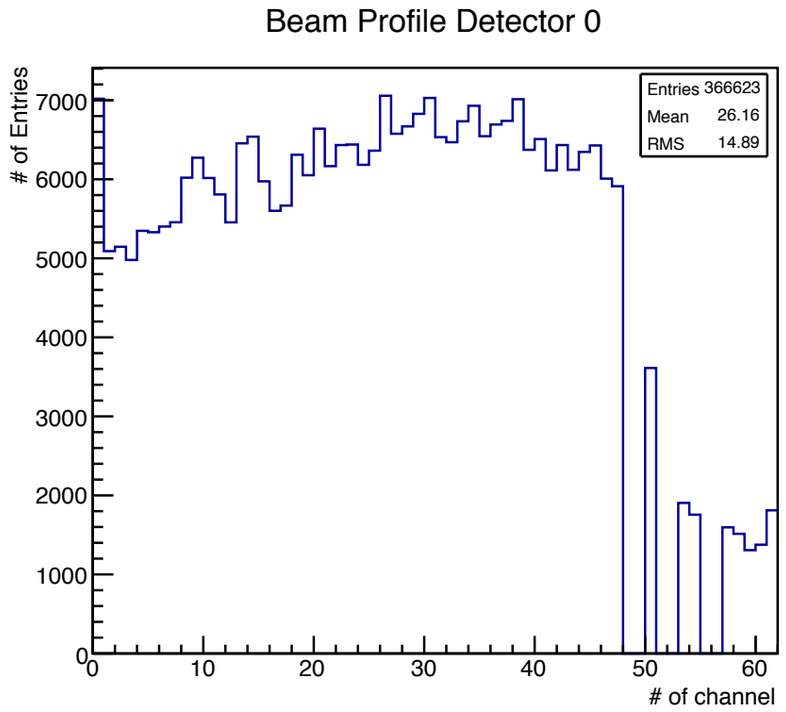
T4

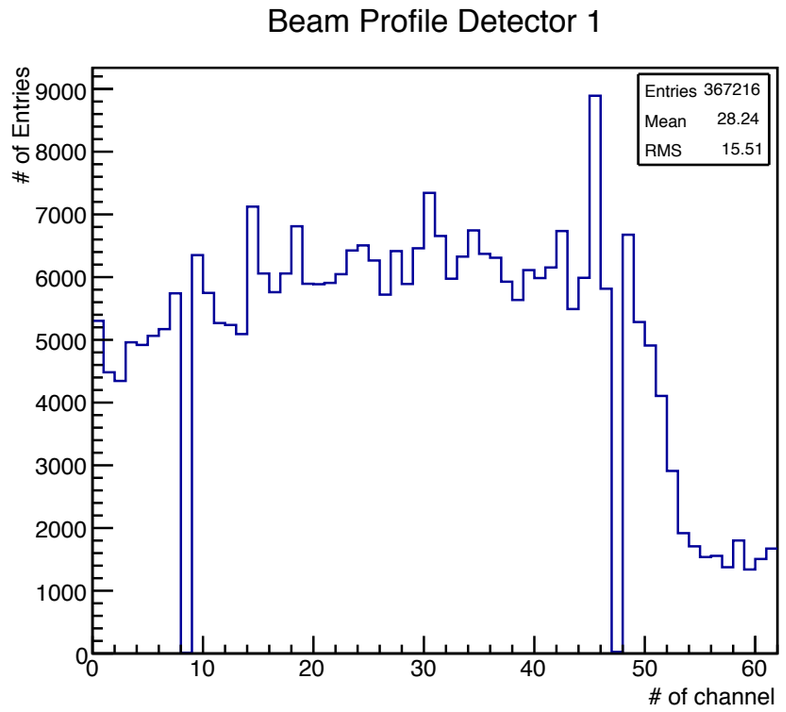


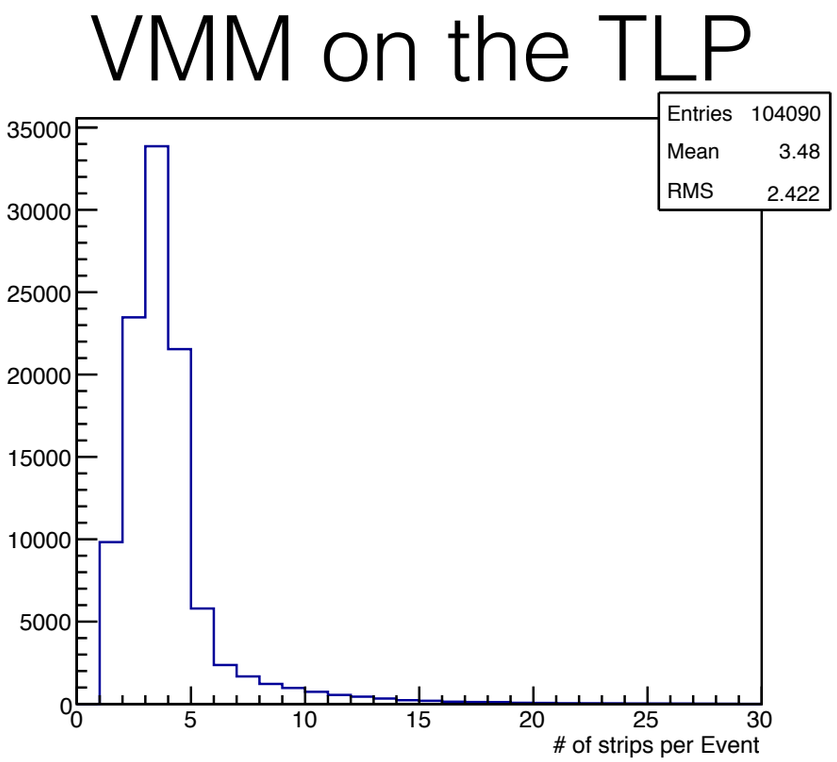


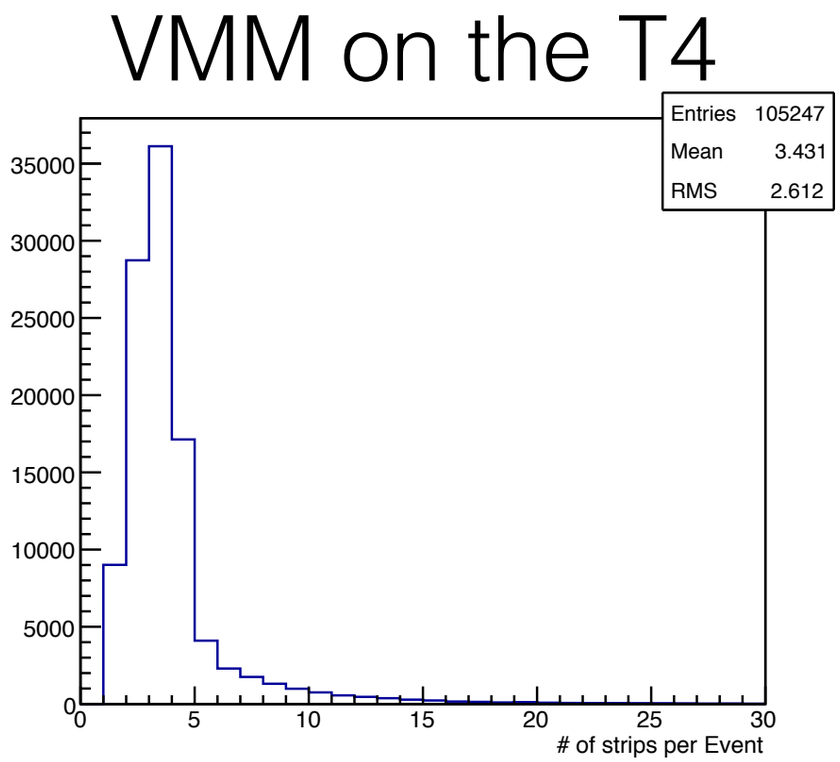
Perpendicular tracks - Raw Data

- Beam profiles with raw data (muons)
- Number of hits per trigger on the lower plots.
- On the first board we have managed earlier than the testbeam to damage many channels after channel 48 so these are ignored for the moment.
- On the second board almost all the channels work fine except two of them.
- Event hits distribution shows a large tail coming from multi track events. Those are cleaned during reconstruction.



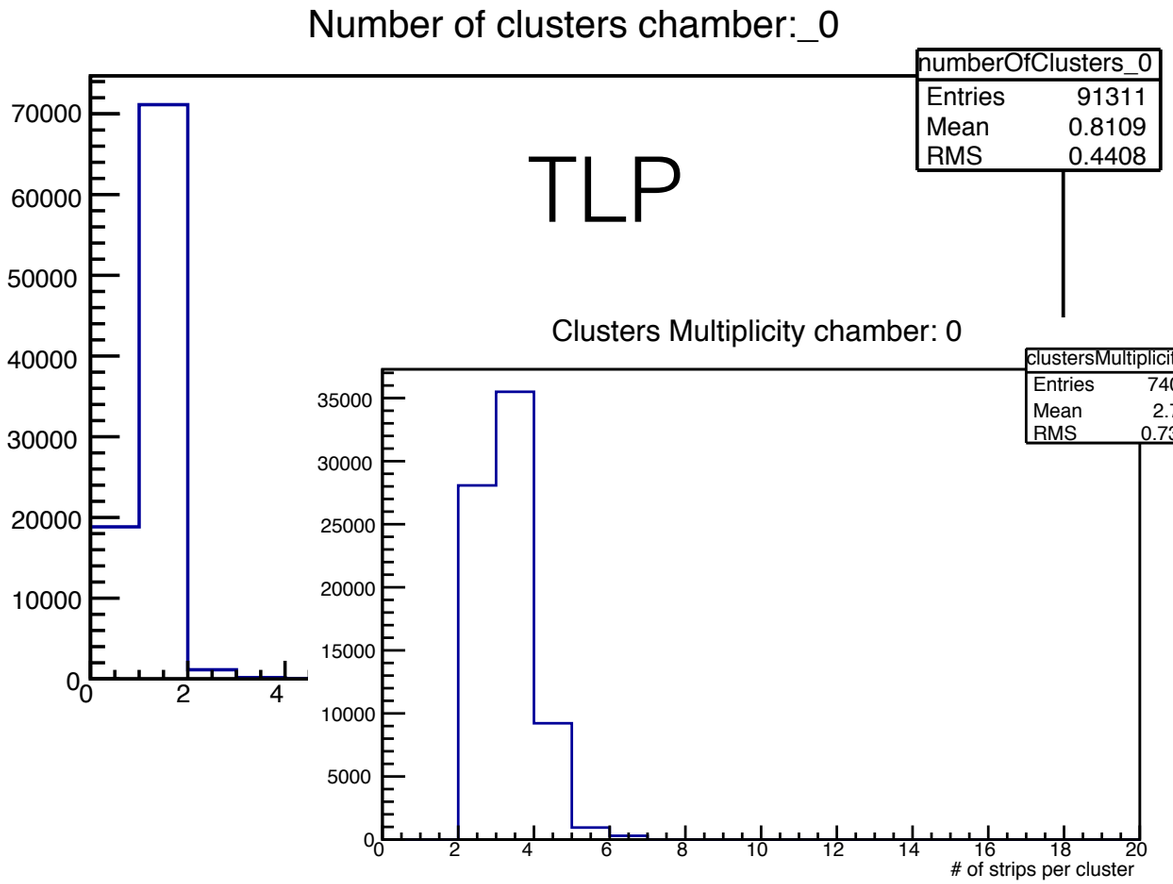


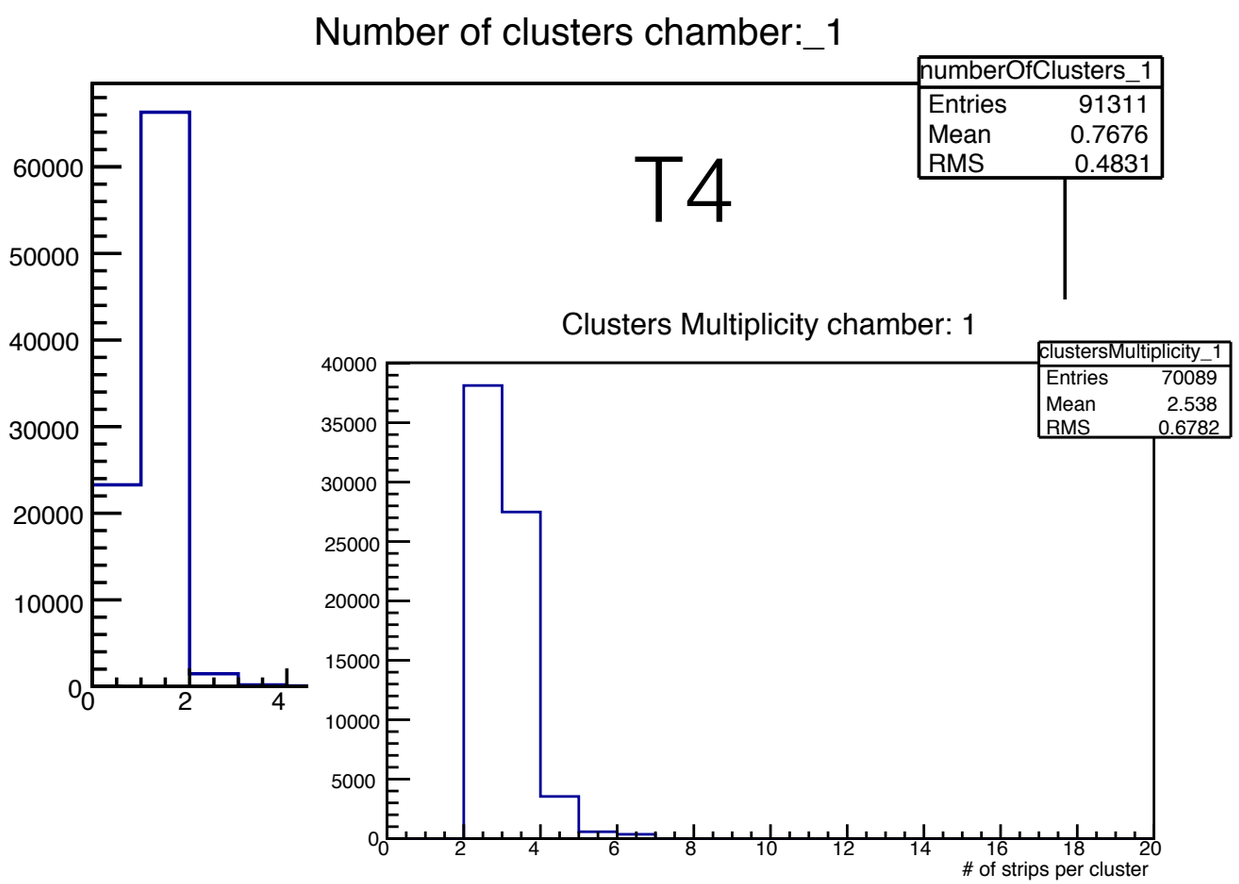




Perpendicular tracks - Clustering

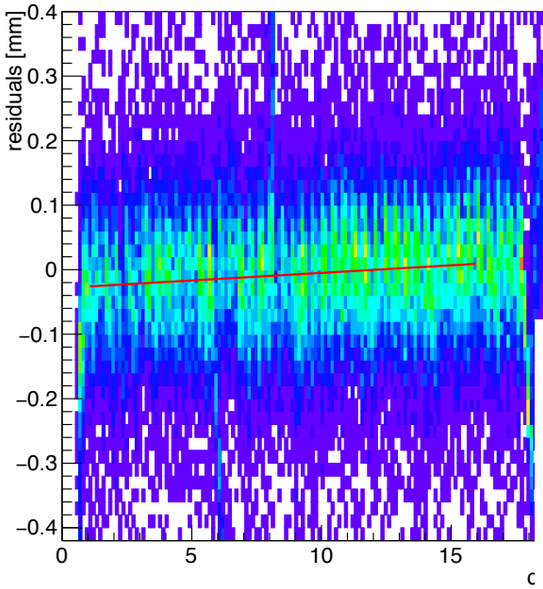
- For the clustering the following algorithm was applied (along with cuts)
  - The strips must be adjacent
  - One hole is allowed (empty strip)
  - Total strips of 2-7 can form a cluster
  - The strips of a cluster must be max 5 BC clocks apart (40MHz) taking into account the turnover of the CKBC.
  - Events with maximum 10 clusters can be reconstructed but as we see the data are clean.
  - The road of the event is within 1mm from the cluster reconstructed on the first chamber.
  - It is obvious form the distribution that the lower gain of the T4 affects the reconstruction but we realised that after the time that we could do something about



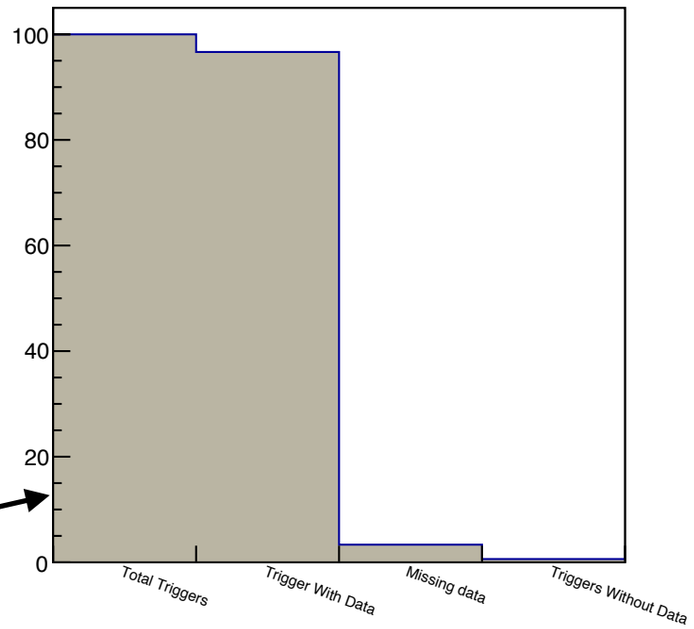


Perpendicular tracks - Resolution, corrections

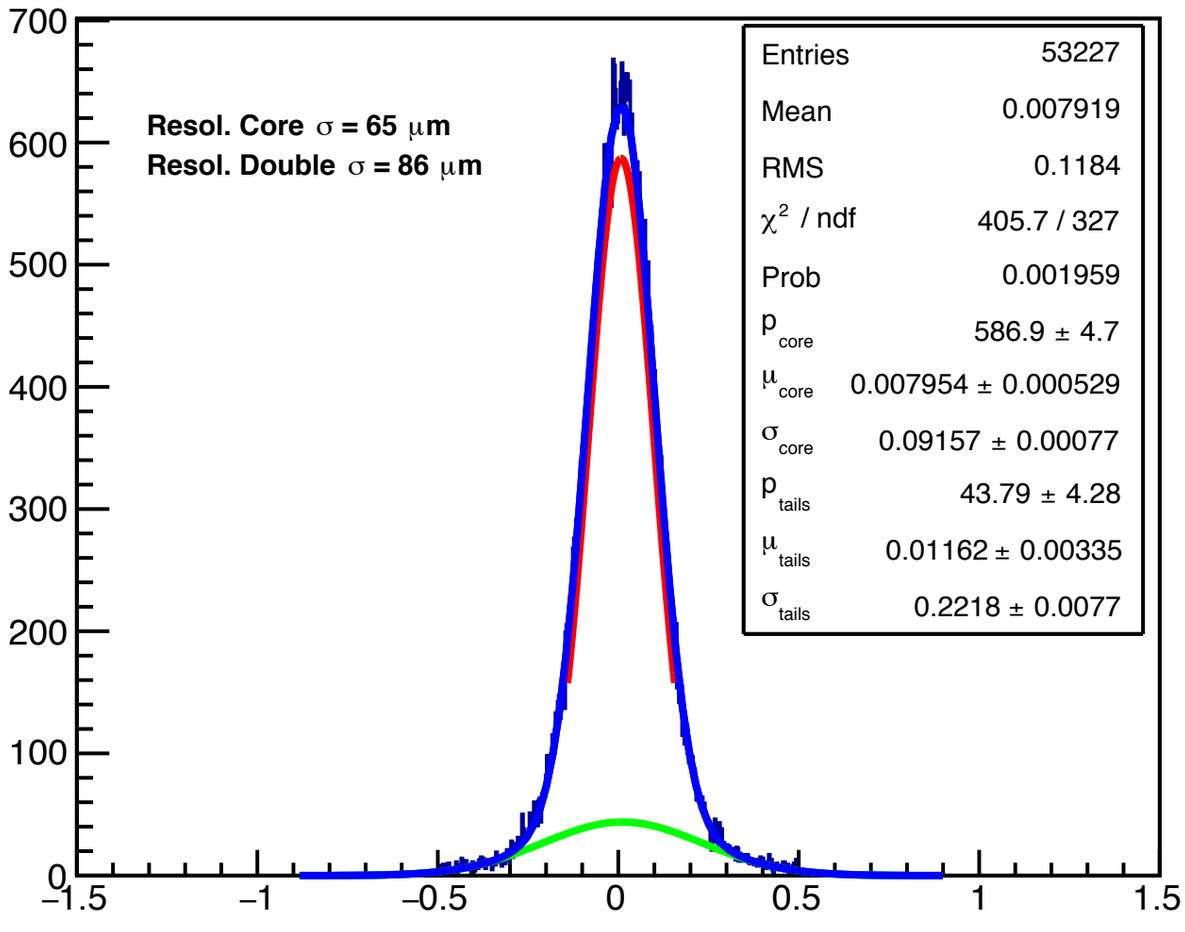
- After examining the Resolution across the detector we found out that the chambers where installed with a small angle in between them ~3mrad. Corrections have been applied.
- Centroid measurements show expected performance of the detectors with VMM3. We could easily achieve 50-60μm resolution. Further analysis can always teach us more but due to lack of time I believe going further is not needed for this study.
- Electronics gain calibration improved by few microns but not essential. Operating parameters must be defined !



Correction applied on the rotation

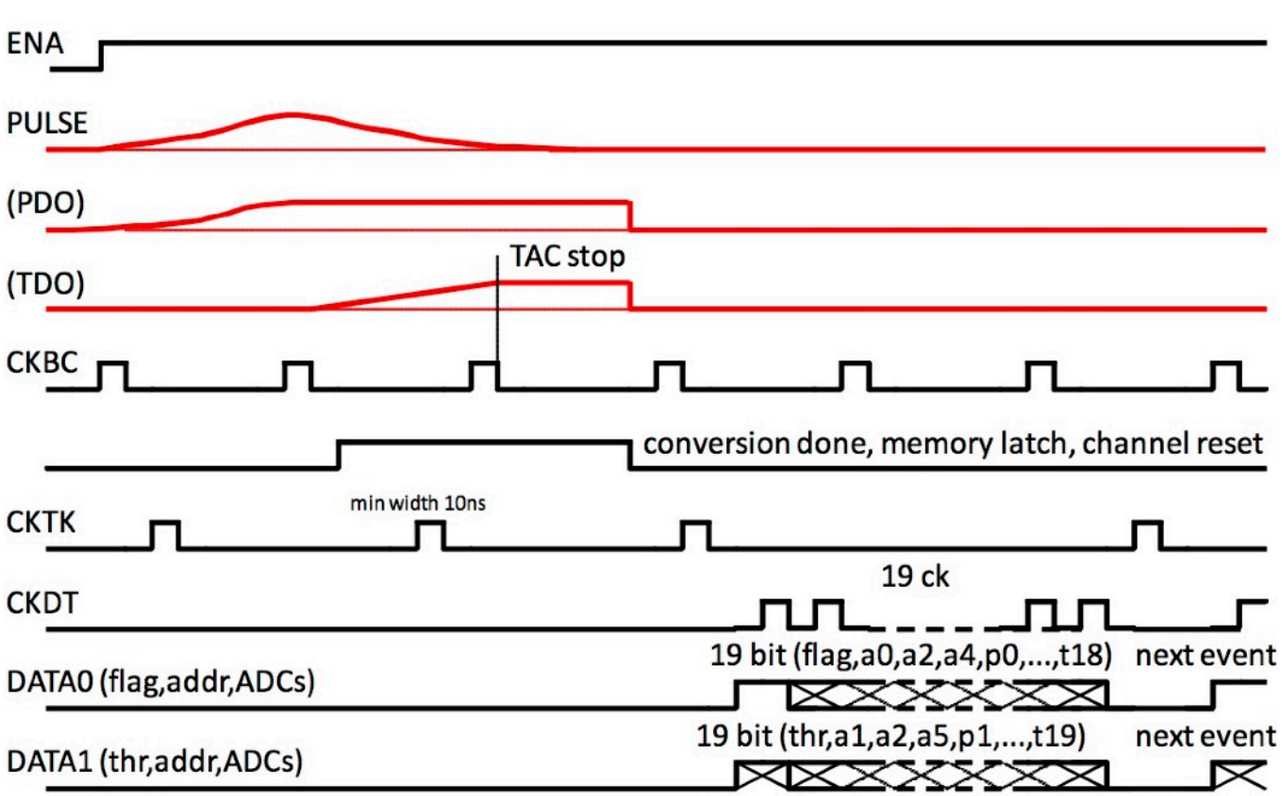


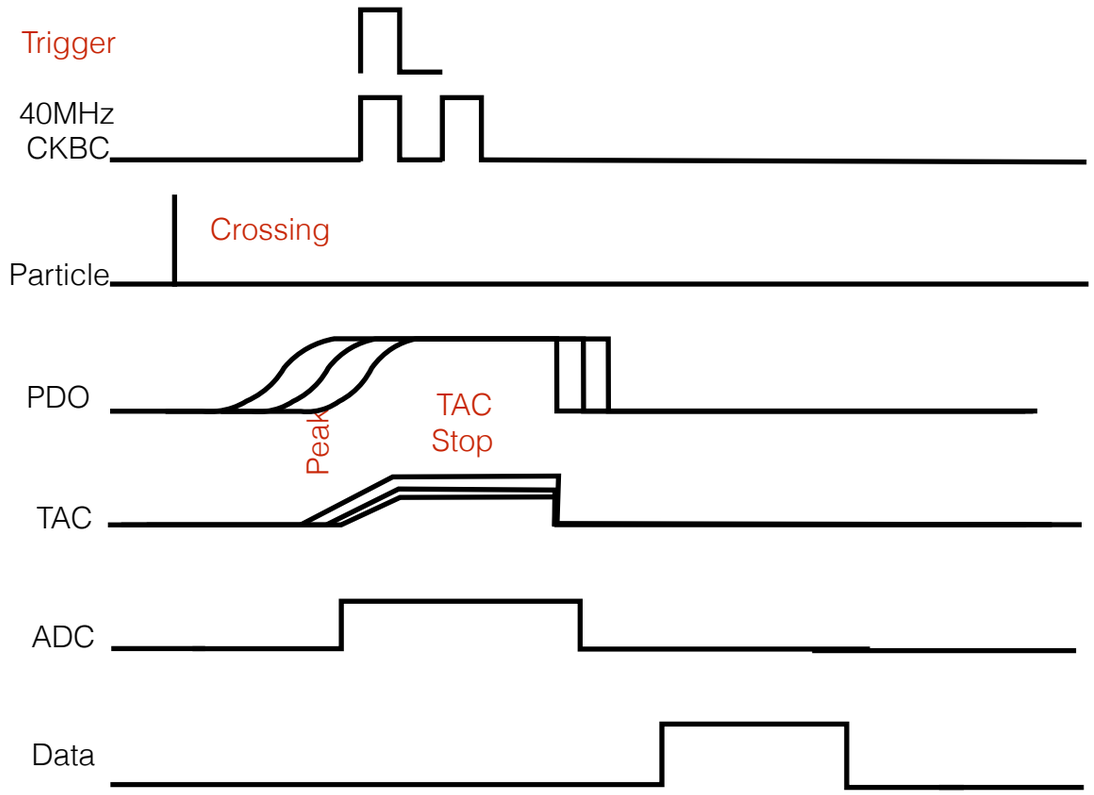
High hit efficiency



VMM - time measurements

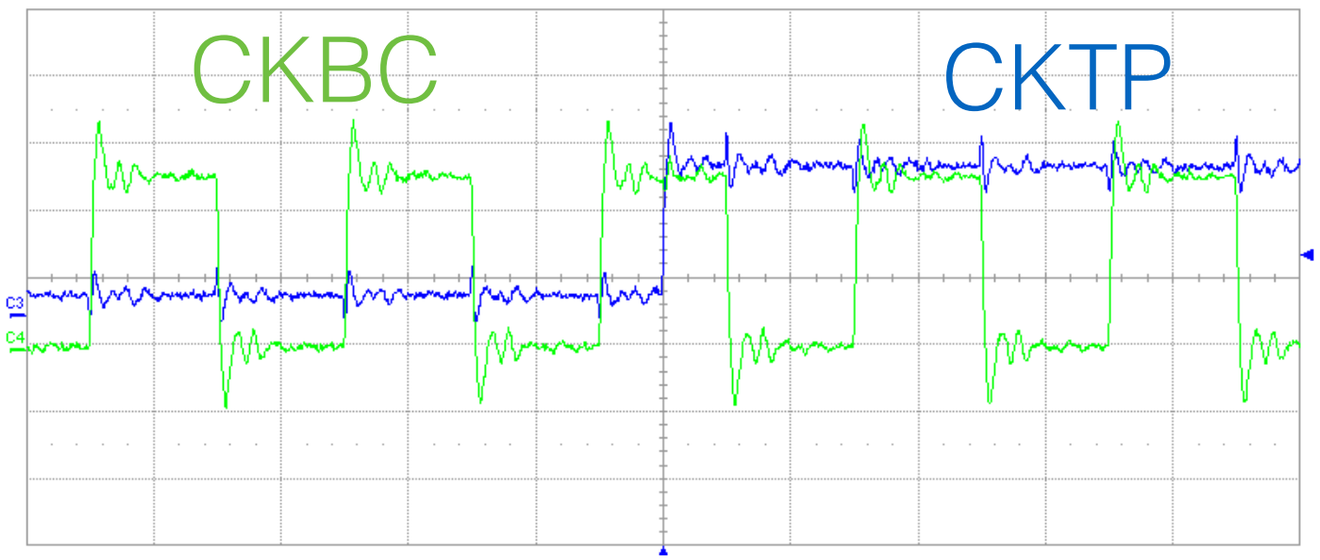
- VMM was designed for synchronous machines in principle. That means that the timing is difficult to be measured in a test beam environment. This results in jitter and uncertainties
- In VMM3 we foresee this need and we implemented the CKBC as a strobe and not as a clock.
- In addition we implemented the bit stcr with which the channel will reset if a stop signal is not occurred
- We developed a firmware to allow these kind of measurements
- The external trigger is controlling the CKBC (adjusted with 320MHz clock)
- This configuration allows to measure the drift time directly and eliminates the t0 jitter

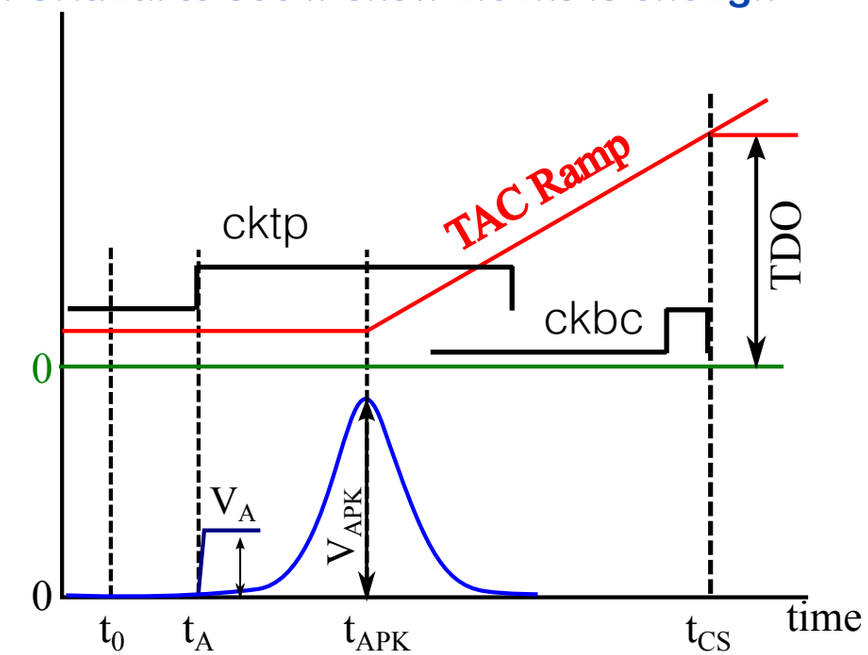


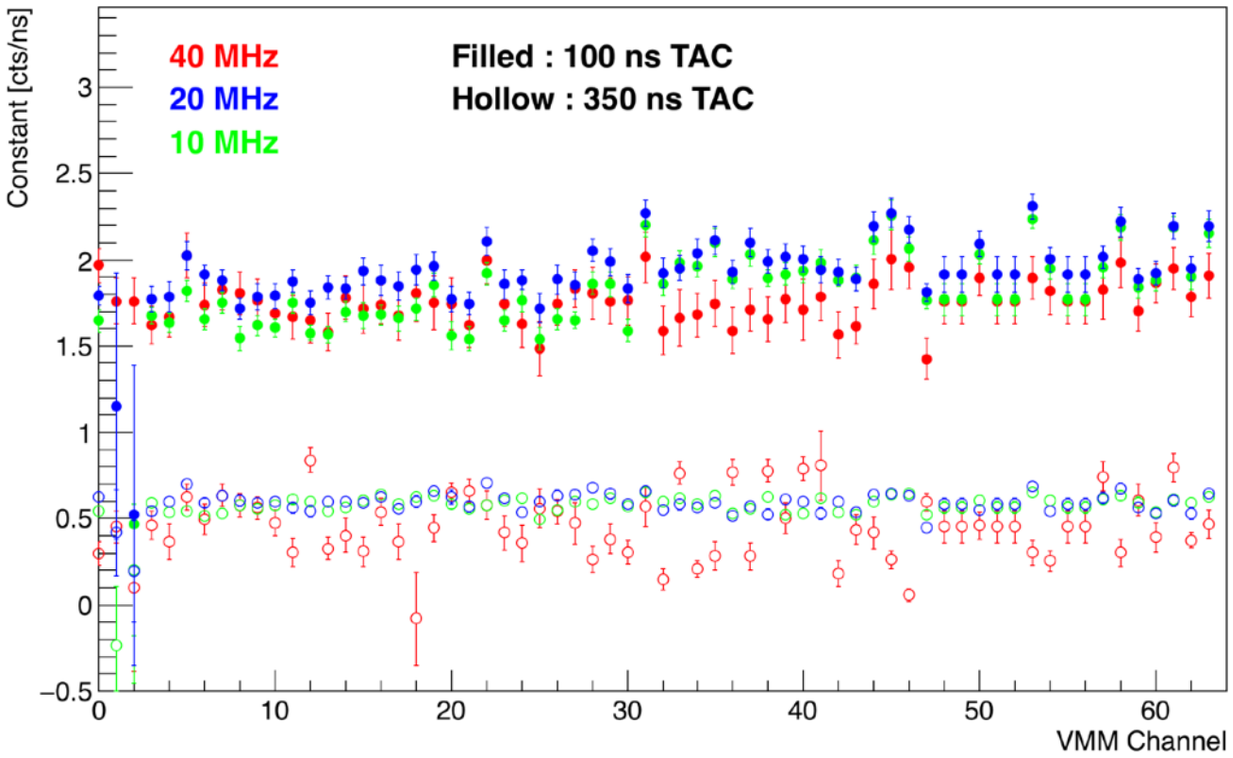


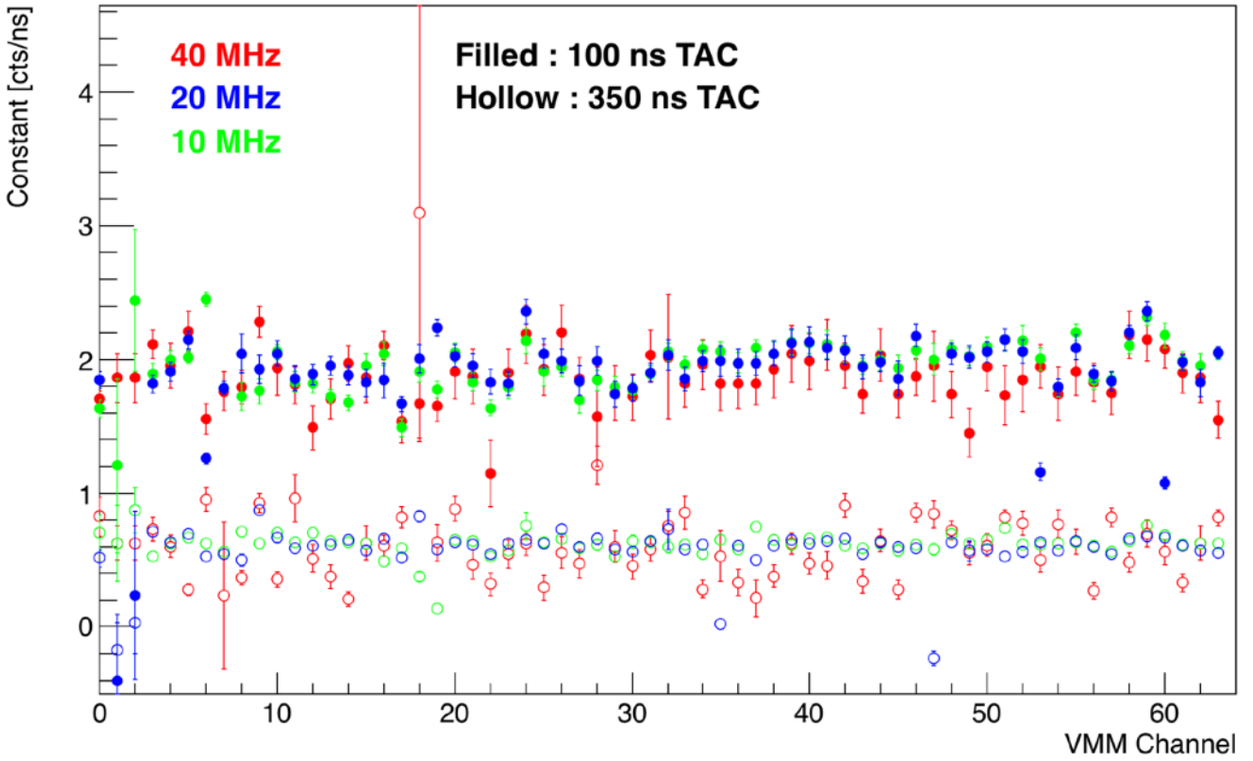
TAC calibration - Slopes

- Calibrate of the TAC for different ramps was automatically performed. Both skewing clocks method (NSW mode) and latency method (Not NSW) was used to extract the ramping rate and pedestal. Critical to see if skew clocks is enough



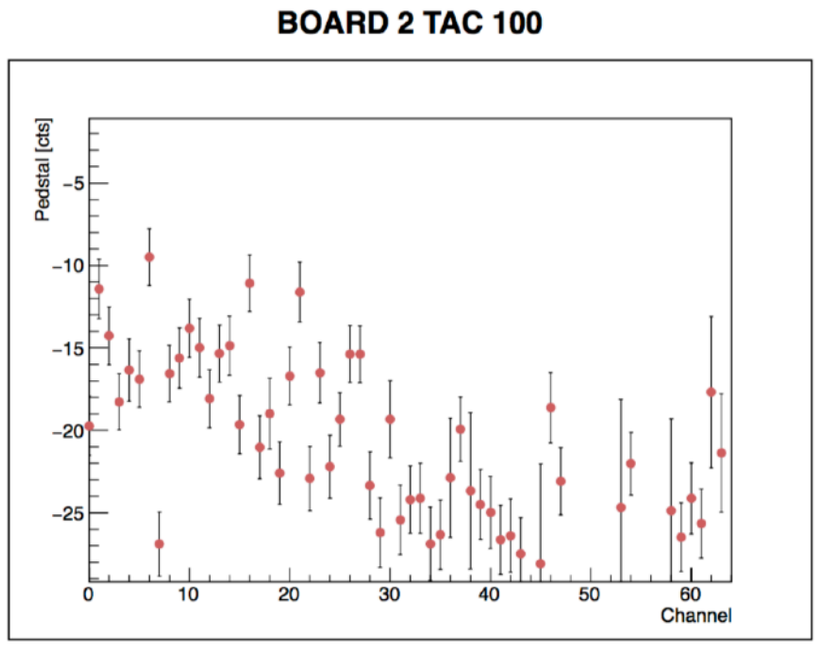


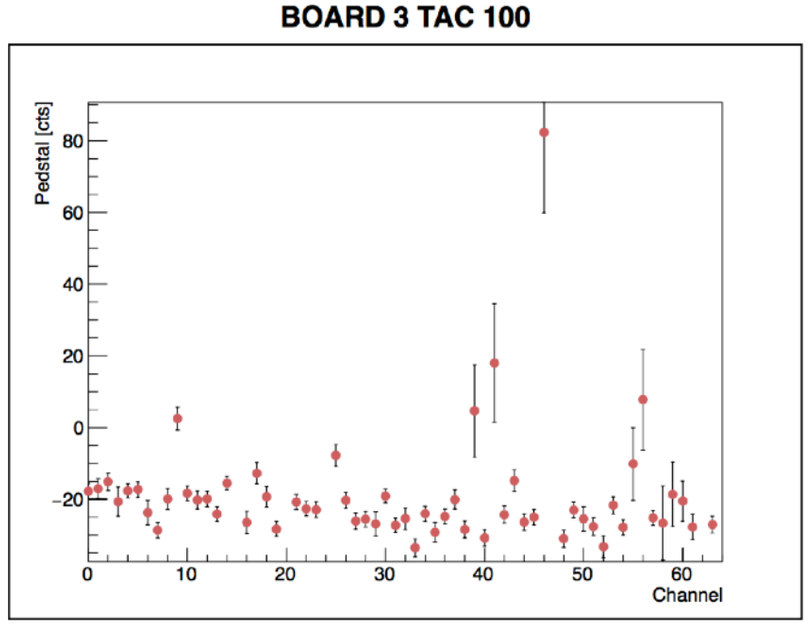


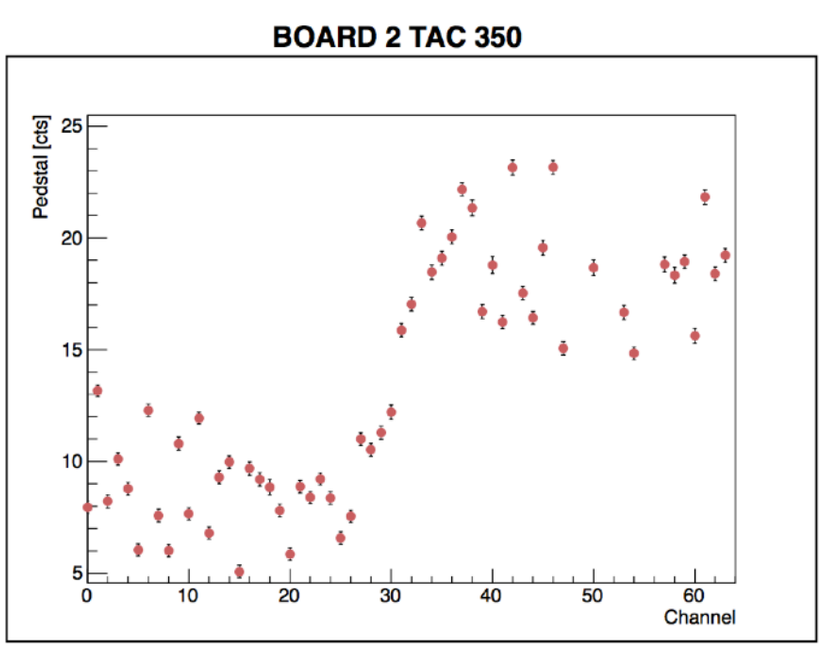


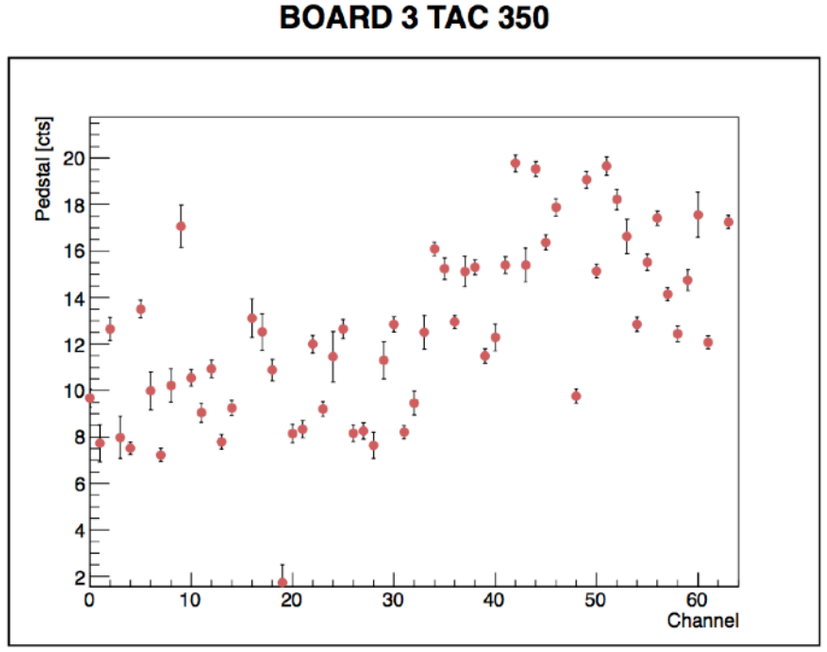
TAC calibration - Pedestal

- Channel pedestals were obtained by getting the intercept from a linear fit performed on the data. This may not be possible on NSW so good uniformity on the chip level is needed. VMM3 showed problems there but should be corrected in VMM3a.
- The pedestal for the analysis is just subtracted from each channel.



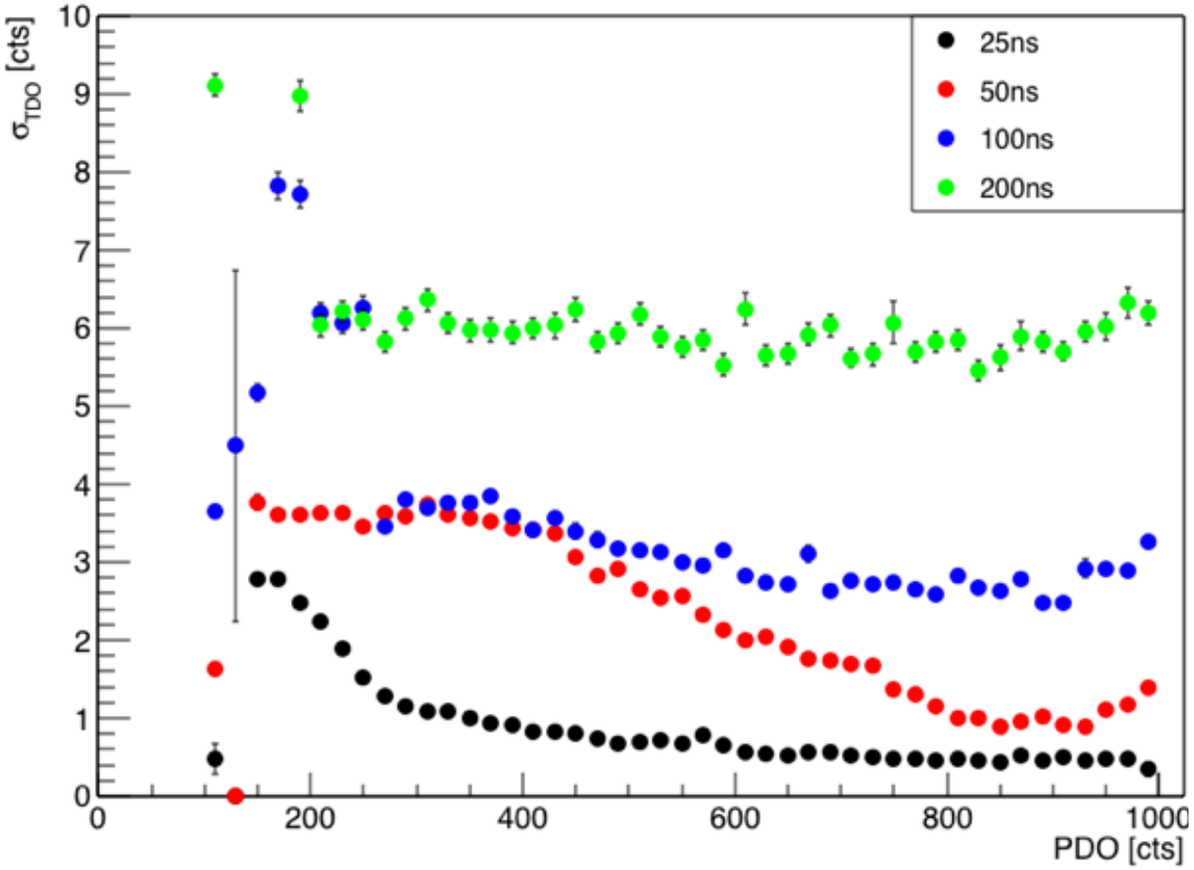


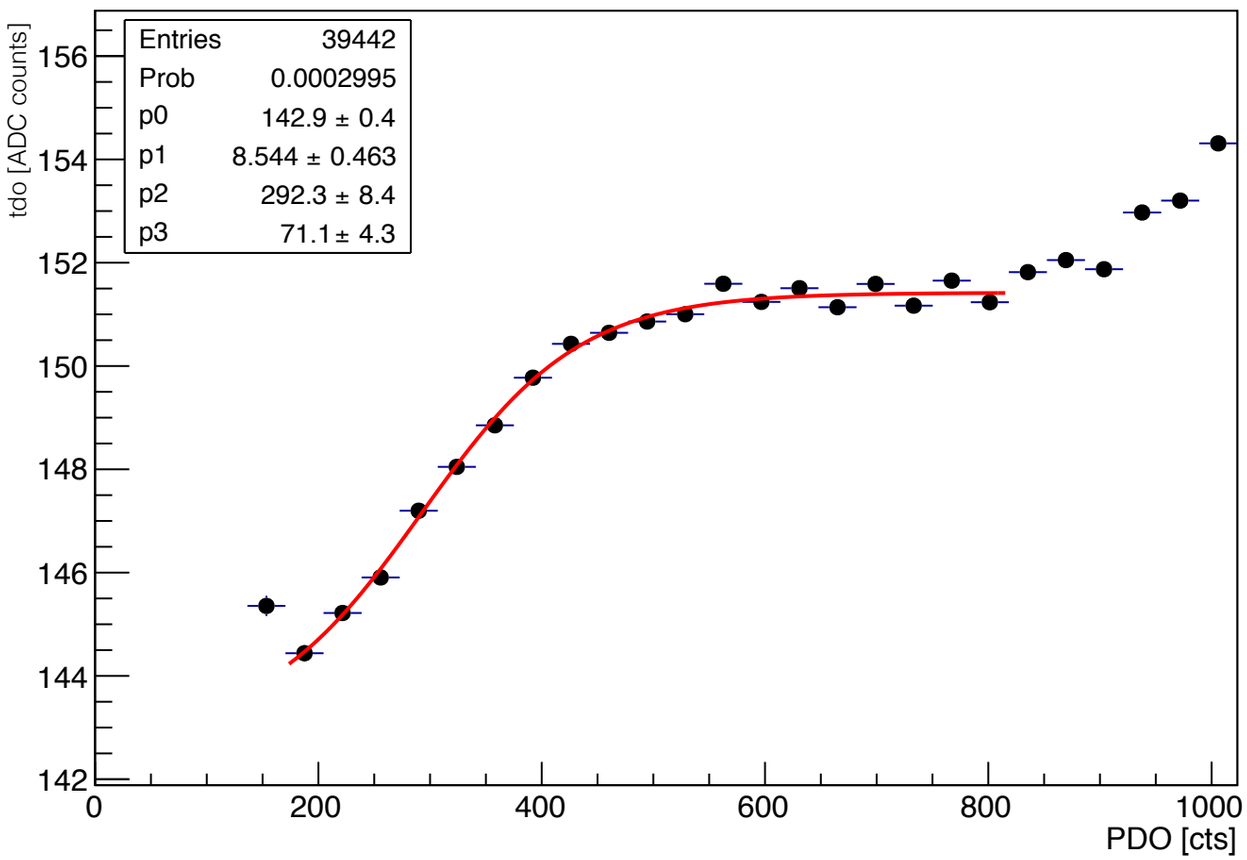




μTPC - timing resolution, time walk

- We have also examined and calibrated the following:
  - Timing resolution along amplitude: This is taking into account on the fitting of the event as an error. Other errors like the longitudinal diffusion is negligible with respect this.
  - Time walk: There is a dependance of the time finding (peak or threshold) from the signal amplitude. This is a correction applied on the timing reconstruction. Fitting the full distribution will improve more the results. To be done.

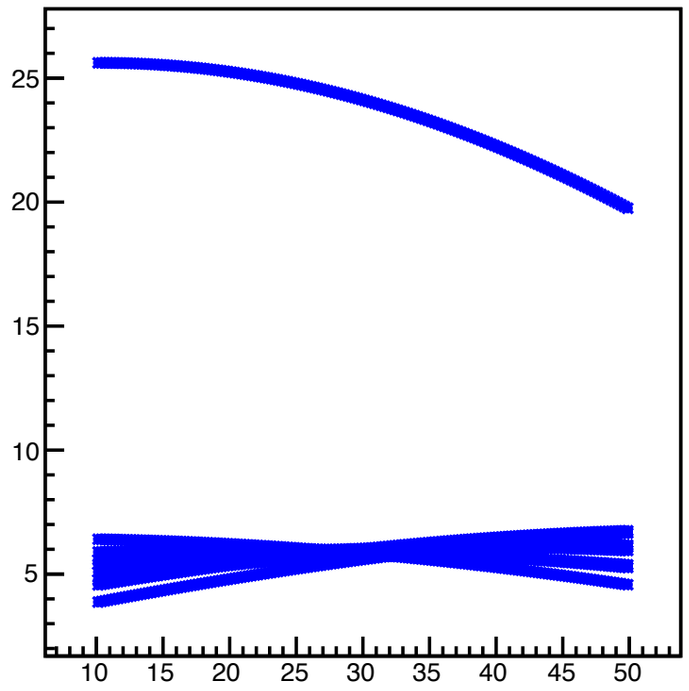




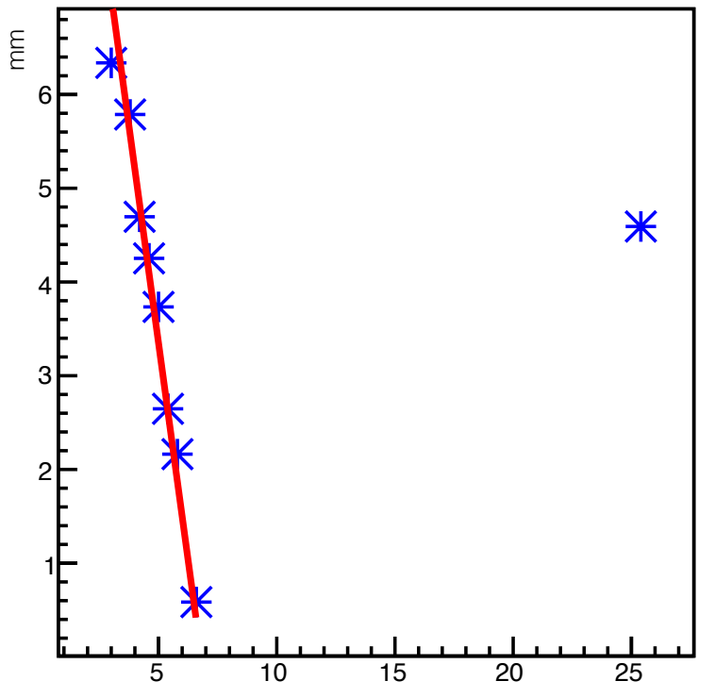
μTPC - Clustering

- The uTPC method is more complicated than the centroid since you can have holes in between strips that belong into a cluster due to ionisation fluctuations. Also noise and irrelevant hits may affect the reconstructions.
- To mitigate those we use a technique involving the Hough transform as a filter.
- Perform hough transform
- get the cross point and transform back the coordinates of the line
- Remove entries not belonging to this line (range over residuals)
- Perform linear fit (including errors on y according to timing errors and on x according to pitch)

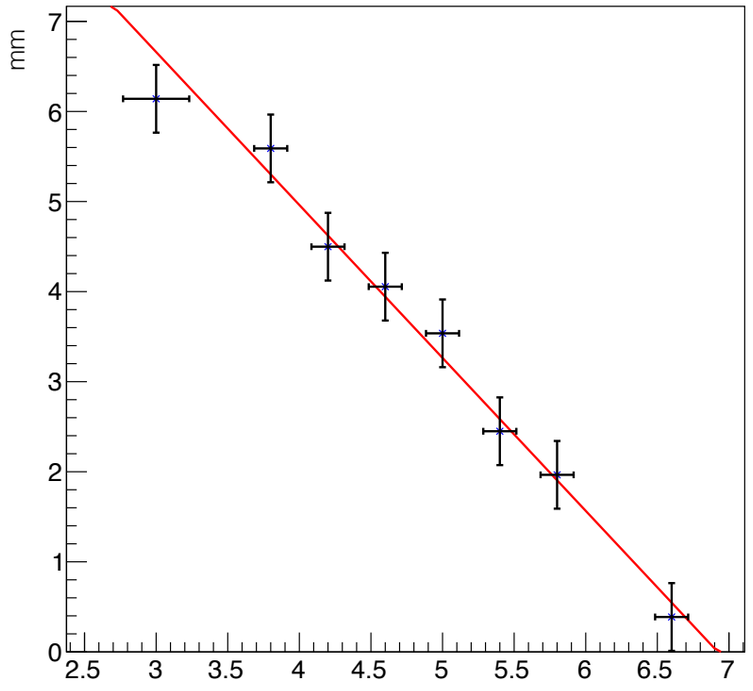
Hough Space



Hough line

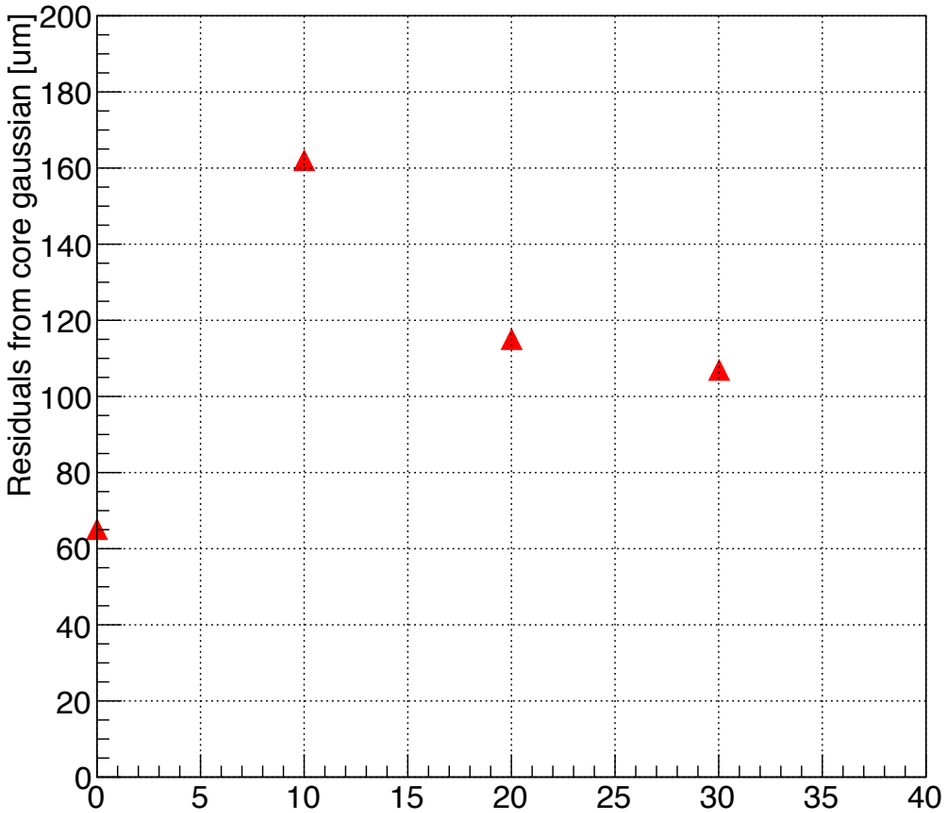


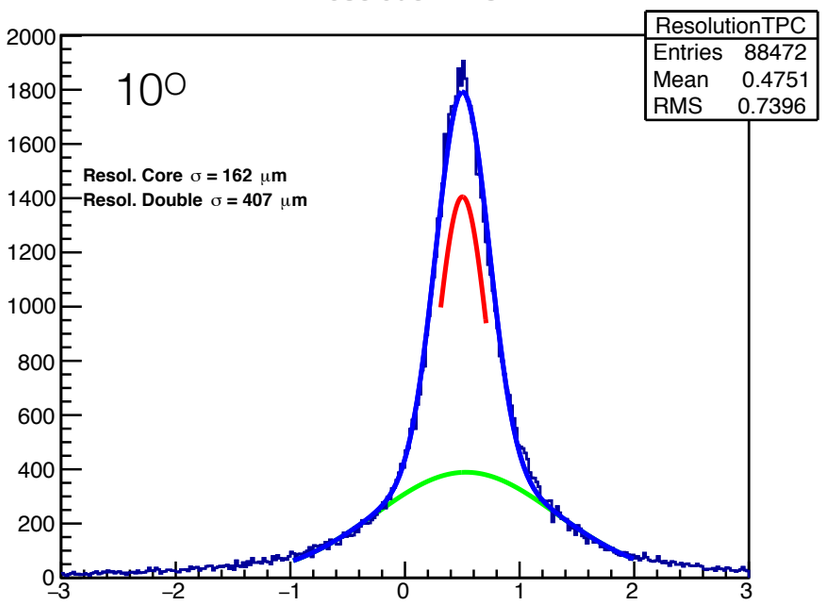
Linear fit after filter

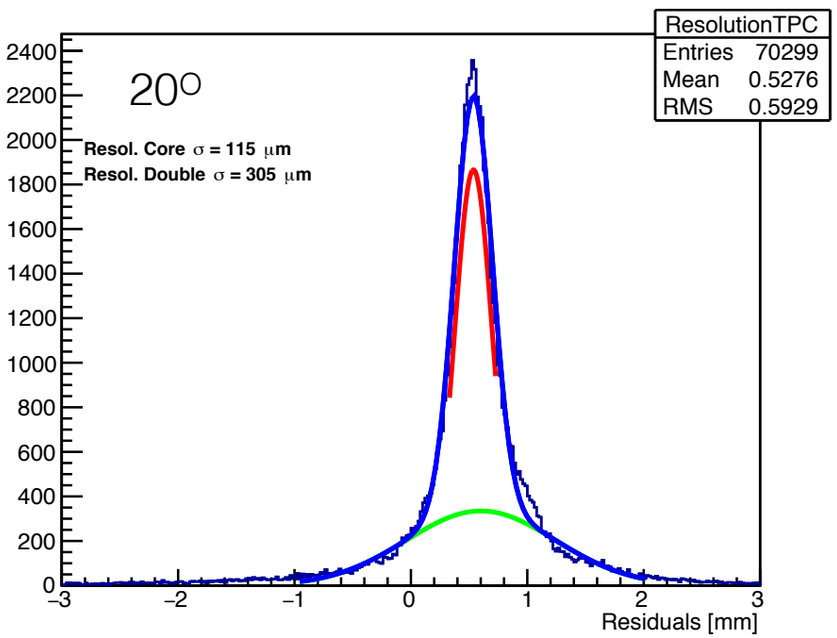


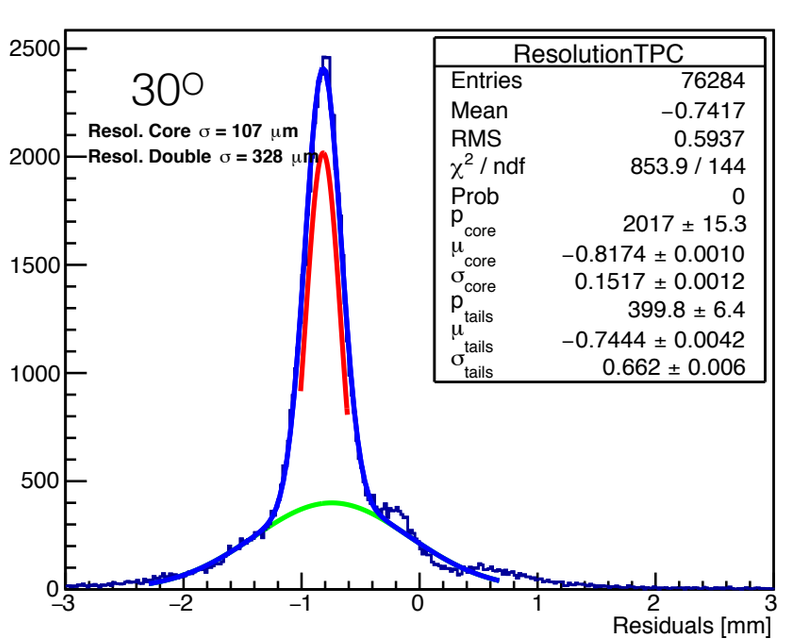
μTPC - Residuals

- Preliminary results show good performance. Results obtained with timing at peak, 100ns integration time, gain of 9mV/fC. The data were selected only on the centre of the detector to avoid mismatches with the geometrical acceptance of the scintillator trigger and avoid dead channels at the edge of the first VMM.
- There are certainly improvements to be made on the reconstruction since the distribution shows some shoulders that needs investigation. Error handling needs some validation
- That's the initial analysis and certainly more digging into the data is needed but due to lack of time that was not possible until now.



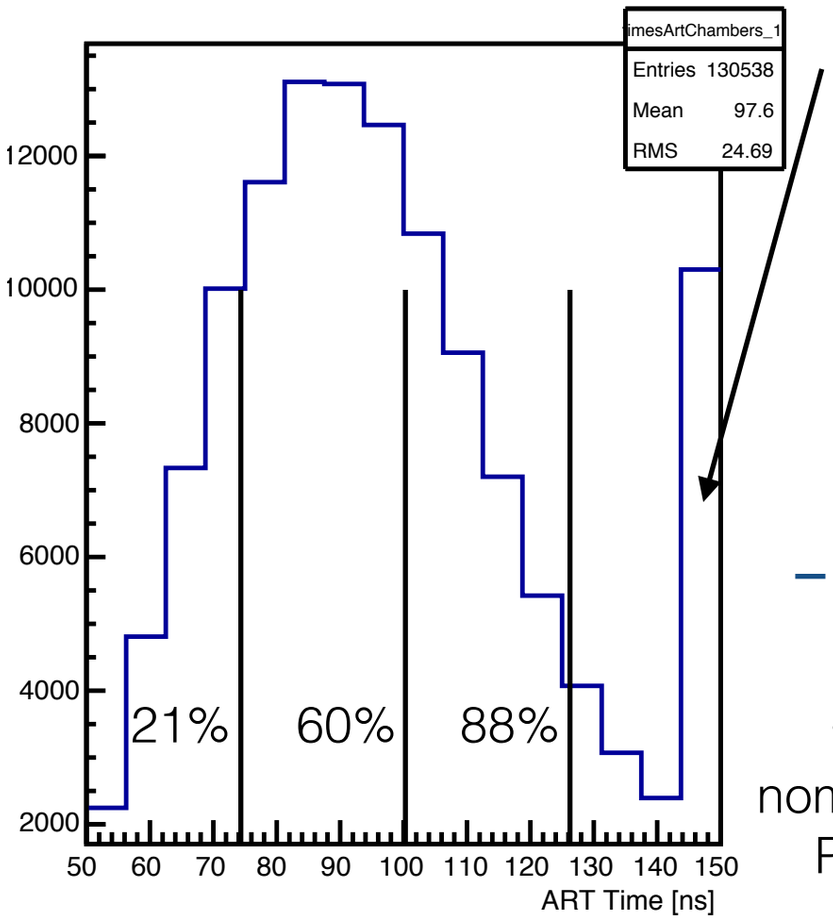




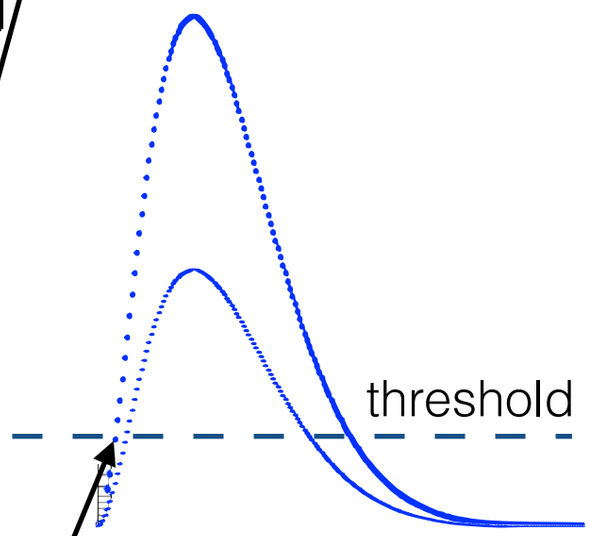


ART Measurements

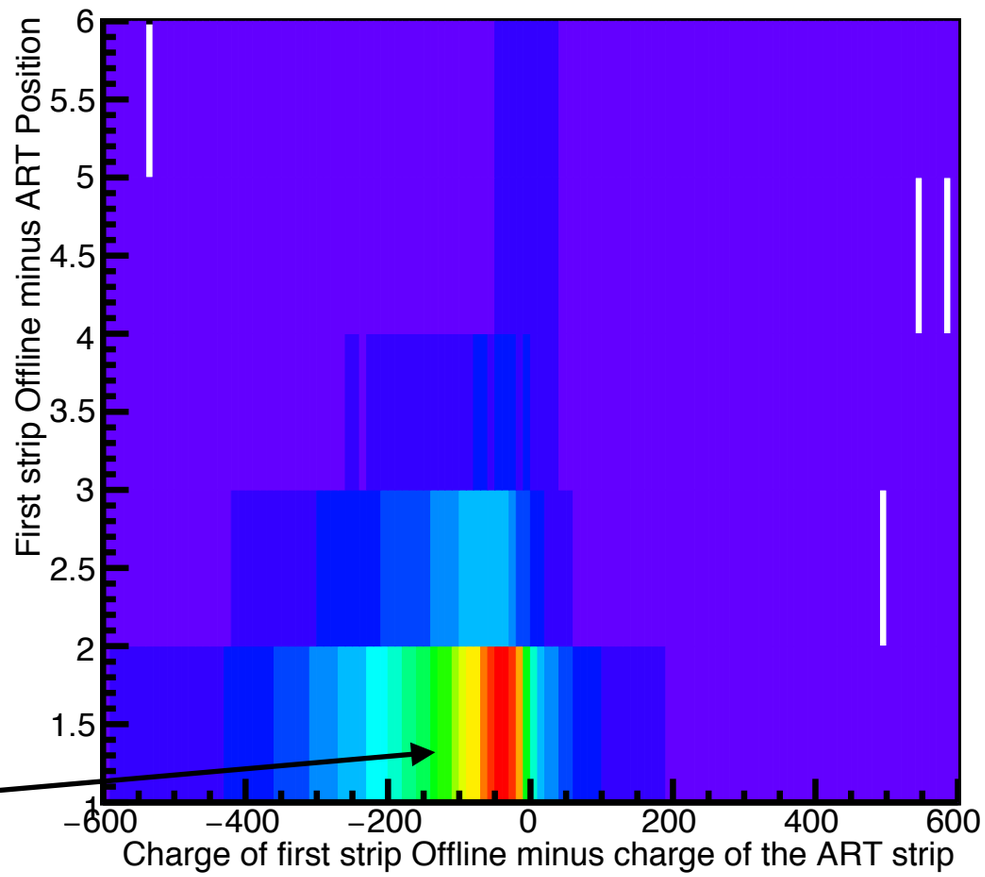
- We measured the ART in the following way:
  - The first ART is captured and a counter measures the time with a 160MHz clock
  - If an external trigger occurs, the ART is kept otherwise is discarded
  - Measuring the ART at threshold maybe not the best idea since there is significant time walk ~10ns and even worse due to the dependance of the charge, the choice of ART may vary up to 5 strips as seen from the data. This may create some bias in the data.
  - A timing window of 3 BCs (88%) may be sufficient for the Micromegas trigger.
  - Unfortunately due to design of the firmware and limited time when realised at the testbeam no data of which someone can draw conclusion were acquired.



Overflows due to external trigger



time walk at threshold nominates the ART selection
Peak has smaller effect



VMM3a

VMM3a - Bug fixing

- Although the VMM3 performance was good enough we decided to produce another version
- VMM3a incorporates all the noticed bugs and includes not other functionality but only fixes and improvements. The only change affecting the FPGA boards is the data line swapping on the pinout - easy implementation on fw.
- This is only a small summary list, much more were fixed related to these issues.

Fix		Detail	Simulation Result
ADC	linearity	• filtering of ADC bias lines ✓	• substantially improved linearity
	yield	• corrected warm-up mirror mismatch • strongly improved bias matching (all ADCs) ✓	• resolved ADC yield issue • strongly improved gain and saturation uniformity
Baseline	stlc	• resolved potential Antenna ratio issue • increased currents in stabilizer ✓	• resolved high-baseline yield issue
	yield	• optimized bias in second-stage driver • optimized size in third-stage driver ✓	• resolved failing/non-efficient yield issue
SFM		• added programmable currents for yield in SFM mode • added full-mirror to third stage • added programmable very-high-current handling ✓	• no external resistor needed for channel yield • strongly improved sTGC currents handling • fully compatible with VMM3 and π-networks
Trim DAC		• optimized driver size in trimming amplifier • improved matching in trim current source ✓	• resolved limited range issue • strongly improved trimming uniformity
Reset and Startup		• merged reset paths merged in local discriminator • added reset to soft-reset register • added reset to stop register ✓	• properly generated soft-reset at ENA-low • no locking with any configuration • no sequence or configuration required at start-up

VMM3a - Status and production plans

- NSW ASICs Final Design Review was held on 6th of September with approval of the ASIC submission
- The VMM3a was submitted in October 2017 through a dedicated engineering run with a turnaround time of ~10 weeks. (VMM3 received indeed in 10 weeks, VMM2 in 13 weeks).
- We expect VMM3a, along with other ATLAS ASIC dies to be delivered early January 2018 due a small delay with MOSIS.
- We submitted 6 + 25 = 31 wafers: 7 for small chips and 24 wafers for VMM3a. We'll get around 2.7k VMM3a
- Package quickly a small number of VMM3a (400) for testing During January-February.
- We envision testing of 4-5 weeks according to a detailed plan produced. Testing will be performed on bench, Micromegas, sTGC. Yield test are also scheduled the same time. Of course if no issues arise !
- NSW needs more VMM3a to start the FE production but we only get ~2.7k VMM3a from those wafers.
- Therefore ATLAS took the risk and ordered 25% of final number now, before checks are done through a pre-production submission done in November 2018 with a turnaround of 20 weeks.
- That will produce more ~11k VMM3a enough for the NSW detector assembly planned for summer 2018.
- Dicing and packaging will be done through Novapack.
- Once the tests are convincing we go through Production Readiness Review on March 2018.
- The full VMM3a production will be submitted by April 2018 where it's wise for others to join at the same time.