

# Status Update on the VMM3

Investigation of the Cooling Requirements

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RD51 Mini Week, 14 DEC 2017

# Motivation of the “VMM cooling project”

# Motivation

- Manual: “[...] cooling of the VMM chips is mandatory.”

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Table 2: VMM Power Supply Requirements

Supply	Voltage[V]	Ripple	Max Current [mA]
Vddp	1.2 ± 5%	< 10 μV rms , 1-10 MHz	150
Vdd	1.2 ± 5%	< 100 μV rms , 1-10 MHz	400
Vddad	1.2 ± 5%	< 100 μV rms , 1-10 MHz	200
Vddd	1.2 ± 5%	< 1 mV rms, 1-10 MHz	150

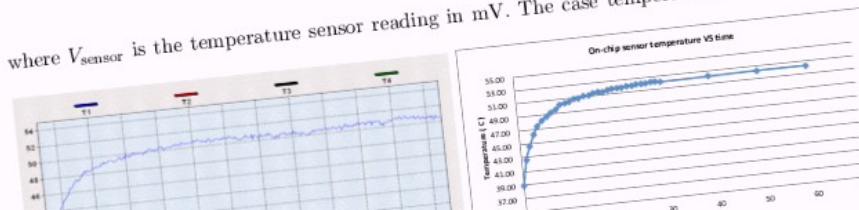
## 8 Cooling

As mentioned already the VMM power dissipation depends on the features used with a maximum of ~ 1 W . Although not excessive, enclosed in a Faraday cage in the high density environment of the NSW (especially in the case of Micromegas detectors), **cooling of the VMM chips is mandatory.** A system with water as coolant is being designed by the teams working on the detectors.

The IBM CMOS8RF Design Manual specifies the operating temperature range to be from -55 °C to 125 °C. However device life time degrades rapidly at high temperatures. The case temperature should be kept below 50°C and preferably in the range 30-40 and should be verified and compared to the junction temperature provided by the VMM ASIC. The VMM includes a temperature sensor which can be read out by appropriately programming the monitor output and digitized by the SCA setting (in configuration mode) scmX = 0, sm5-sm0 = 000100 (see Table 6). The die temperature is approximately given by:

$$^{\circ}\text{C} = \frac{725 - V_{\text{sensor}}}{1.85}$$

where  $V_{\text{sensor}}$  is the temperature sensor reading in mV. The case temperature of a single-chip



# Motivation

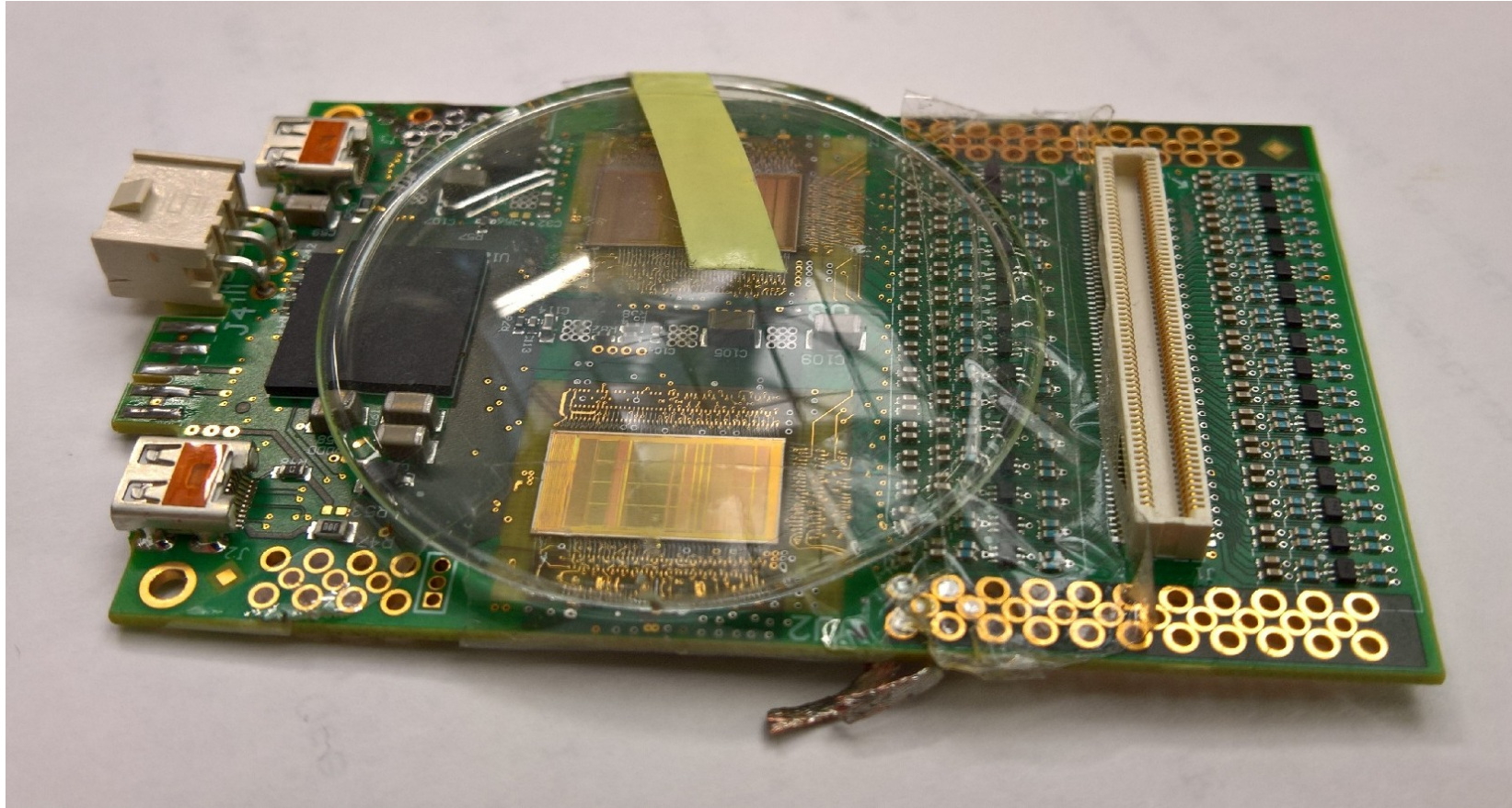
- Manual: “[...] cooling of the VMM chips is mandatory.”
- ATLAS uses water cooling
- GDD/ESS/RD51: Other kind of implementation
  - VMM still consumes about 2 W of power

Is water/active cooling required? Is passive cooling sufficient?

- Investigate performance of the VMM depending on the temperature
  - Create test set-up and perform measurements
- Why this effort?
  - NMX Experiment has movable detectors
  - Neutrons scatter on hydrogen
  - Passive much simpler; easier to adapt for others

# GDD/ESS/RD51 Implementation

- Replace APV25 cards with VMM hybrid:

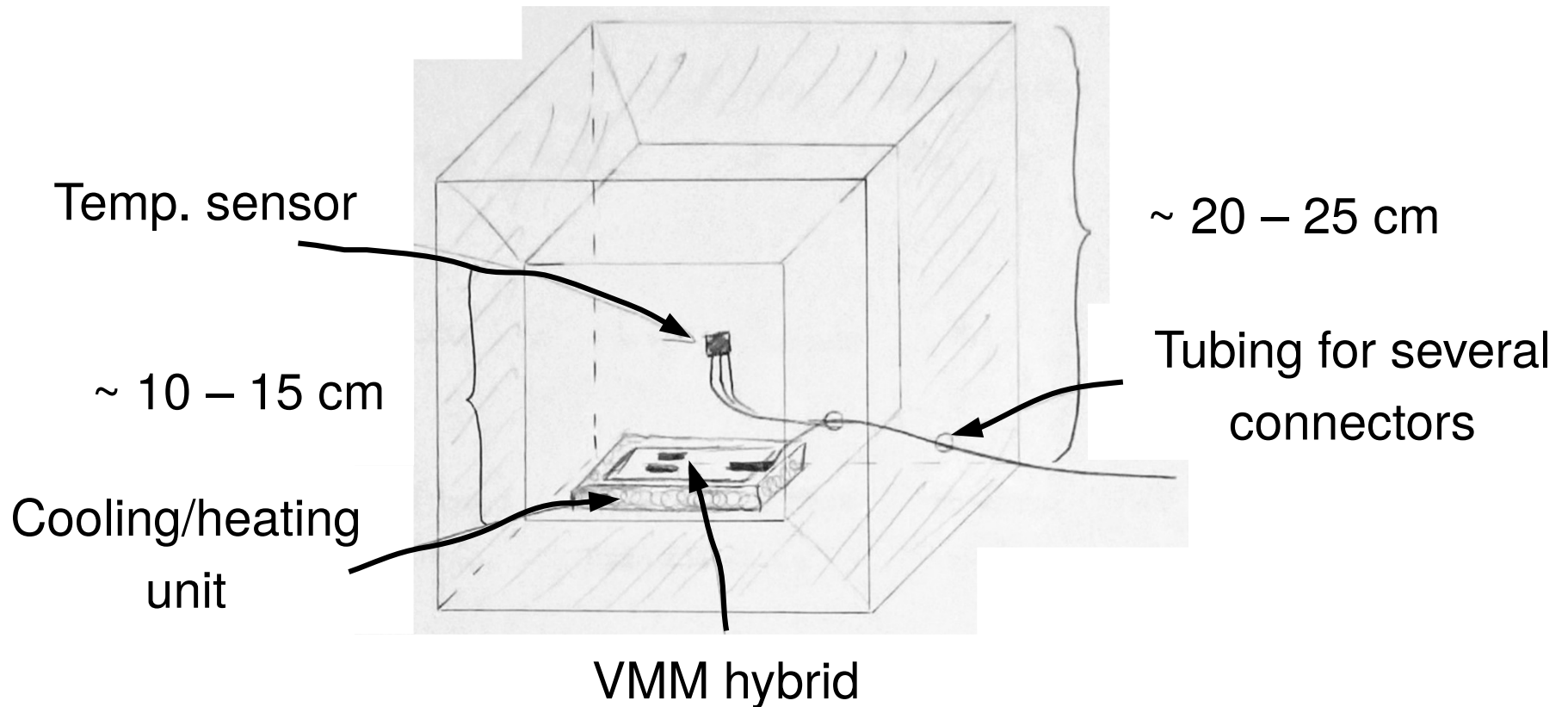


- For more details: See talks from Michael and Hans
- Build test set-up for hybrids

# Design & Assembly of the Test Set-Up

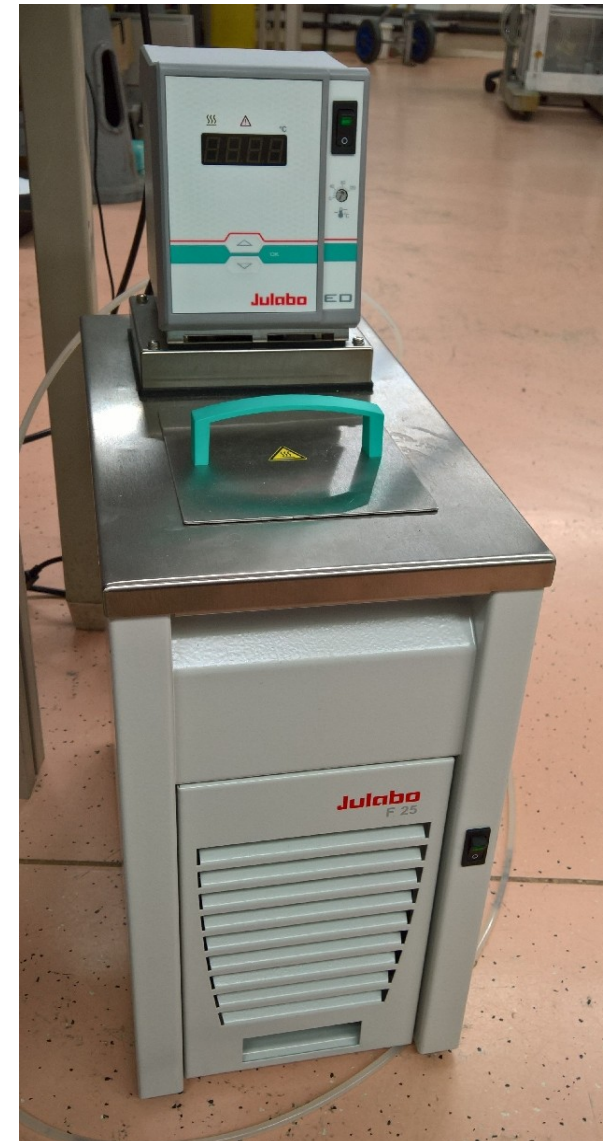
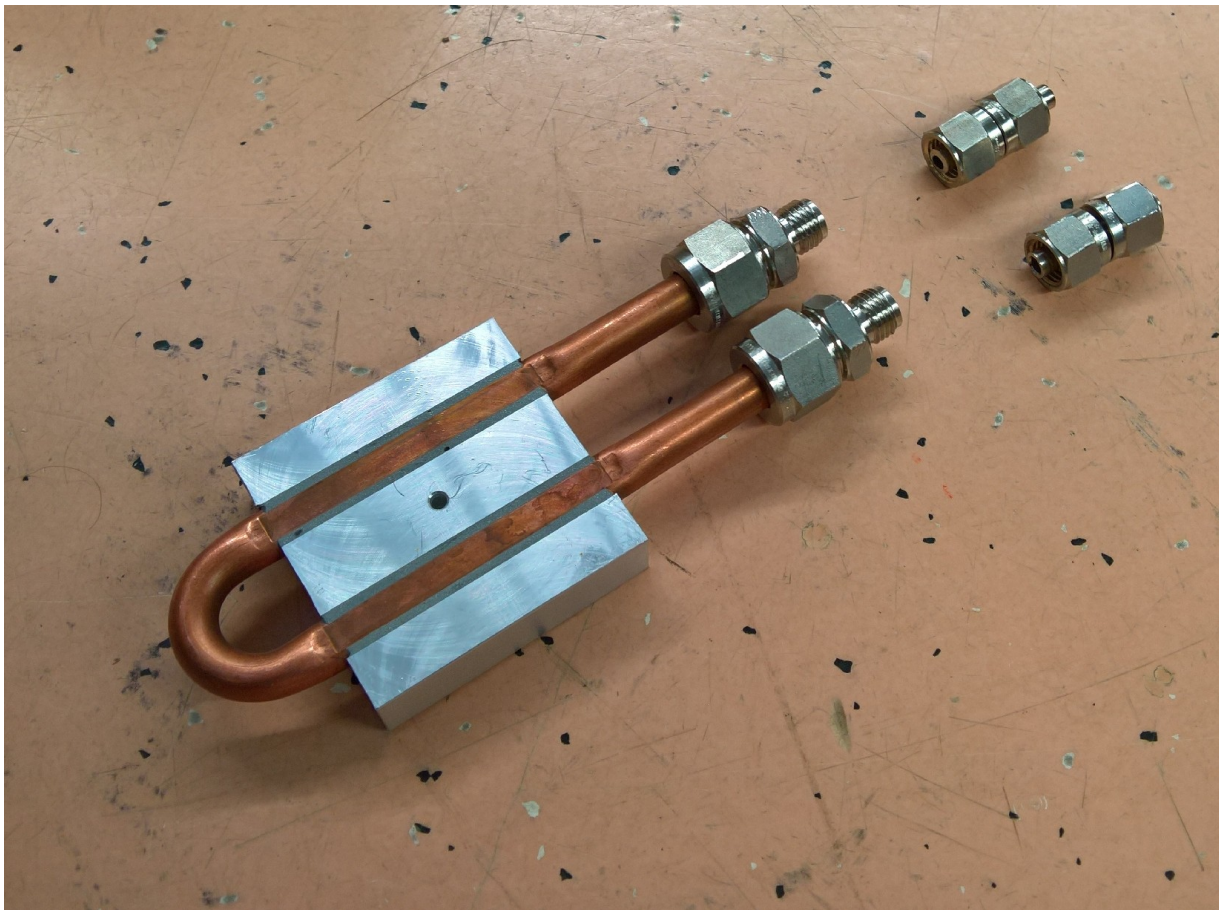
# Design of the Test Set-Up

- First attempt...



# Assembly Process

- Key component: Aavid Hi-Contact™ 2-Pass Cold Plate
- In combination with: Julabo FN25-ED





# Assembly Process

- For test set-up a good heat distribution is needed  
→ Use copper plates and thermally conductive paste



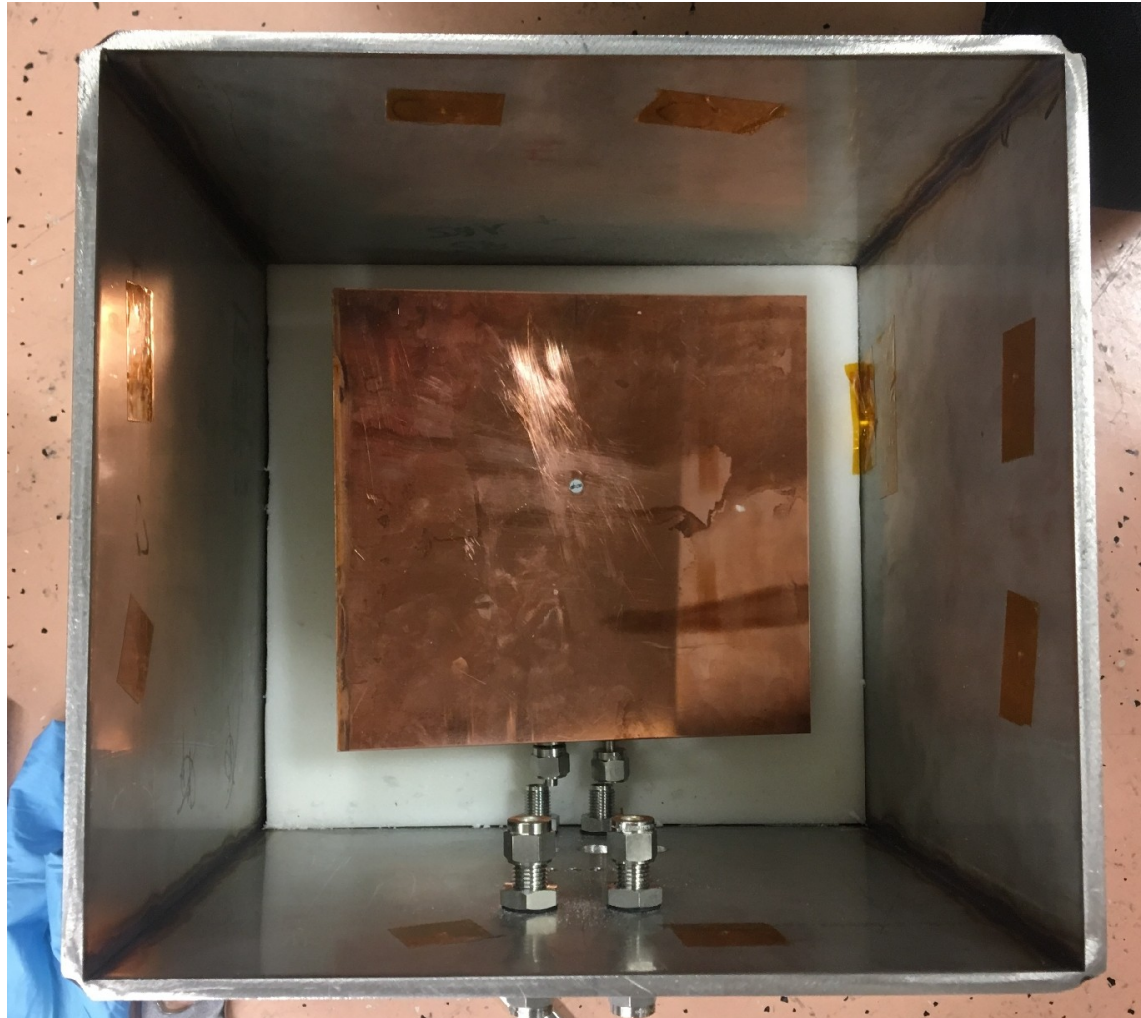
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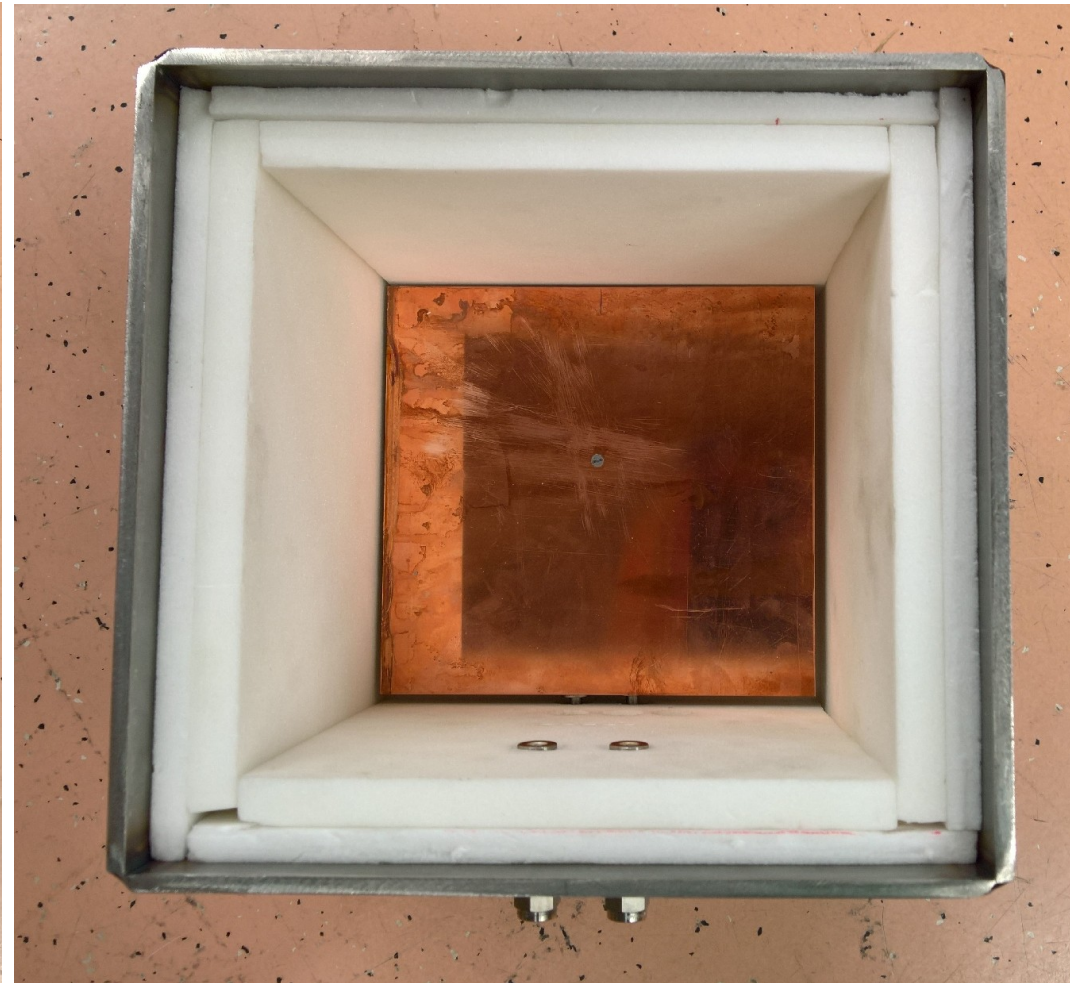
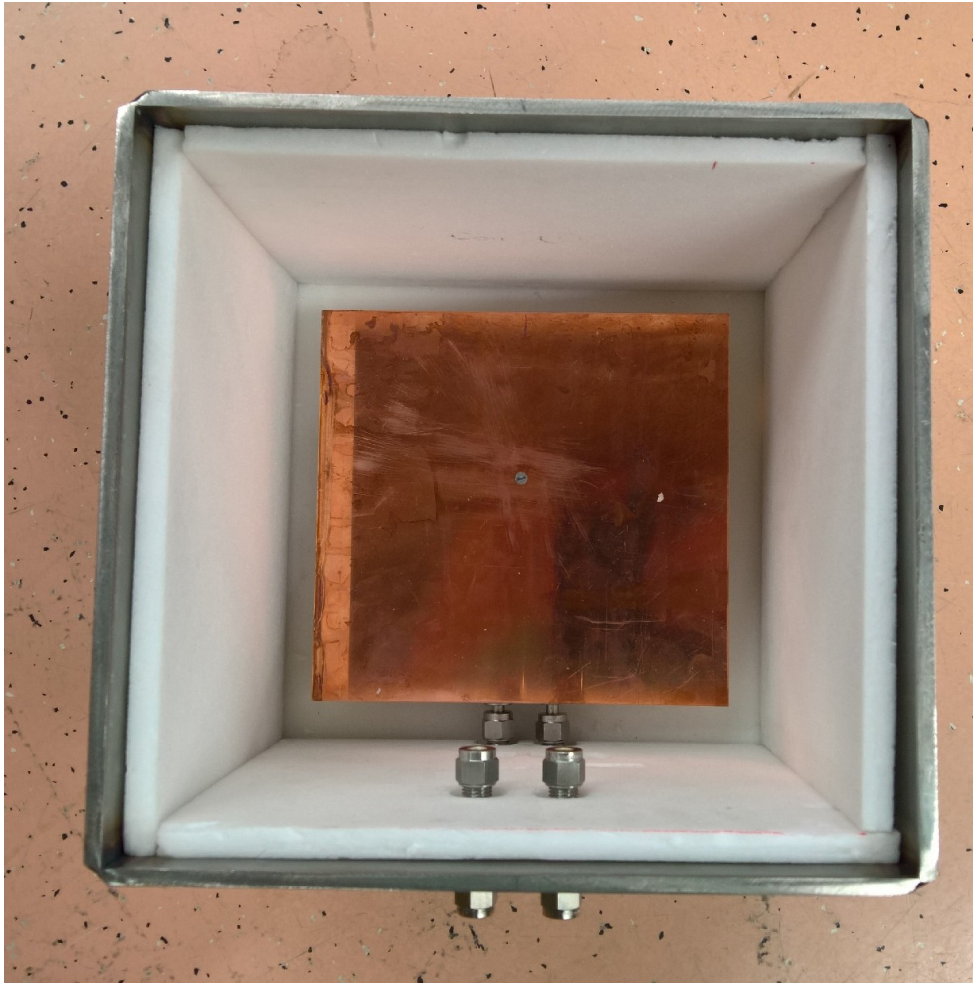
# Assembly Process

- Fit everything into box (little test environment) to protect from variations of conditions outside:



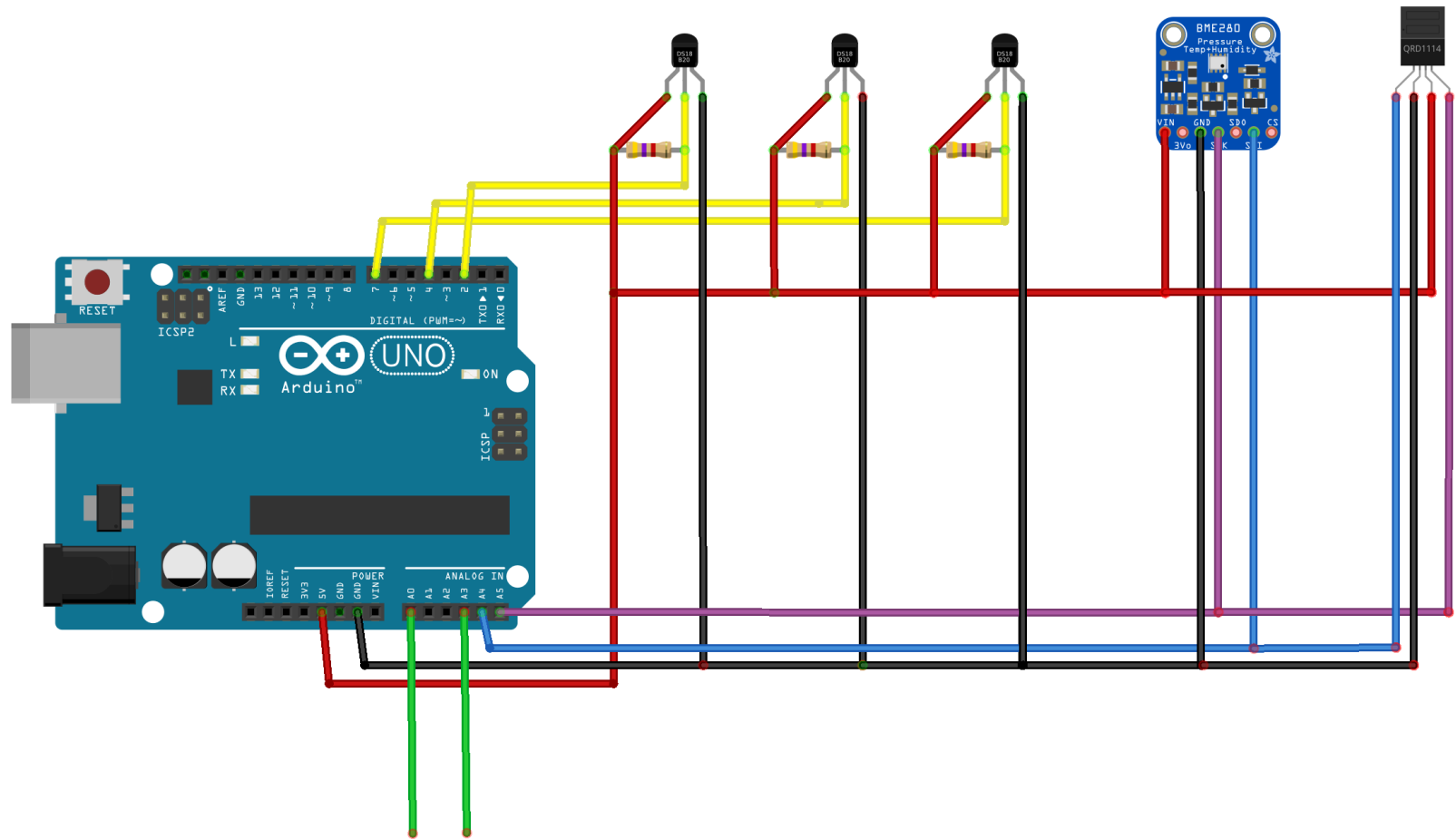
# Assembly Process

- Build even more controlled/stabilised environment  
→ Use insulating material (polyurethane)



# Electronics Assembly

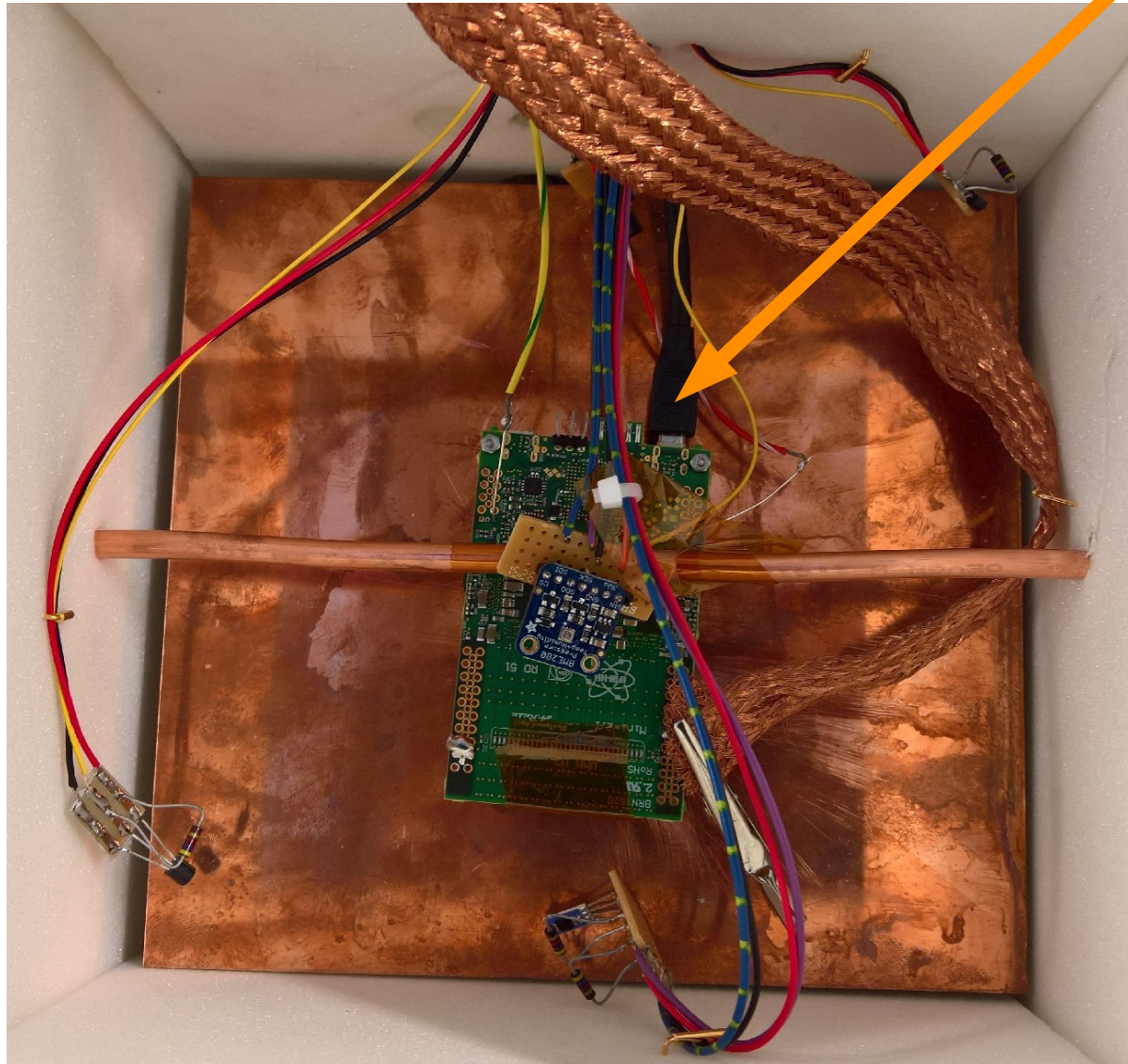
- Mechanical set-up done  
→ Move on to measurement circuit



fritzing

# Electronics Assembly

- Positions of sensors in box



HDMI: Power  
& Readout  
of VMM

# Electronics Assembly

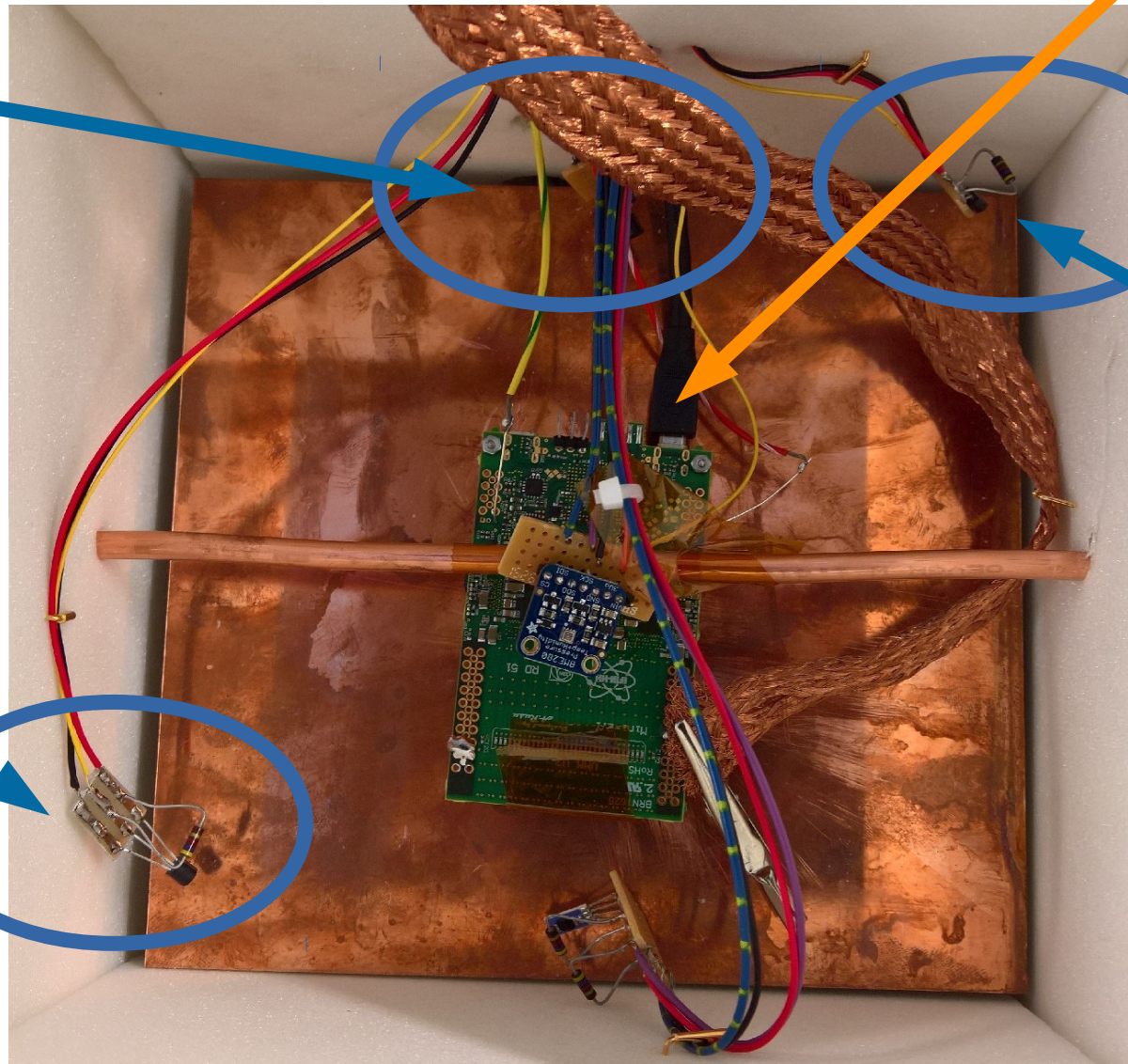
- Positions of sensors in box

DS18B20

HDMI: Power  
& Readout  
of VMM

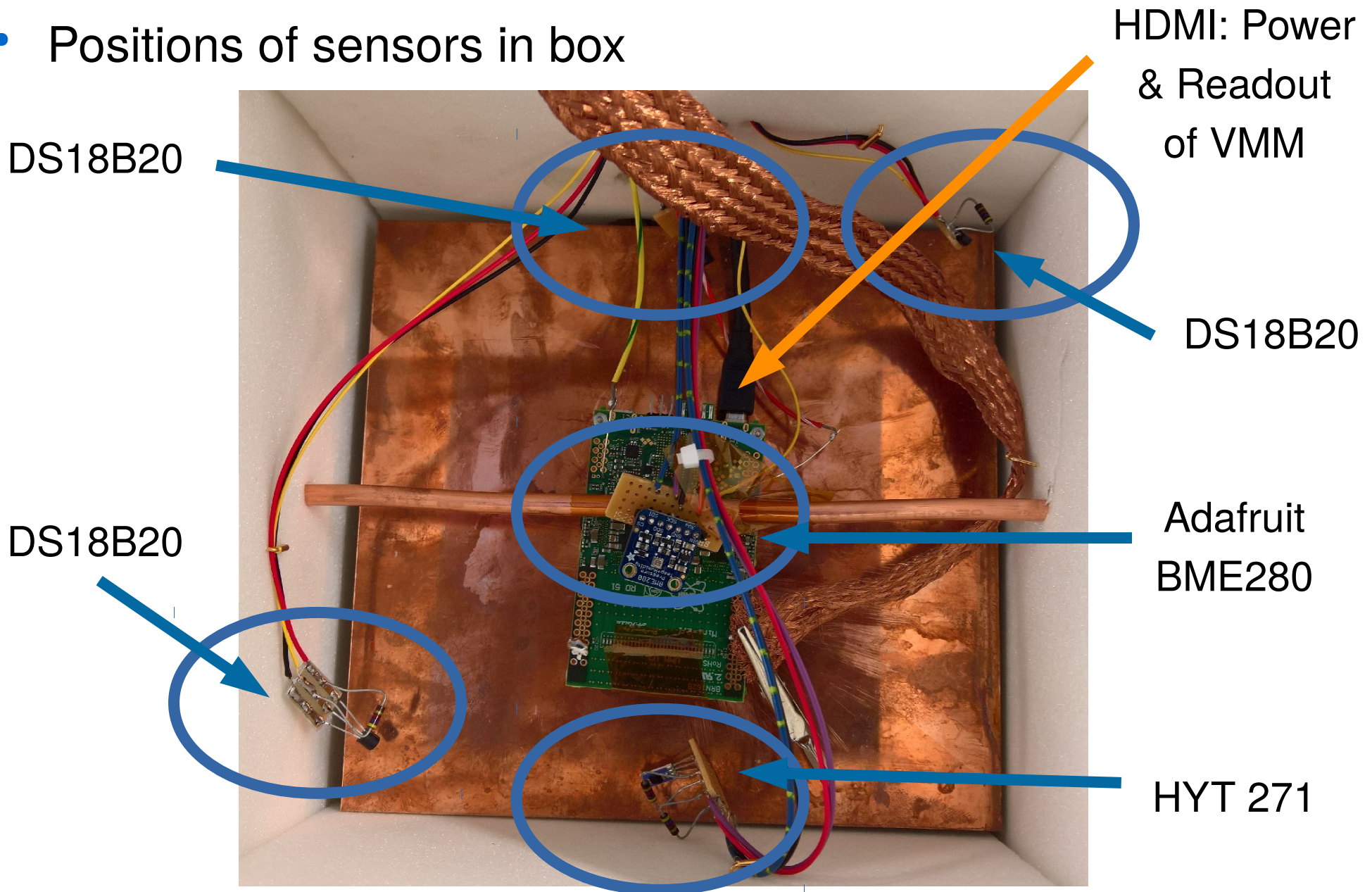
DS18B20

DS18B20



# Electronics Assembly

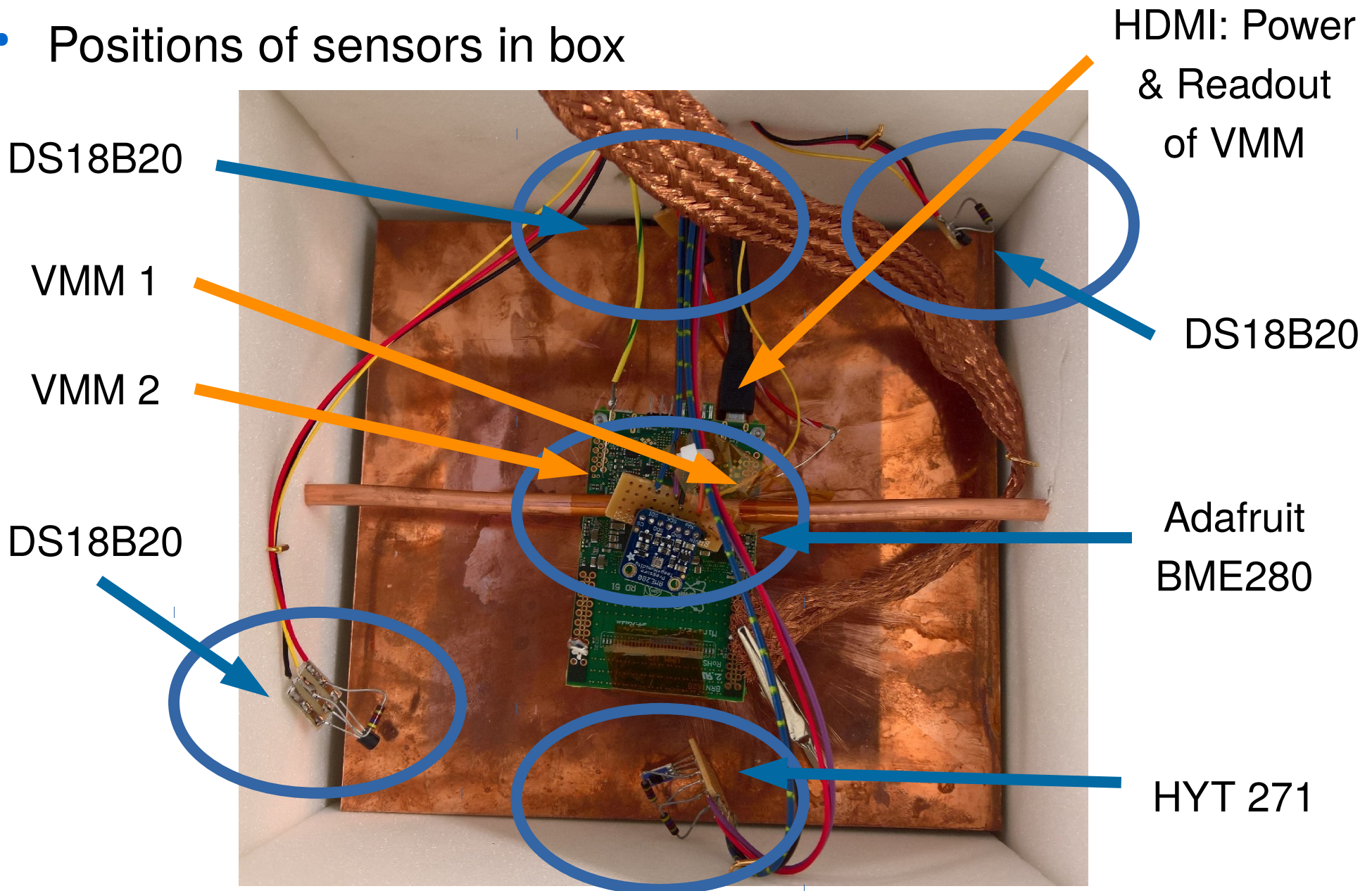
- Positions of sensors in box





# Electronics Assembly

- Positions of sensors in box



# Electronics Assembly

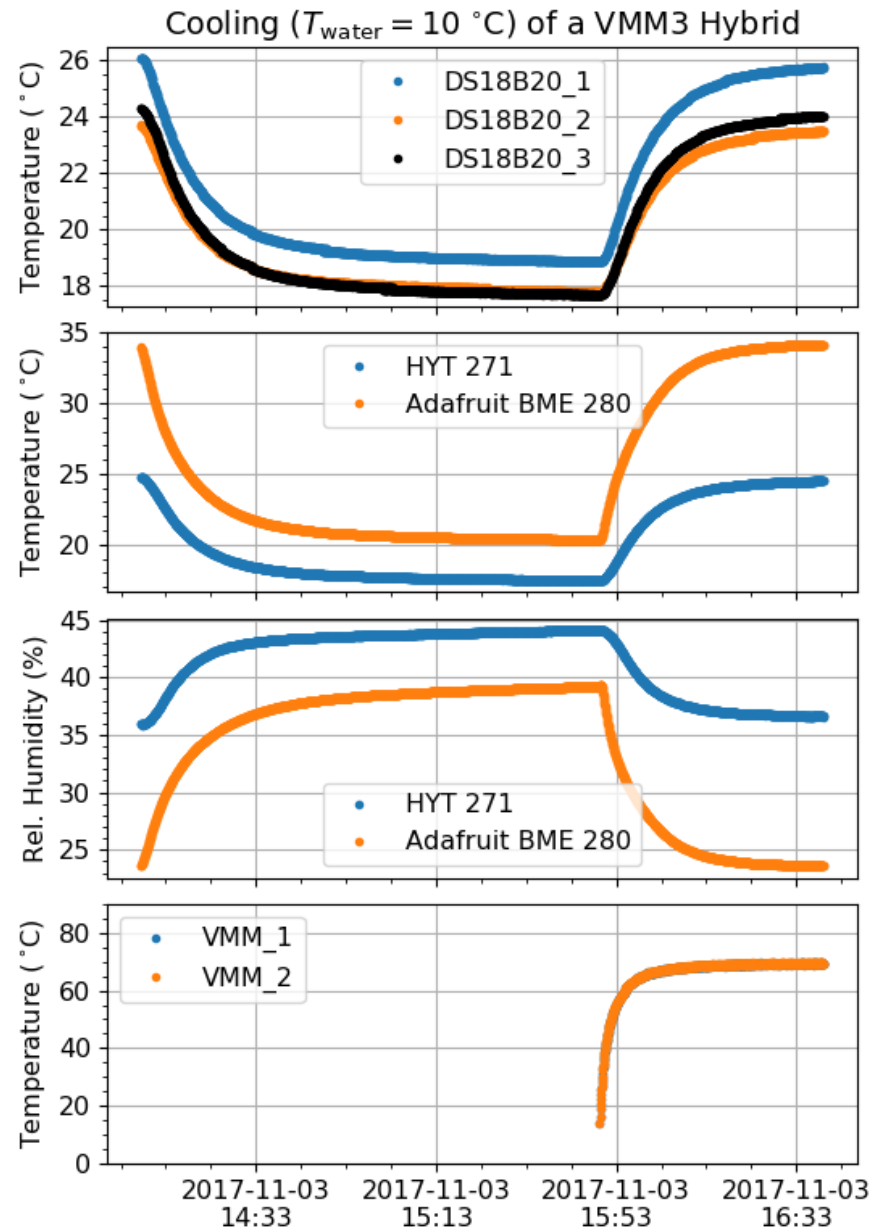
- Several sensors to measure the temperature
- 10-bit ADC used for digitising the voltage output from integrated temperature sensor
- Conversion of sensor voltage to temperature

$$T (^{\circ}\text{C}) = \frac{725 - V_{\text{sensor}} (\text{mV})}{1.85} \quad (1)$$

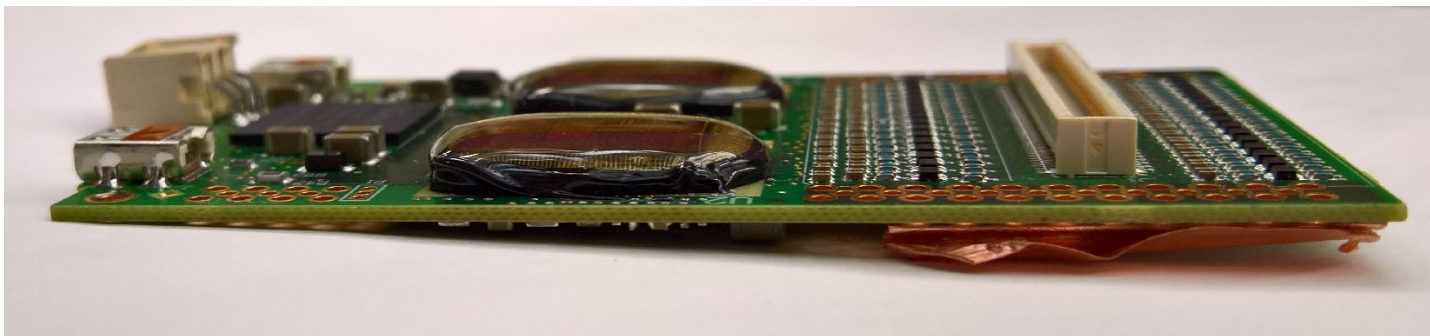
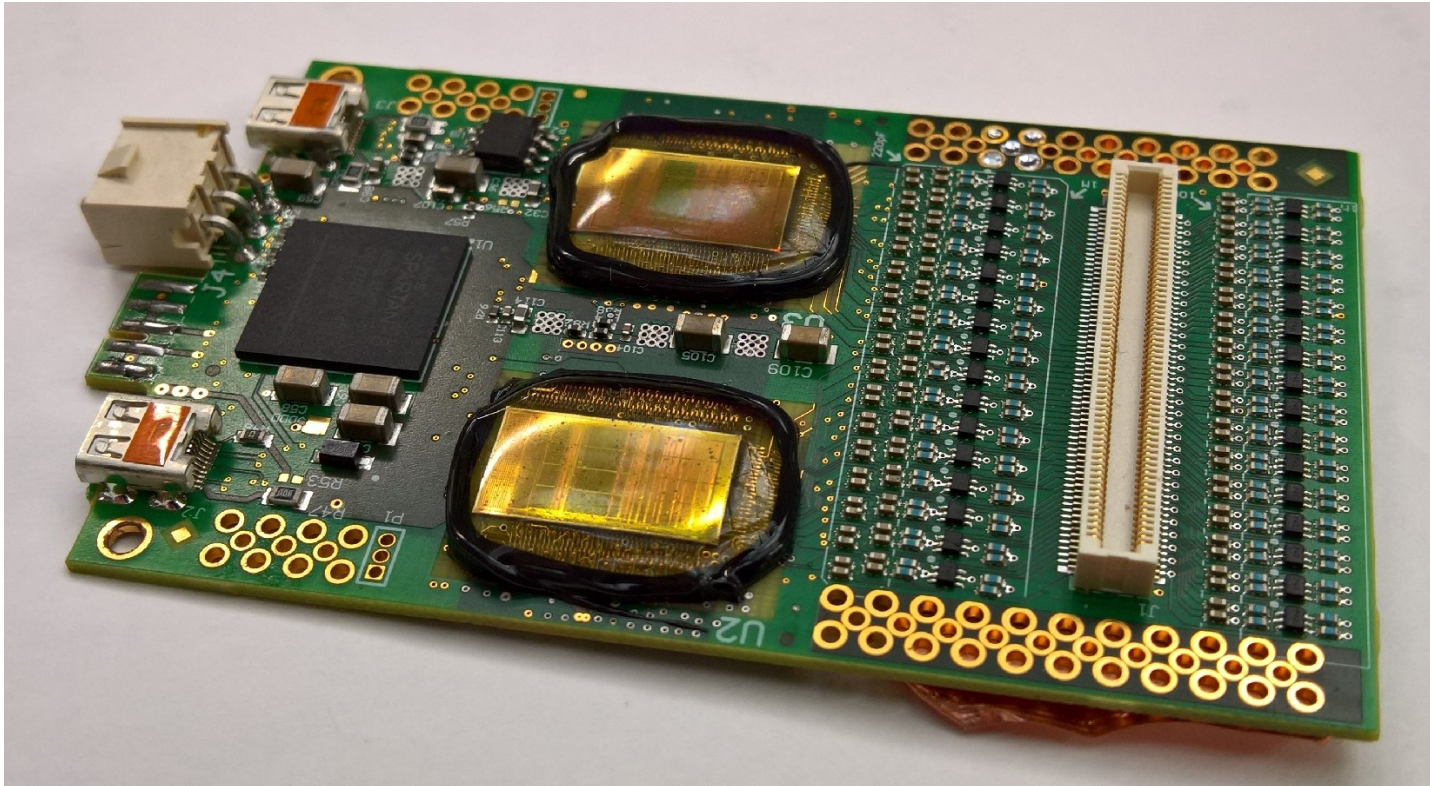
- Start testing of set-up...

# First Tests

- One of the first test of set-up
- Still with glass protection
- Temperature inside chip reaches equilibrium state
- Unfortunately some of the external sensors died
- Further improvements of the set-up...



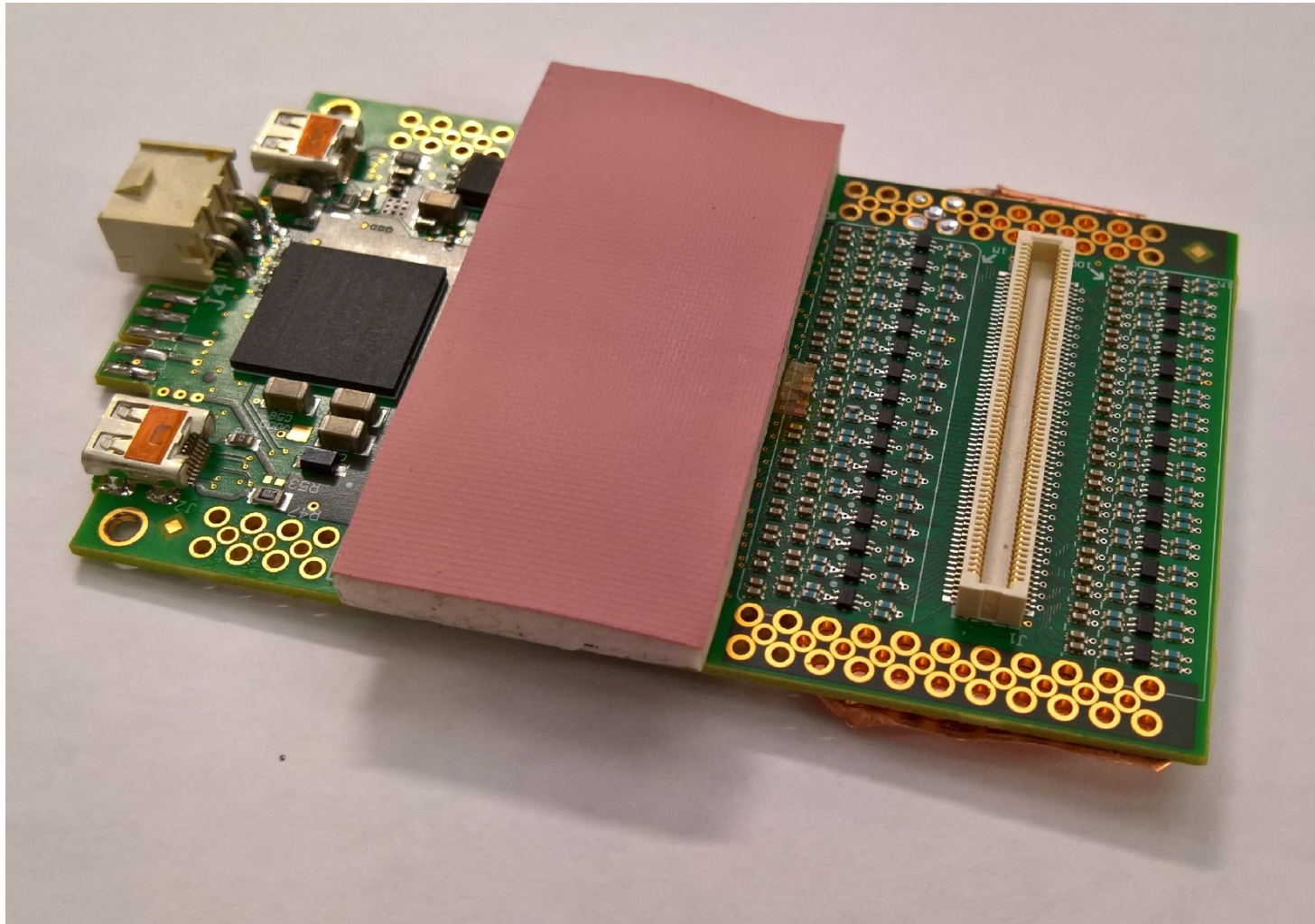
# Prototype Glob Top



Great Thanks to Hans!

# Further Improvement

- Get the temperature directly “inside” the chip:  
→ Use thermally conductive tape



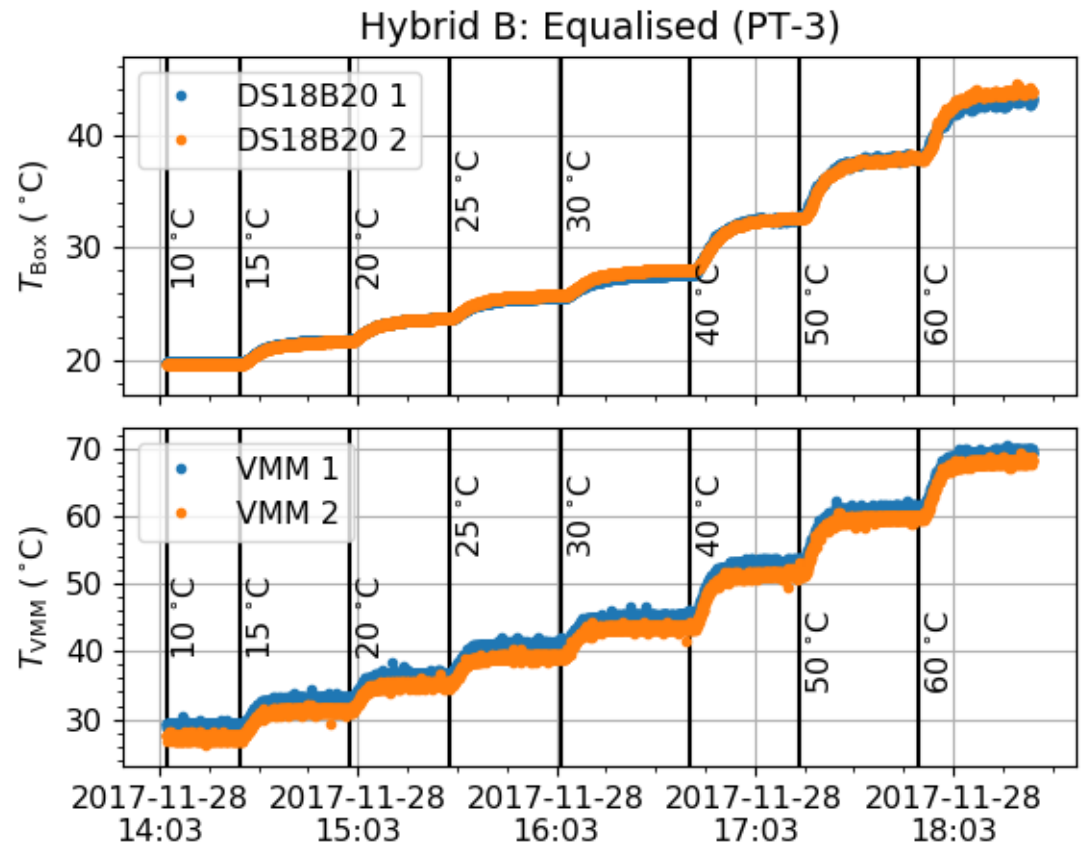
# Data from the Performance Measurements

# How to Quantify Performance?

- As mentioned: Quantify performance depending on temperature
- **How to achieve this?**
  - Take data and look how they change for different temperatures
- Problem: Data taking not possible, due to geometrical restrictions
  - Only hybrid fits in the box, but no complete detector
- Solution: Take test pulse spectra for different chip temperatures
- Test pulses on each channel → 64 t.p. per VMM
- Important: Makes only sense for equalised ADC baseline

# Measurement Process

1. Cool down environment
2. Connect Hybrid to power
3. Wait until equilibrium state is reached
4. Start measurement with test pulses
5. When measurement finished: Increase temperature and repeat process from 3.

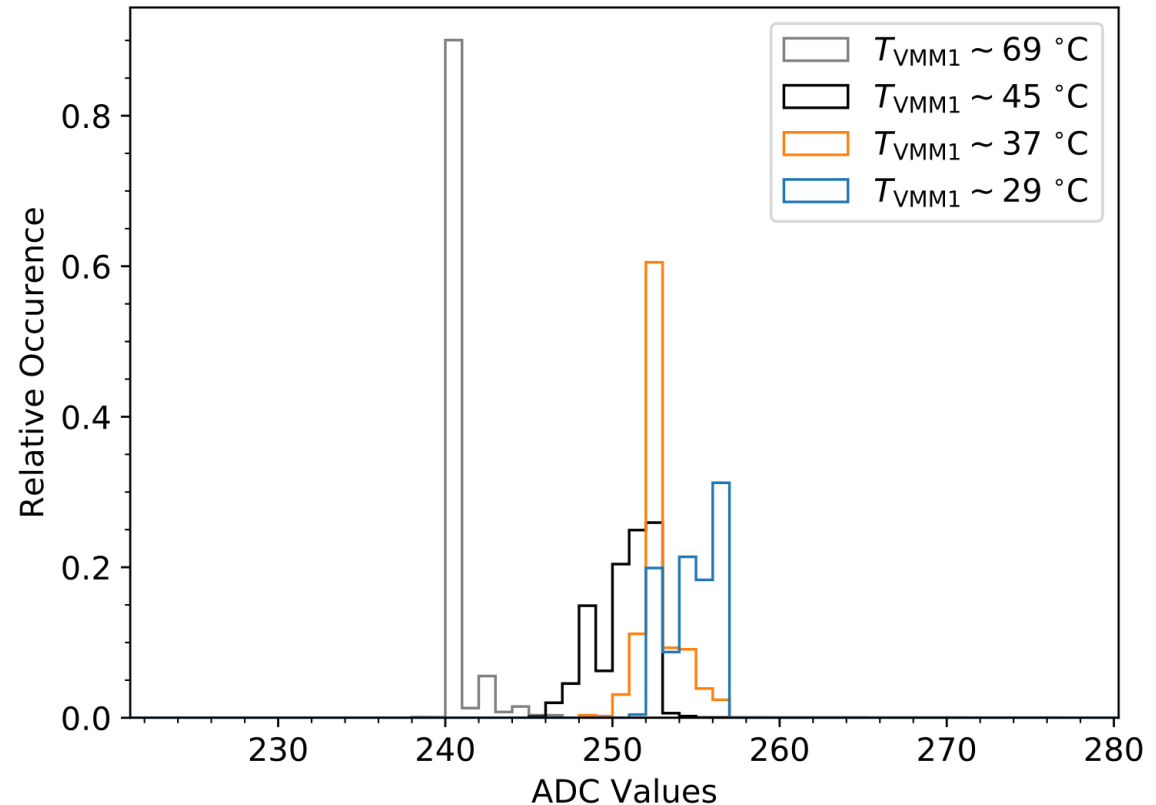




# Starting Point of Analysis

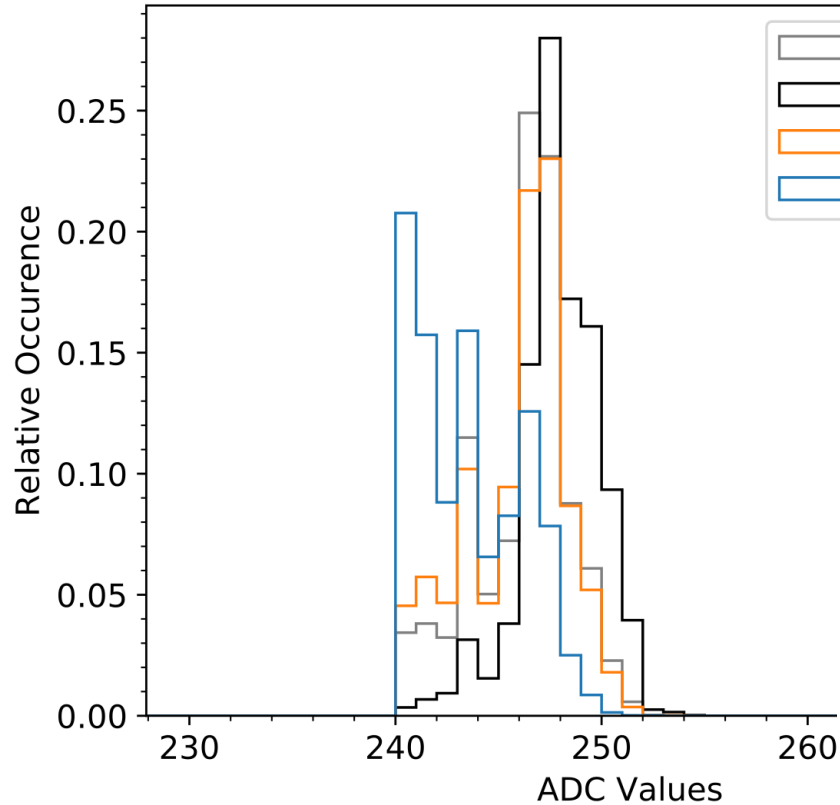
- Look at ADC spectra for each channel for different chip temperatures
- **What can we extract?**
  - Mean ADC value
  - Width of ADC distribution

Example ADC Spectrum (Hybrid B, VMM 1, Channel 42)

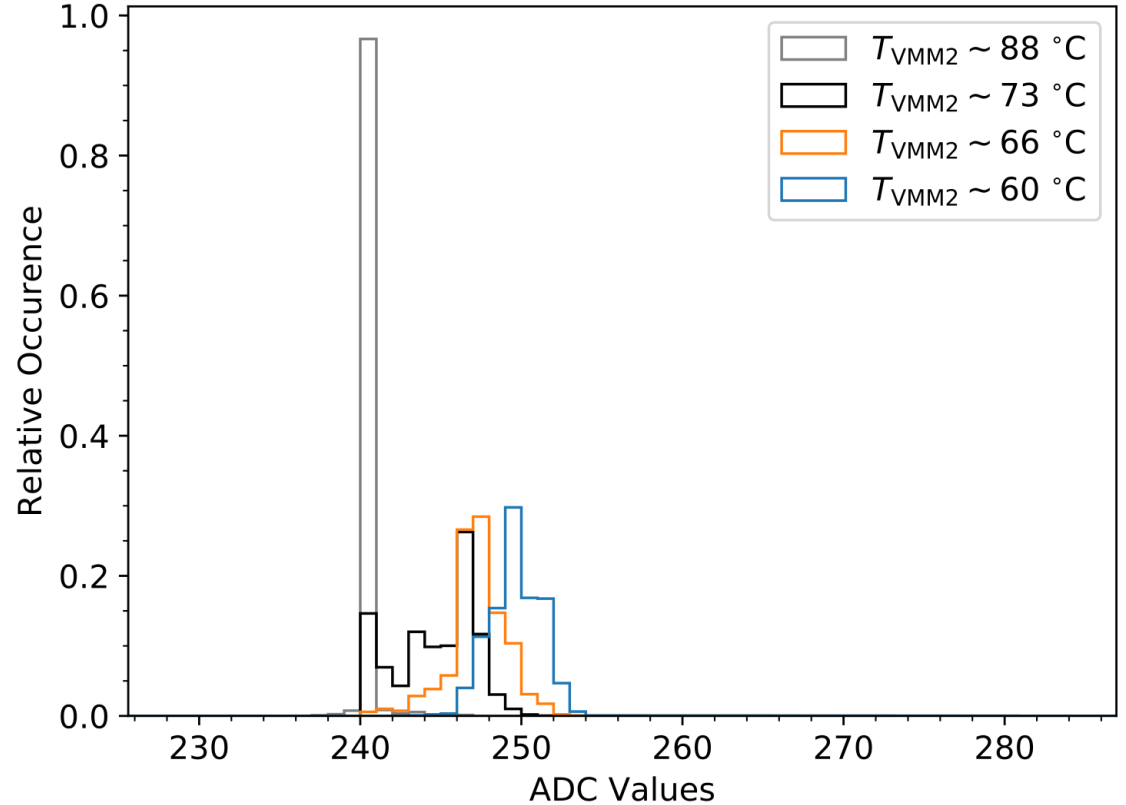


# Some Examples

Example ADC Spectrum (Hybrid A, VMM 2, Channel 42)

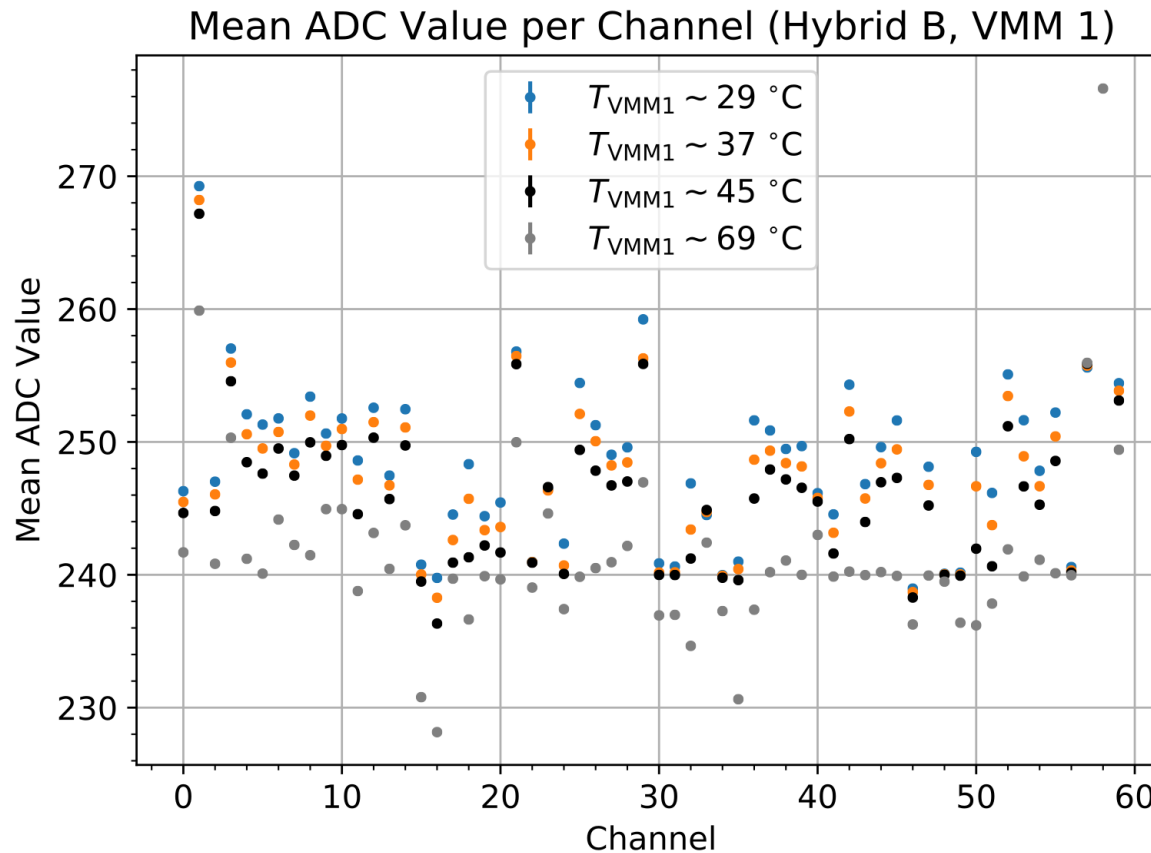


Example ADC Spectrum (Hybrid C, VMM 2, Channel 42)



# Mean ADC Value per Channel

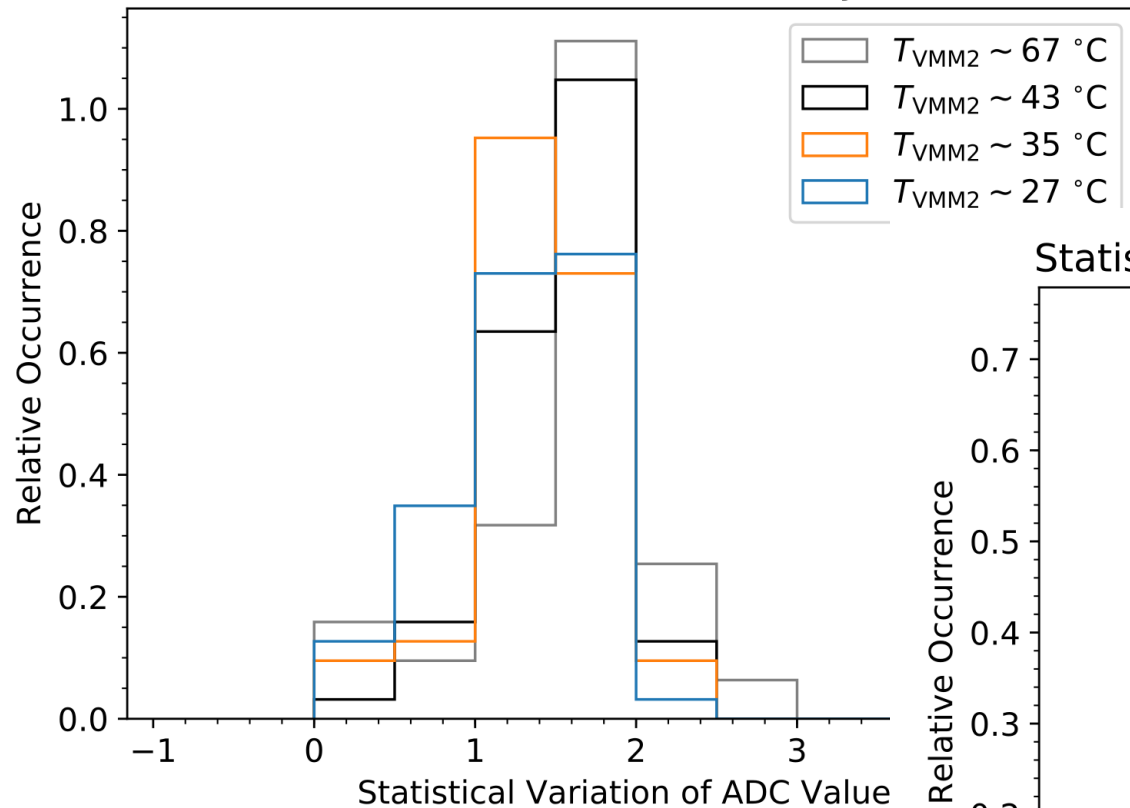
- Looking at every ADC spectrum is not useful



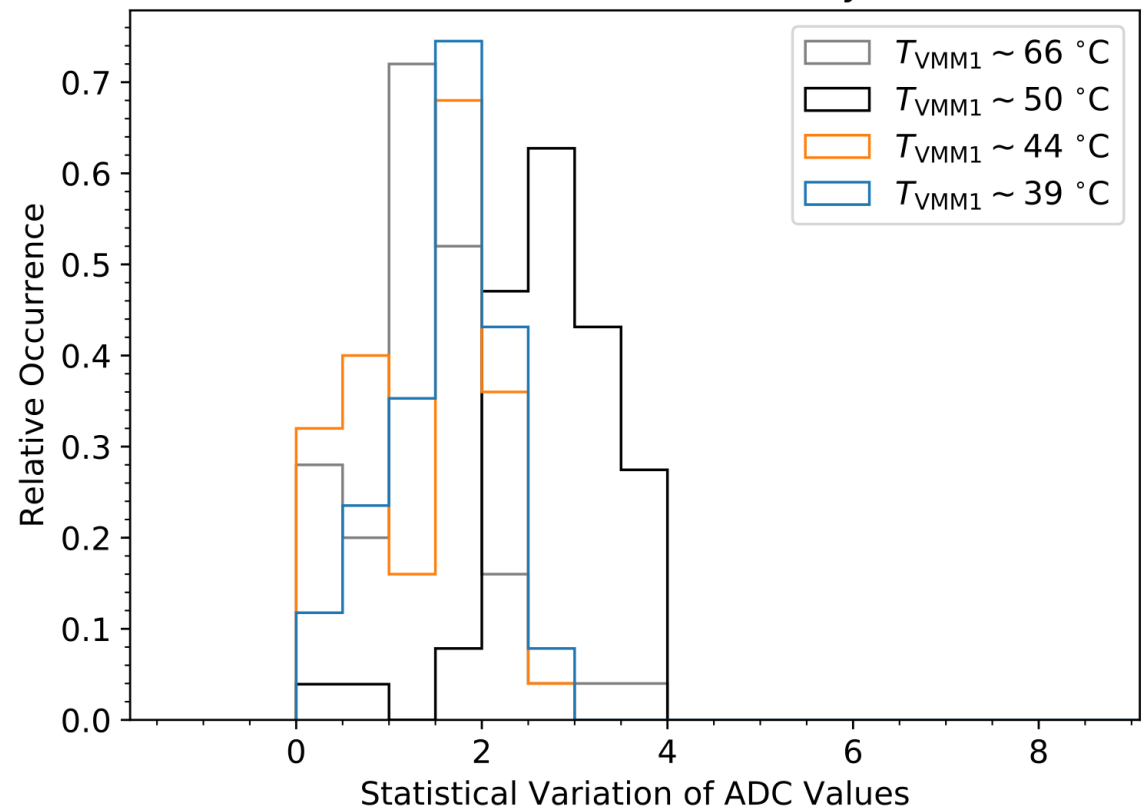
# Width of ADC Spectra

- Looking at every ADC spectrum is not useful

Statistical Variation of ADC Values (Hybrid B, VMM 2)

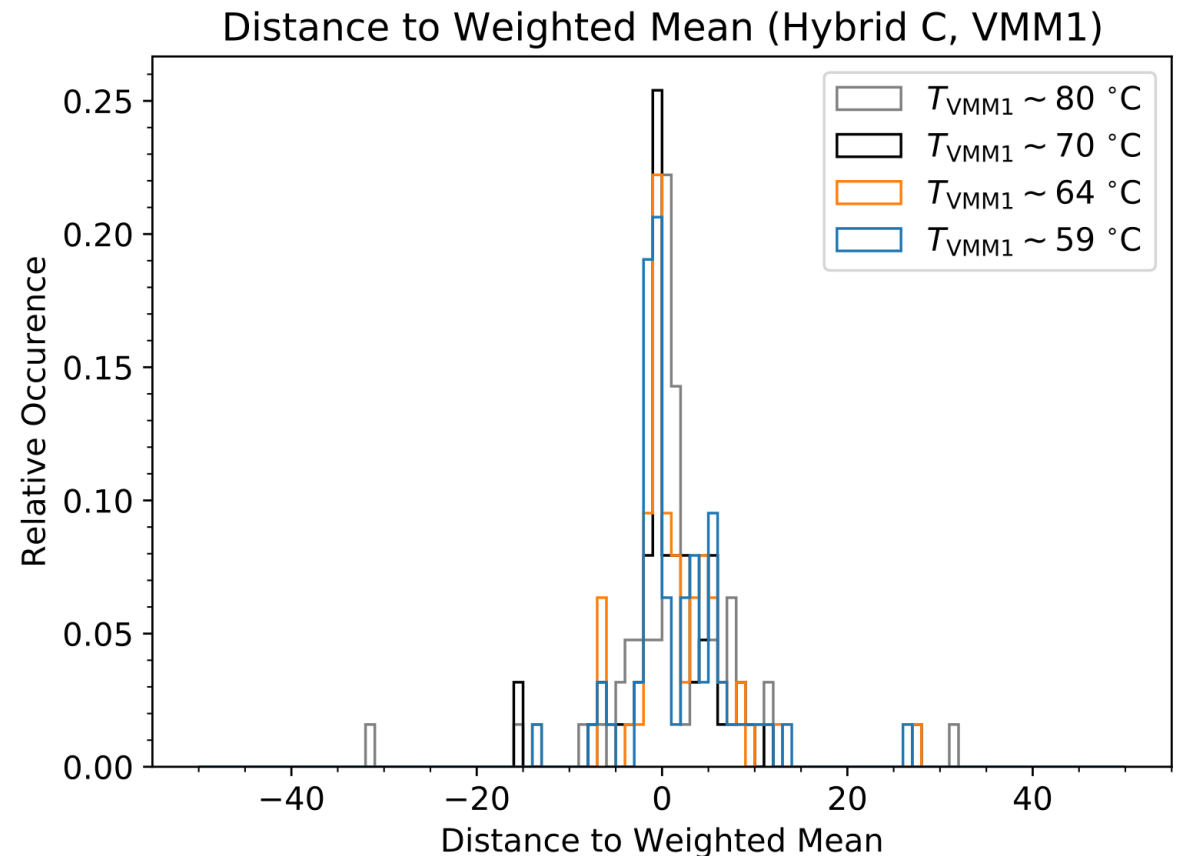


Statistical Variation of ADC Values (Hybrid A, VMM 1)



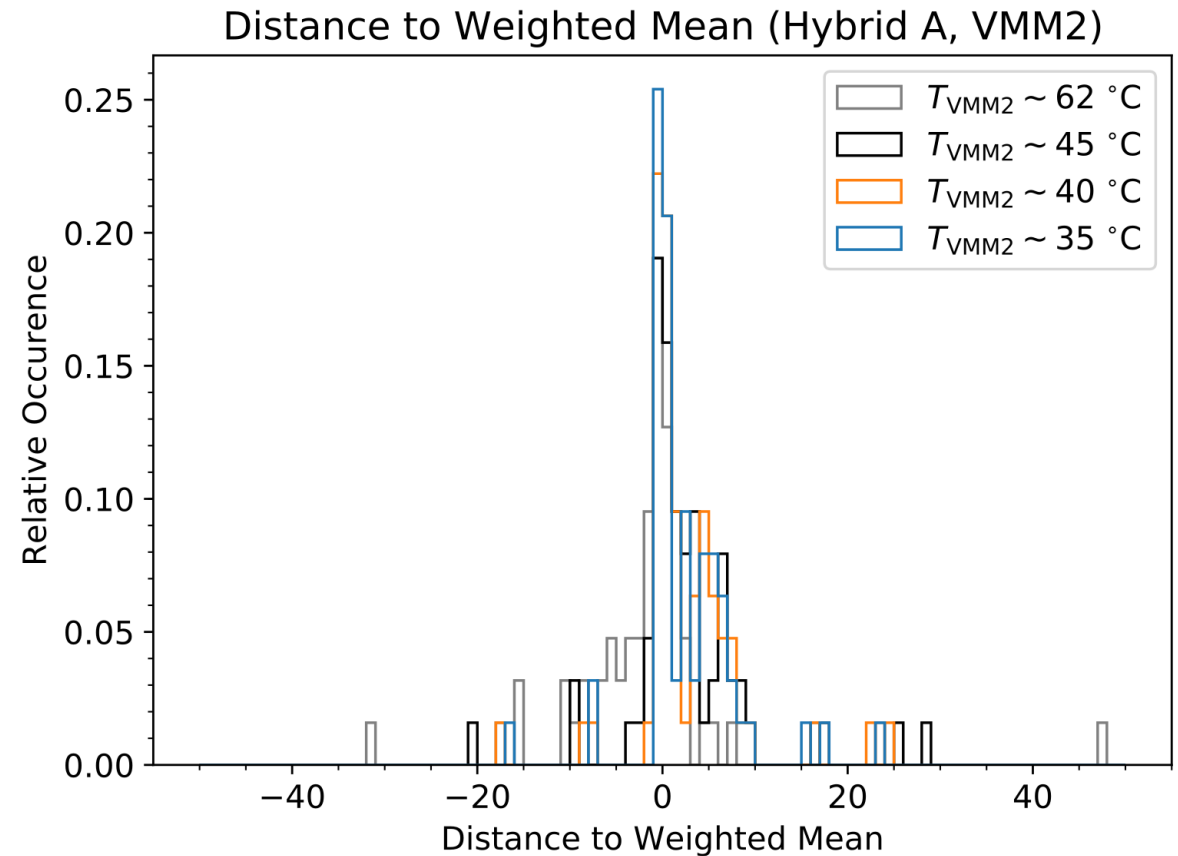
# Behaviour of the Chip

- So far: Looked at every single channel independently
- Now: Look at overall chip behaviour
  - Distance of mean ADC (channel) to weighted mean ADC (chip)



# Behaviour of the Chip

$T_{VMM}$ (°C)	Weighted Mean ADC
39	$228.7827 \pm 0.0012$
44	$225.5148 \pm 0.0012$
50	$224.1560 \pm 0.0029$
60	$223.9634 \pm 0.0014$
35	$240.44833 \pm 0.00080$
40	$240.3689 \pm 0.0012$
45	$240.3916 \pm 0.0012$
62	$240.1308 \pm 0.0012$



Weighted mean for hybrid A

Top half: VMM 1, Bottom half: VMM 2

# Conclusion & Summary

# Conclusion & Summary

- Successfully build test set-up to investigate the thermal behaviour of the VMM3 readout ASIC
- Measured 3 hybrids → 6 Chips
- Temperature dependence seen: ADC baseline shifts
- **Only** baseline shifts: No change in behaviour for constant temperature
- **Proposal for cooling:** Cooling might help, but only necessary to stabilise the temperature. Cooling itself seems to have no influence on performance. Passive cooling should be sufficient
- Did not investigate very high temperatures ( $> 100\text{ }^{\circ}\text{C}$ )  
→ Not enough hybrids to risk destruction



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Thanks for your Attention.  
Questions?