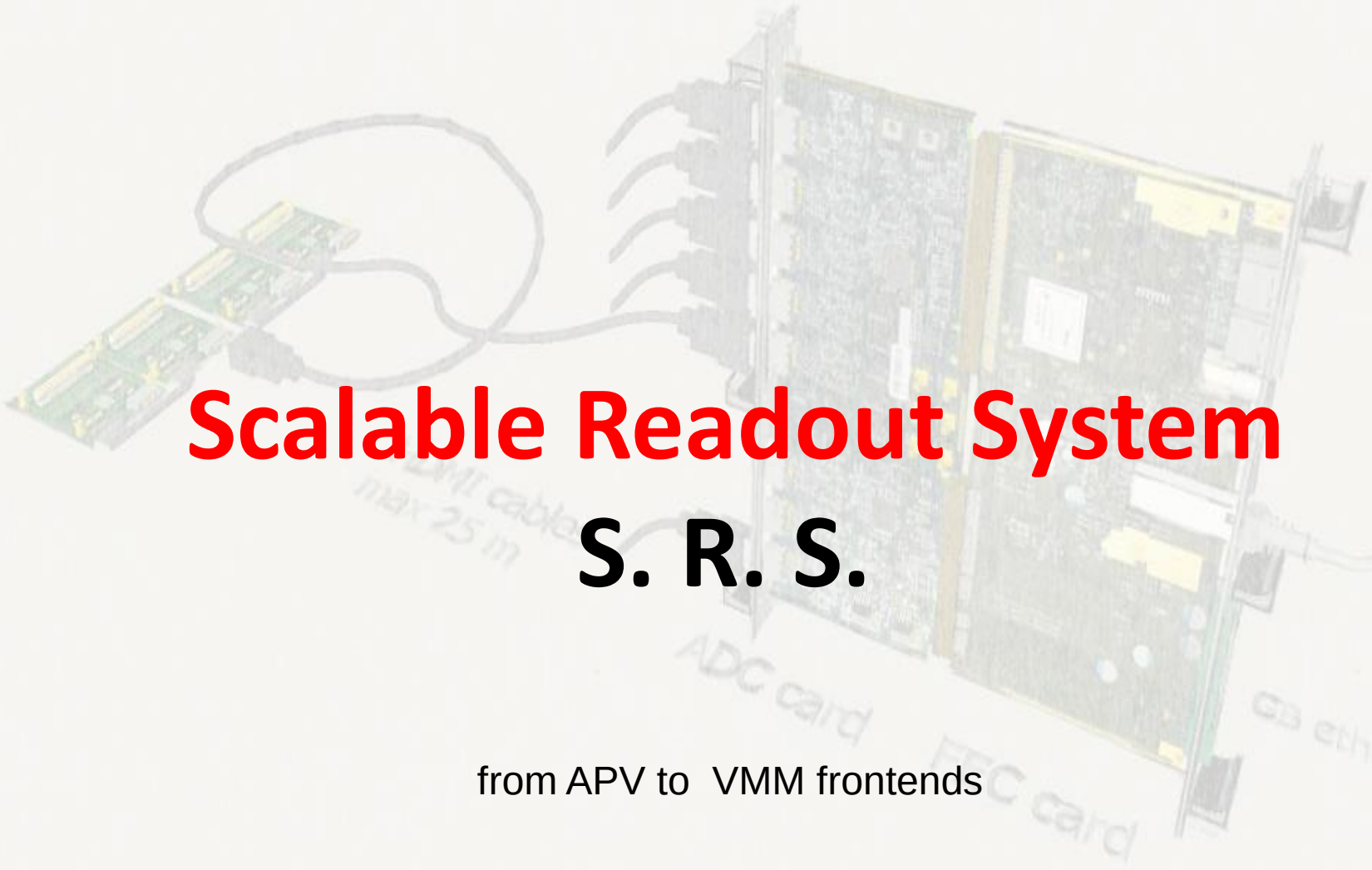


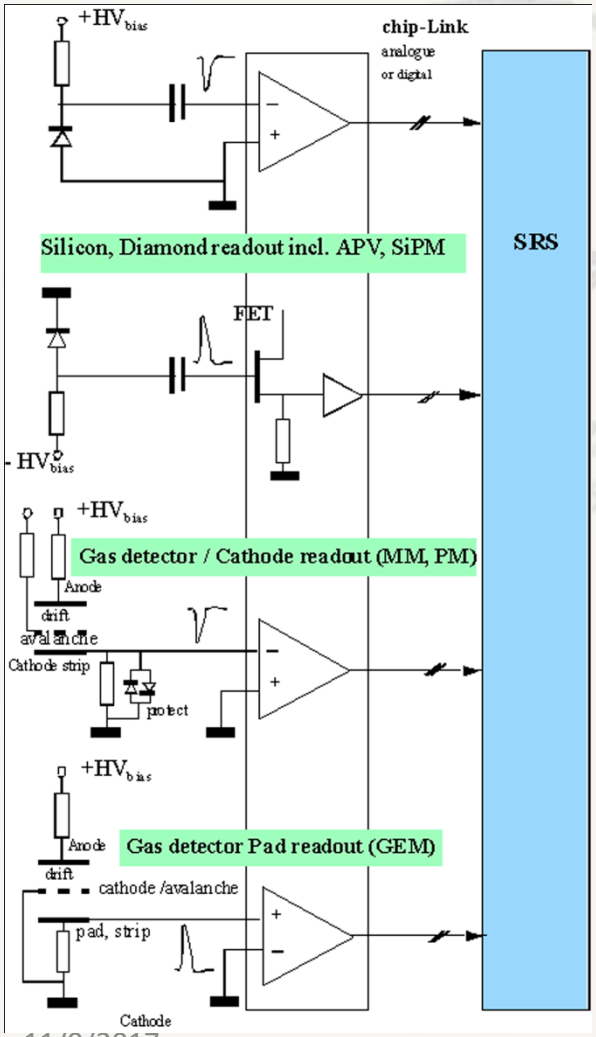
Scalable Readout System

S. R. S.

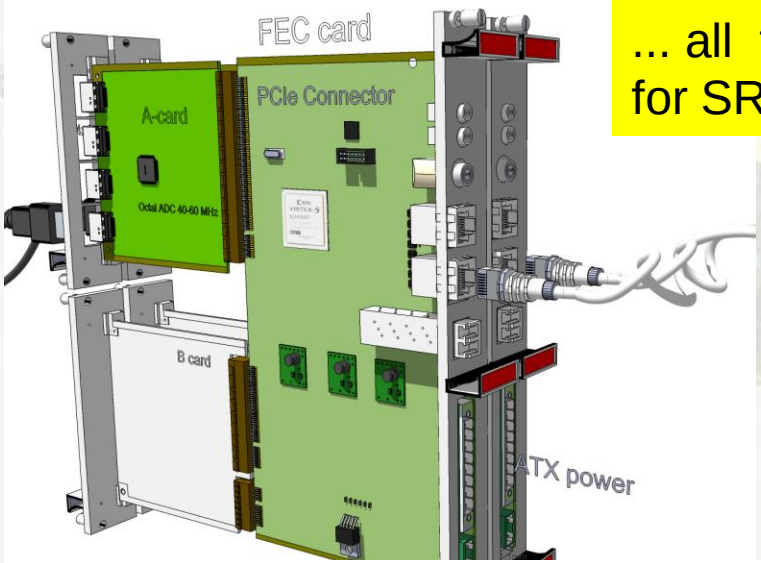
from APV to VMM frontends

RD51 user requirement (slide from 2009)

Many different detector frontends exist: users need common readout electronics with:



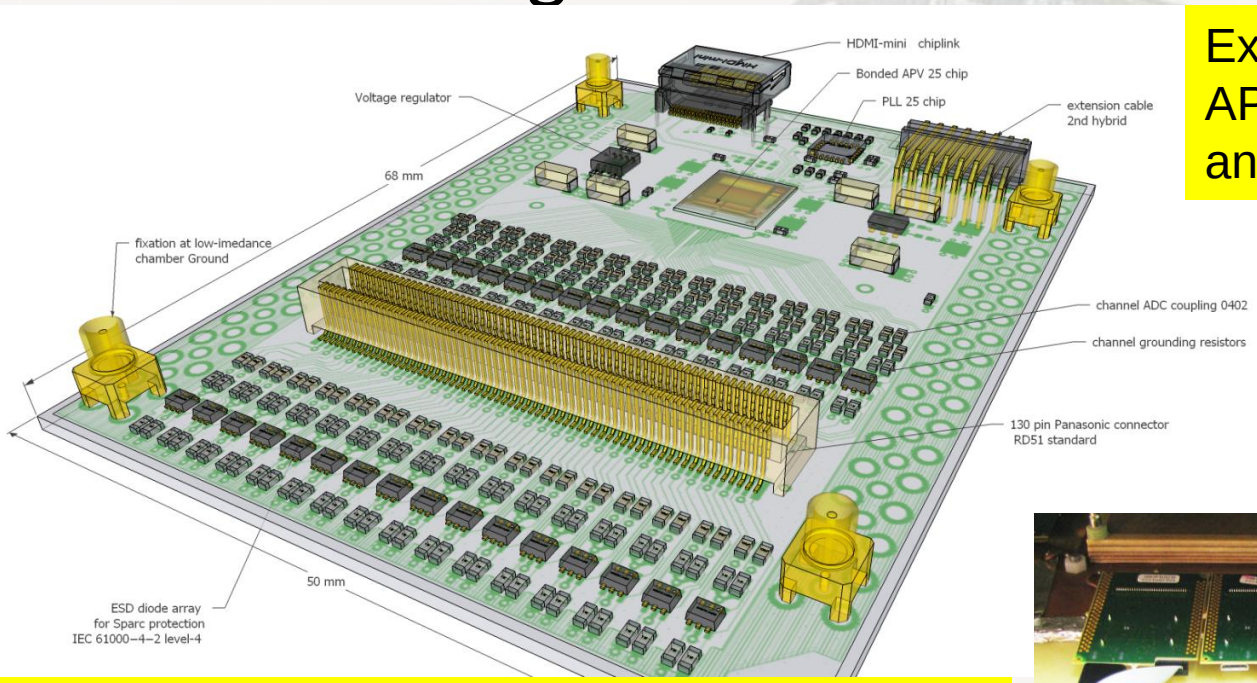
- Small set of modular components
- Performance at low cost
- Scalability from 100 to 1000.000 channels
- Plugin-choice of frontend ASICs
- Open developer platform for physics algorithms
- Supported Software made for Physics



... all this is the reason for SRS

First SRS slide from Nov. 2009, RD51 collaboration

SRS target: “plug&play”:
-keep the backbone system
-exchange the ASIC based frontend



Example hybrid with 128 cha
APV chip and HDMI readout
and ESD sparc protection

SRS backend (i

All SRS hybrids can be connected to the SRS individual hybrids have different readout ASICs

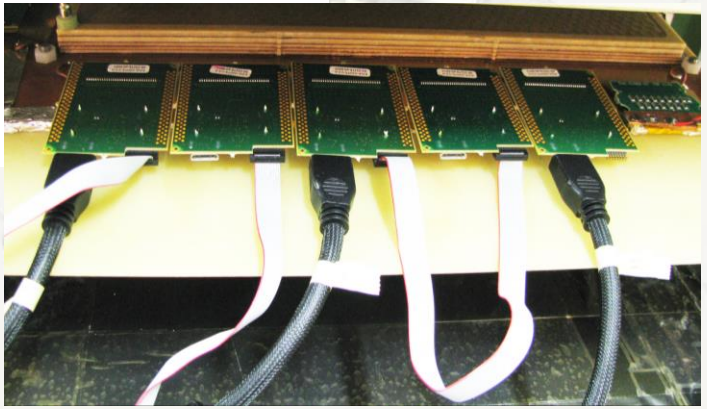
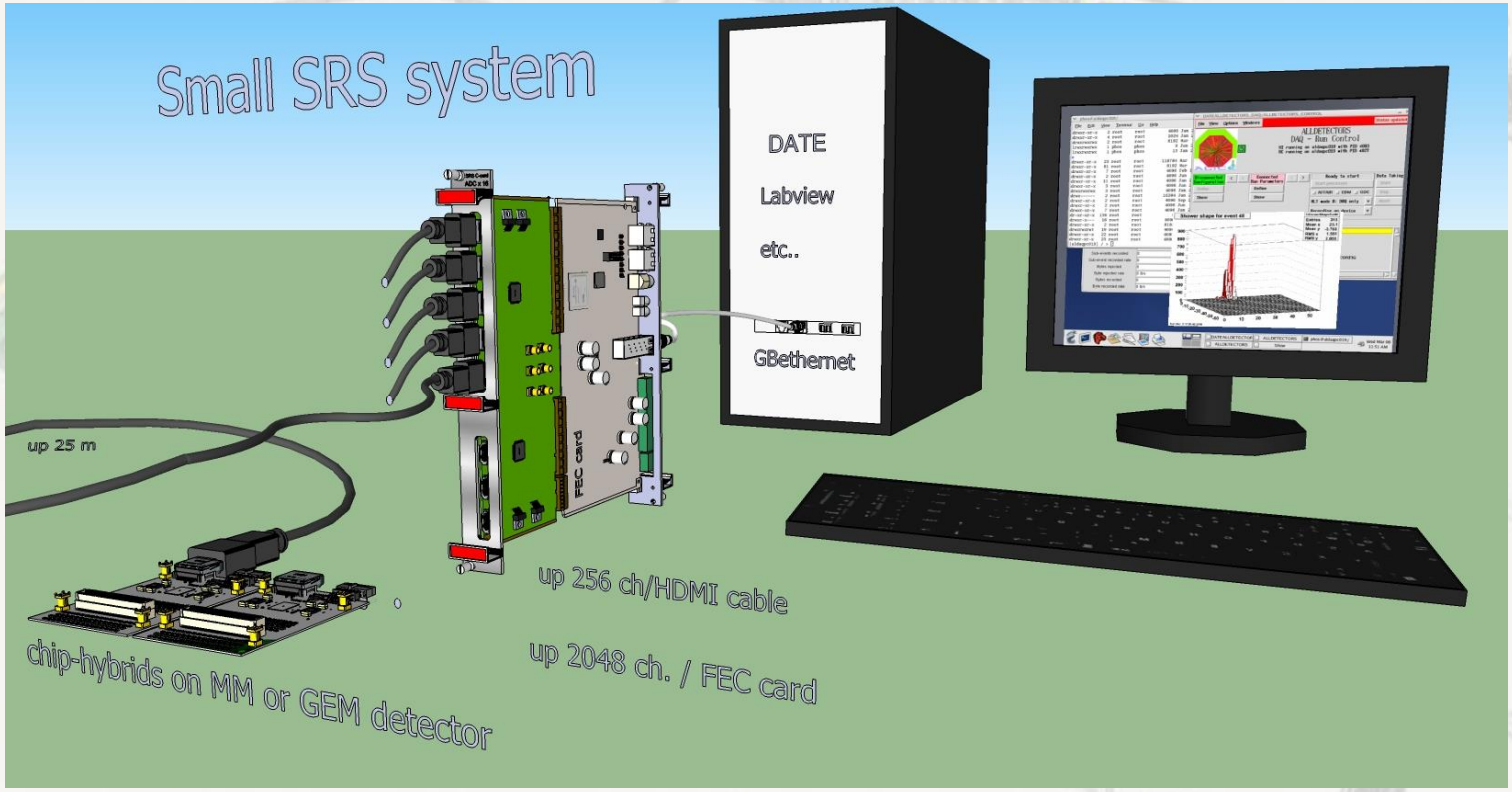


photo of APV hybrids on GEM chamber readout via HDMI cables

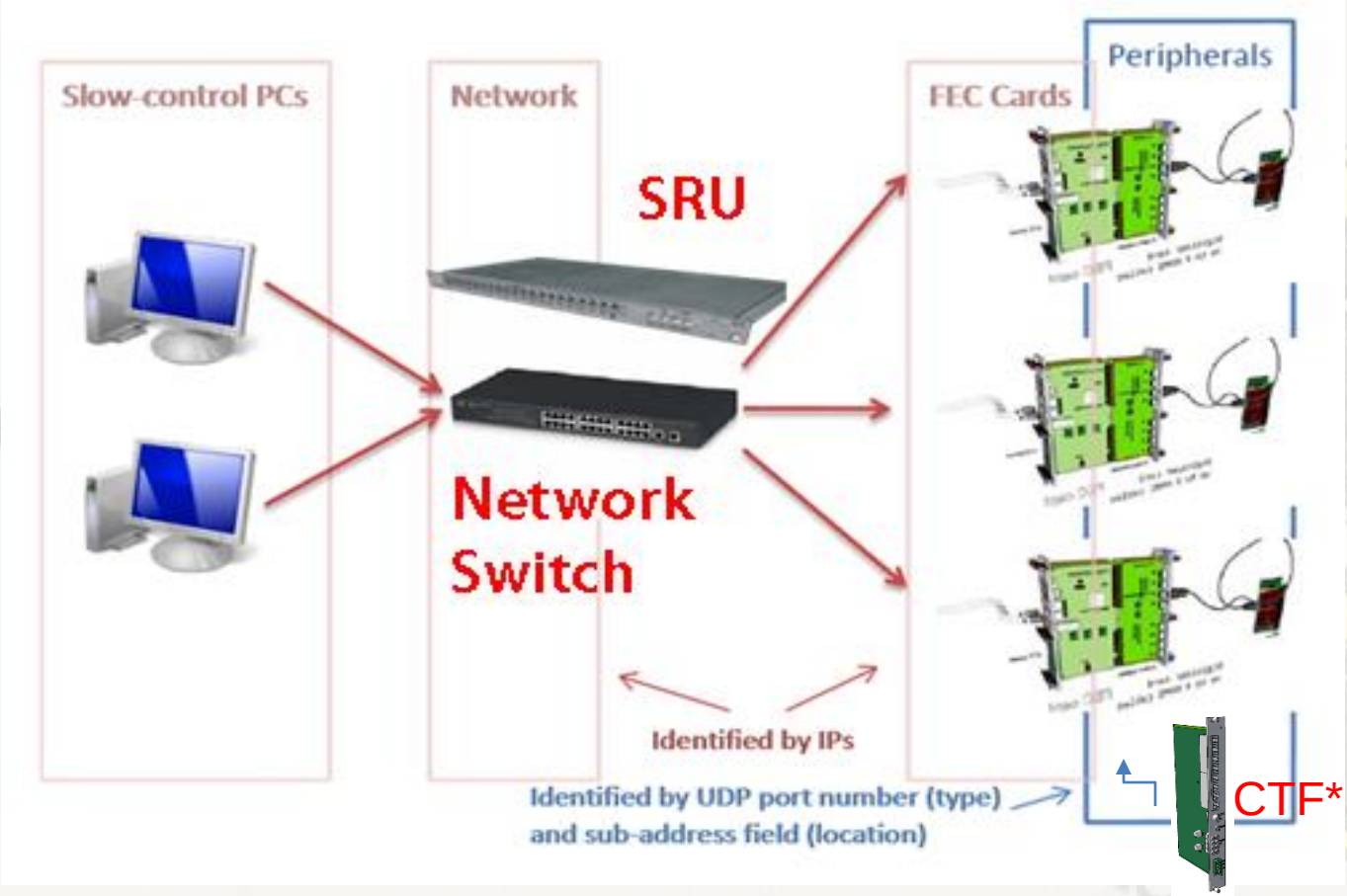
Small SRS system

128...2096 channels: 1 ADC-FEC combo



O(100) small SRS systems with APV sold via CERN store
Standard SRS Online software flavors so far: **DATE**, RCDAQ, mmDAQ, srsLabview
New ideas on Online SW see talk by D.Pfeiffer/M.Christensen

Larger SRS systems



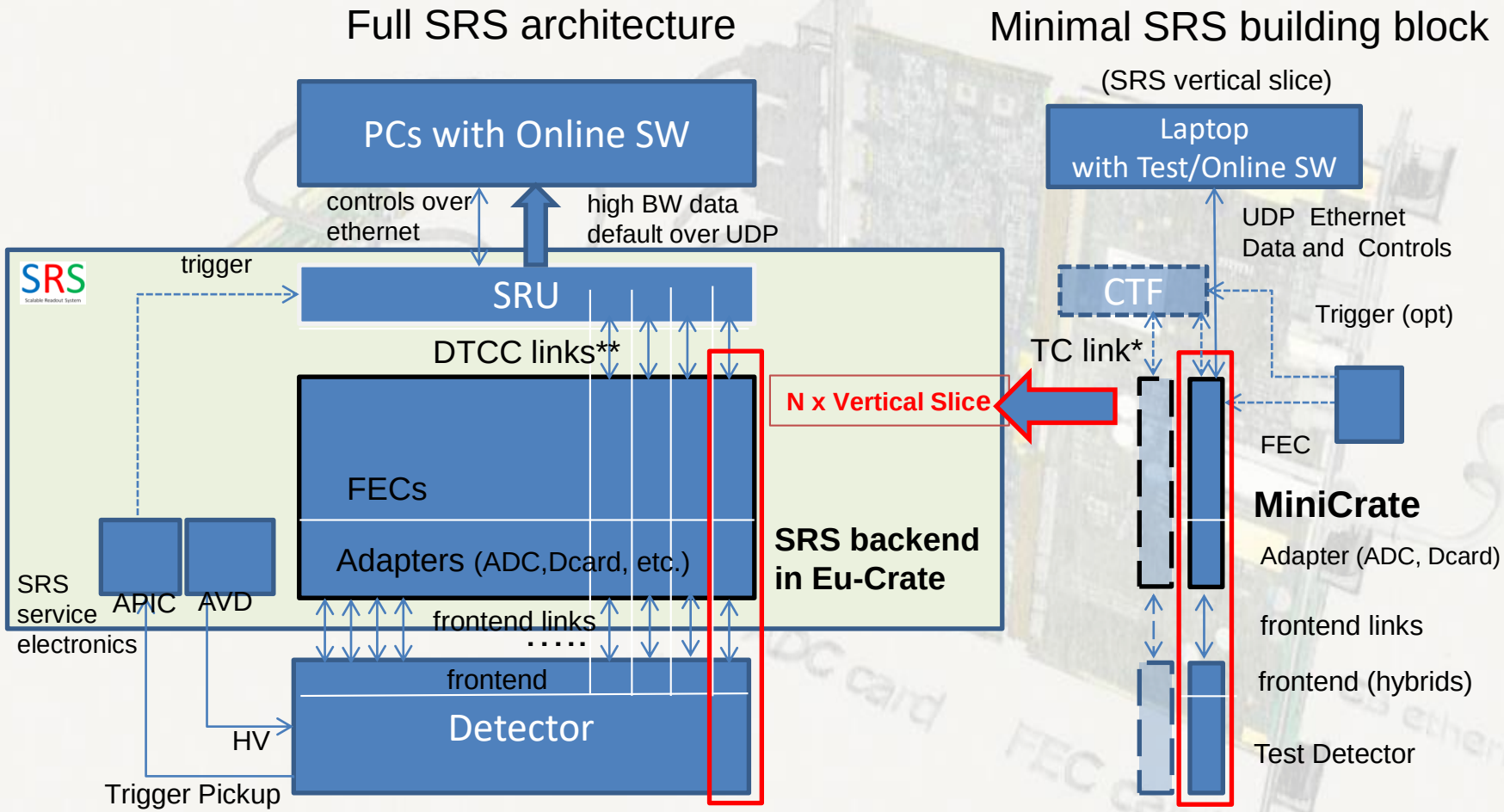
Scalability: add FEC Combos in parallel inside a powered SRS Eurocrate for readout via UDP:

a.) Network switch + CTF clock-trigger card ➔ works with few FECs

b.) SRU with 10 GBE uplink and 1 GBE controls ➔ scales up 40 FECs

*CTF and SR are exclusive
they use the same DTC link

Scalable Readout Architecture



a full SRS system is a stack of vertical slices of small systems

**DTCC link: physical and logical Data, Trigger, Clock, Controls

*TC link: physical subset of DTCC link: Trigger,Clock

SRS HW components so far

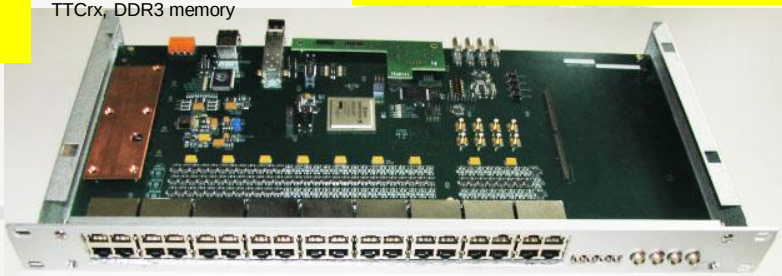
ADC adapte card

ADC card design, S.Martoiu IFIN Bucharest

HDMI interface for 16 analogue hybrids
16 ADC's 12 bit 40 MHz

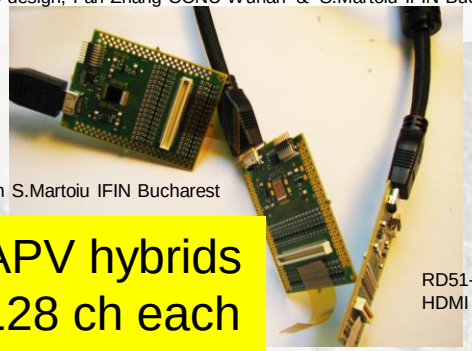
Scalable Readout Unit

FPGA based , 40 DTC links
4 GBE links, Trigger interface
TTCrx, DDR3 memory



SRU design, Fan Zhang CCNU Wuhan & S.Martoiu IFIN Bucharest

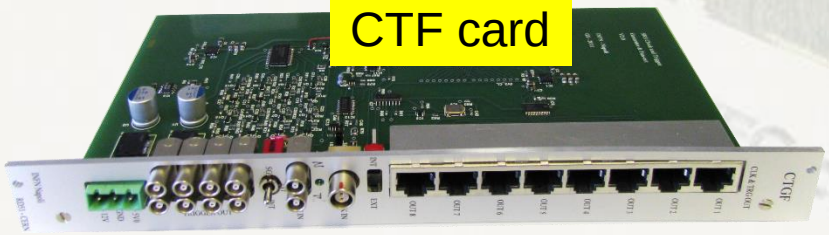
APV hybrids 128 ch each



APV hybrid design S.Martoiu IFIN Bucharest

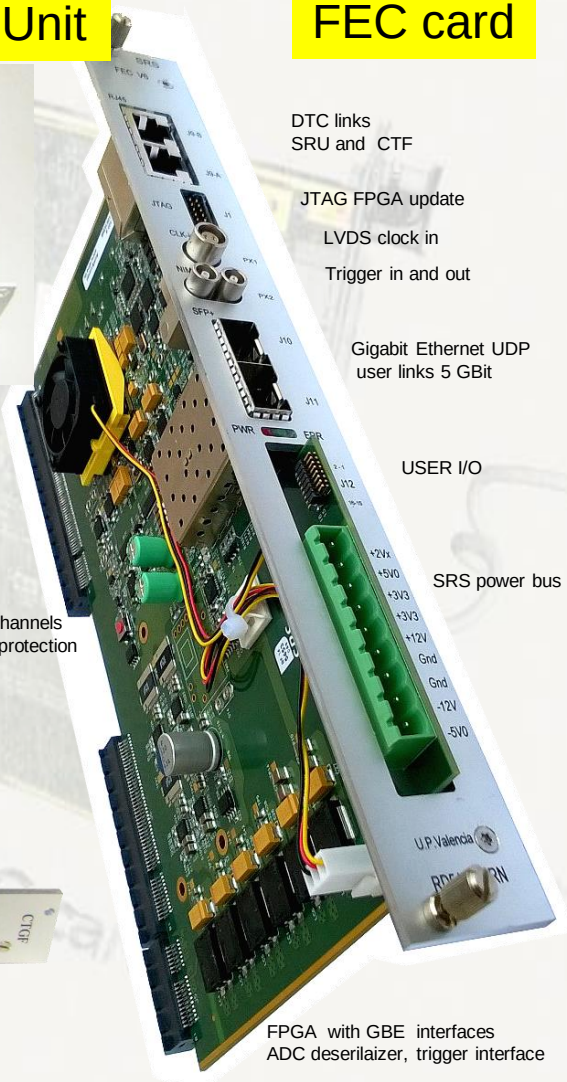
RD51-standard , 128 channels
HDMI interface, sparc protection

CTF card



CTF design, G. Sekhniaidze INFN Naples

FEC card



DTC links
SRU and CTF

JTAG FPGA update

LVDS clock in

Trigger in and out

Gigabit Ethernet UDP
user links 5 GBit

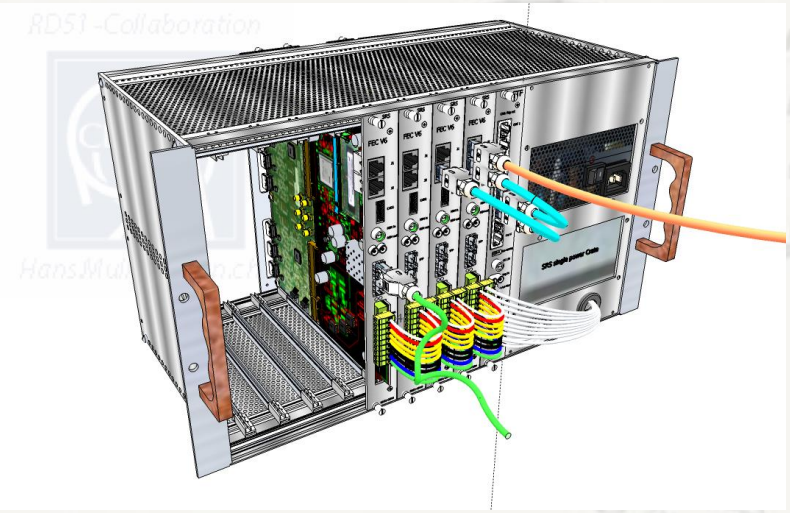
USER I/O

SRS power bus

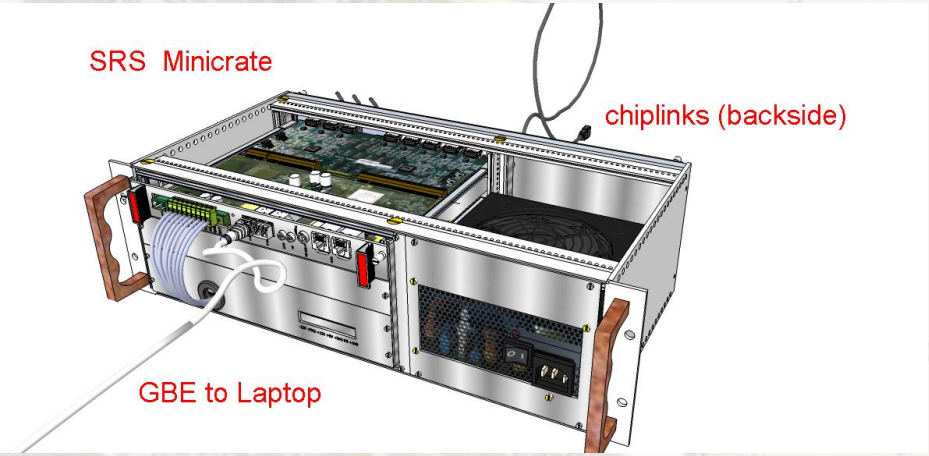
FPGA with GBE interfaces
ADC deserilaizer, trigger interface

FECV6 design J.Toledo UPV

SRS 19” Crate and power

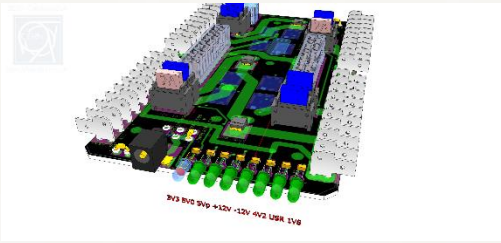


Crate design EU + Mini H.Muller CERN



6U x 220 mm Eurocrate V1
max 8 FEC + 1 CTF slots

3U x 220 mm Minicrate V2
2 FEC slots

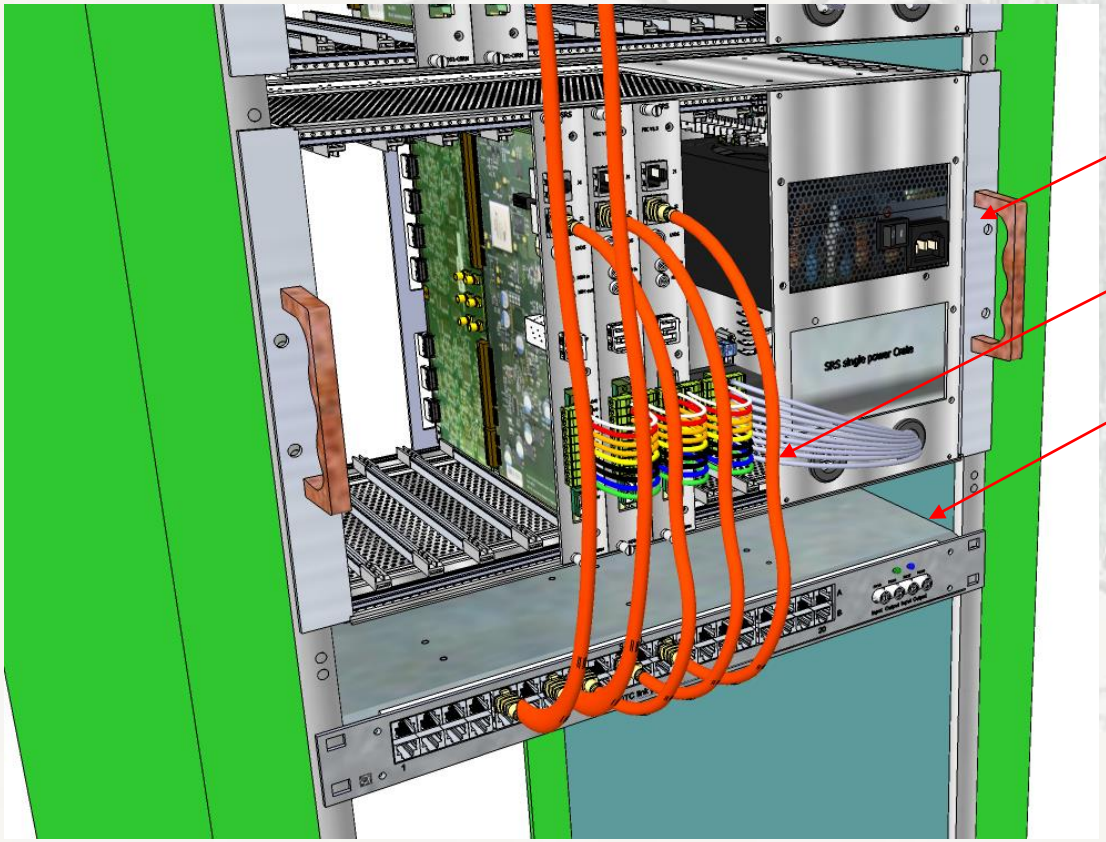


ATX adapter design V.Gezer / H.Muller CERN

Power adapter ATX -> SRS included in SRS crates

Under revision for dual-power Eurocrate V2

SRS rack environment



Eurocrate with FEC cards

DTCC links (CAT6 cables)

SRU in 1 U rack mounted box

3 ports 5Gbps, 1 port 10 GBE

24 Ports DTCC links

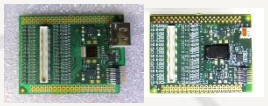
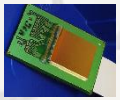
FPGA
LX240 Virtex6

Beyond 10 Gbit SRU bandwidth

use of SoC multi-processors with integrated high bandwidth SRIO / GBE ports

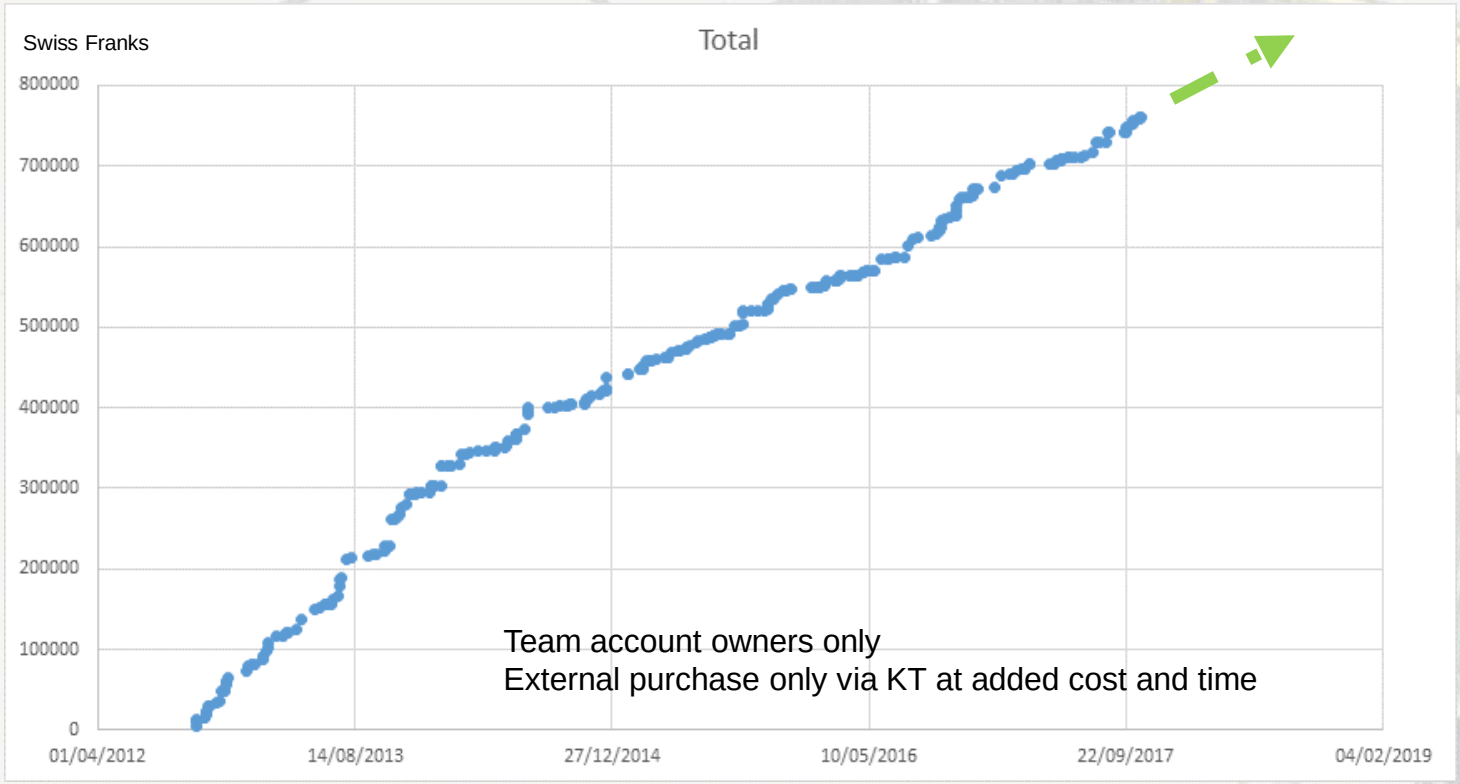
see talk by Dorothea Pfeiffer

SRS frontends

APV25-RD51		V1,V2,V3 proto hybrids V4 became “working horse” up today
SiPM-NEXT		2 prototypes ATCA -SRS became standard for NEXT TPC
Timepix Univ.Bonn		2 prototypes A -> C-card -> AIDA project restart for Timepix 3 SRS
VFAT-RD51		V1 prototypes hybrid, discontinued, technical problems
Beetle RD51		V1 prototype hybrids, discontinued, manpower shortage
GEMROC-AGH/EicSys		AIDA-project: GEMroc hybrid with plugin adapter for SRS, non info
VMM-RD51	 	V1,V2,V3 proto hybrids, V4 becoming new standard 2018

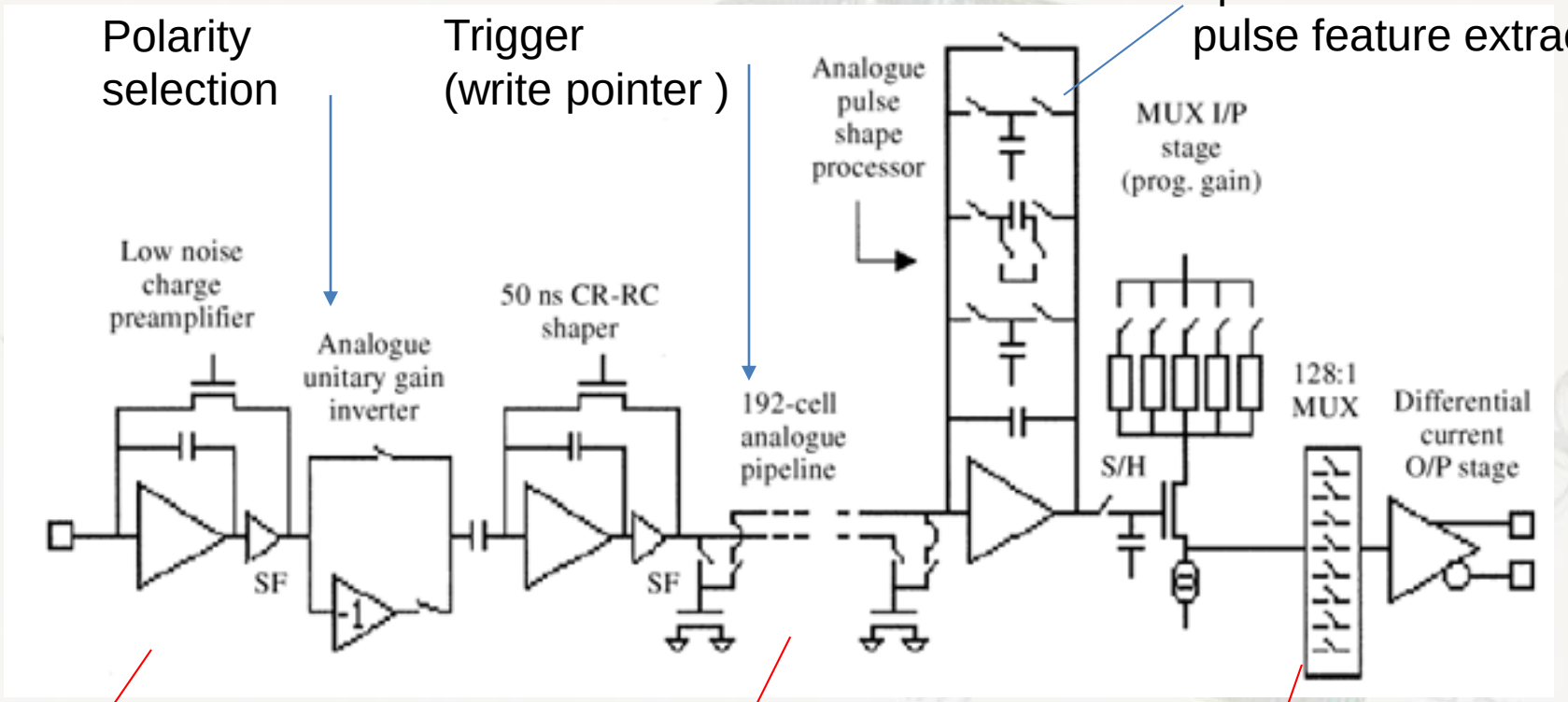
successful frontends: man x years + resources required for HW, FW, SW

SRS sales until 2017: CERN store



New SRS sales paradigm:
KT-licenced companies Samway, EicSys, SRStechnology

APV 25 frontend

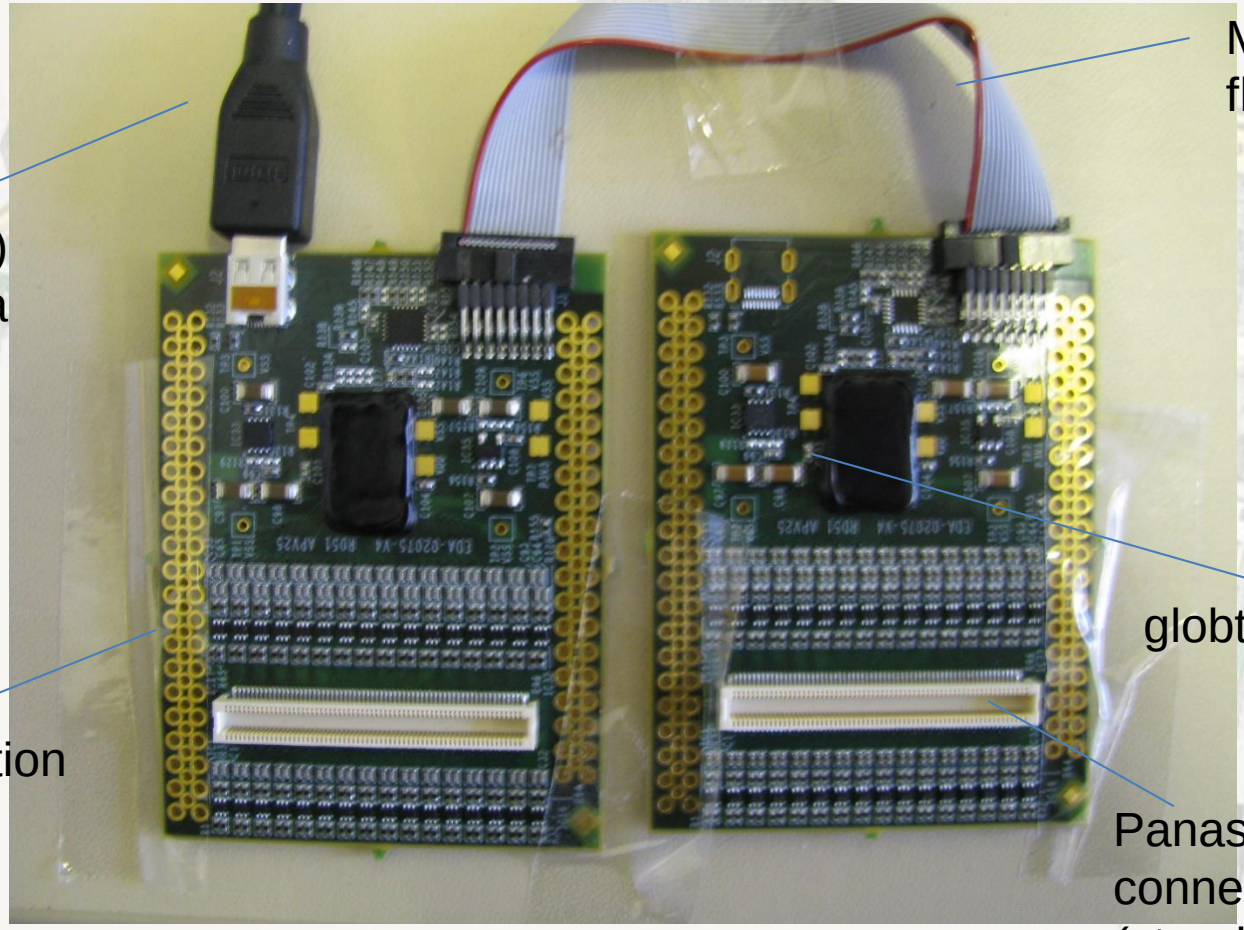


1 of 128 CSA's
fixed gain ~5mV/fC
Noise ~ 250e- +36e-/pF

analogue pipeline 192 deep
1 symbol / 25 ns (4.8us)

serialized analogue output

Master-Slave APV readout



Readout cable
to SRS (HDMI)
-analogue data
-trigger
-power
-controls

Master-slave
flat cable

globtopped APV25

-spark protection
-AC coupling

Panasonic
connector
(standard up to now)

2 x 128 channels

APV* Pros and Cons

PRO

- Like a multichannel oscilloscope: signal waveforms
- availability from stock
- 128 channel per chip
- Low power O(1/2 W)
- no major cooling issues
- SRS: plug&play
- many users

CON

- Max trigger rate O(5kHz)
- No zero suppression in chip
- Limited cable length (analogue)
- max C_{det}~ 50 pF (2000 e- noise)
- fixed CSA gain -> limited dyn. range
- Non-consecutive channel readout
- reported non-linearity over dyn range

*0.25 micron CMOS

VMM ASIC

Design efforts in RD51 started in 2014

proto versions V1,V2,V3 ->V4

RD51 main interest in VMM frontend for SRS

- digital chip with zero suppression
- no rad-hard embargo for RD51 communities
- (auto-trigger) rates 100..1000 above APV

VMM3

programmable shaper
25,50,100,200ns

neighbor sensing logic

Digitizers 6 b channel
10b peak, 8b time

L0 trigger selector

2 x digital data lines effectively 2x 512 Mb/s 38b / event

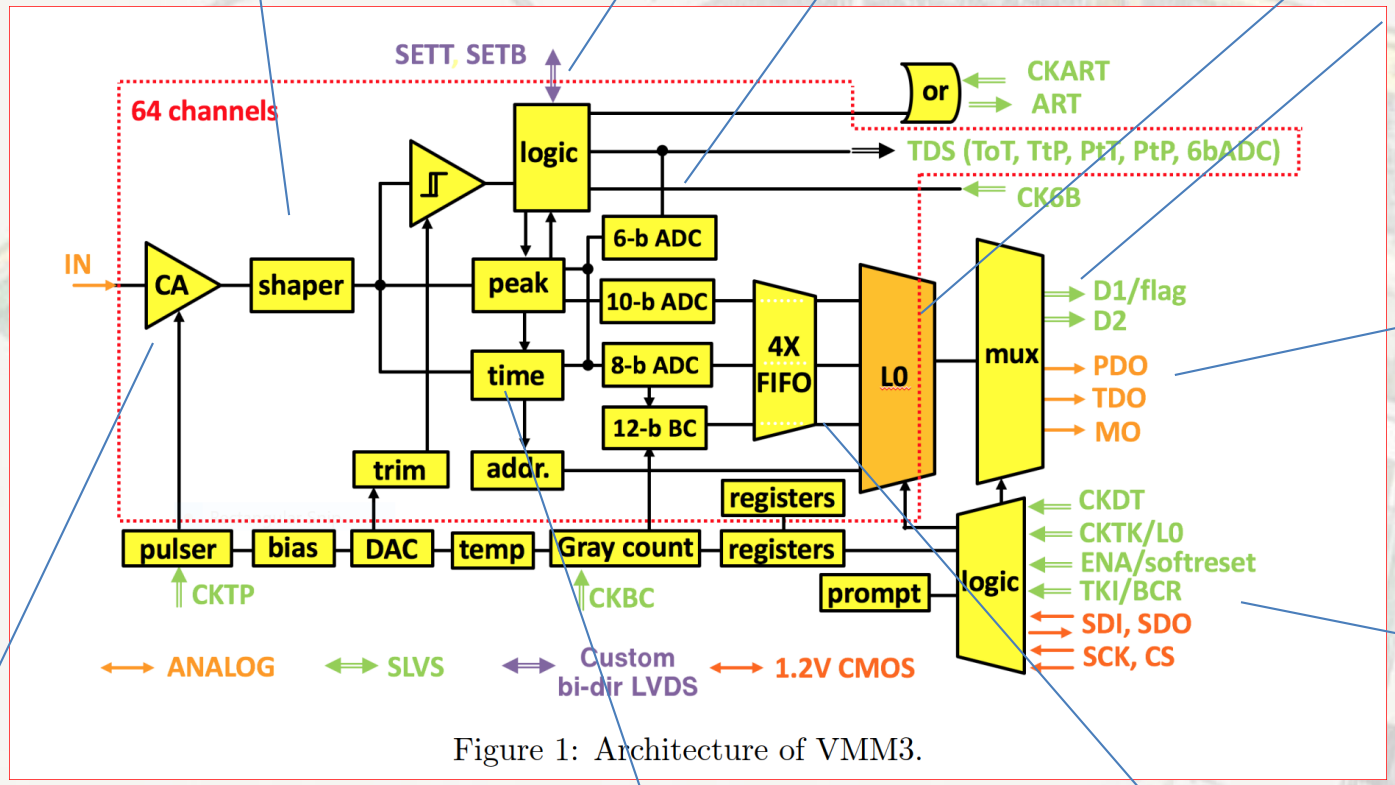


Figure 1: Architecture of VMM3.

analogue monitoring
1 of 64 ch.
Peak,Time
Temperature

controls

1 of 64 CSA's
programmable gain
0.5, 1, 3, 4.5, 6, 9,12,16 mV/fC

Peak and time detectors

FiFo with tokens for ZS

VMM* Pros and Cons

PRO

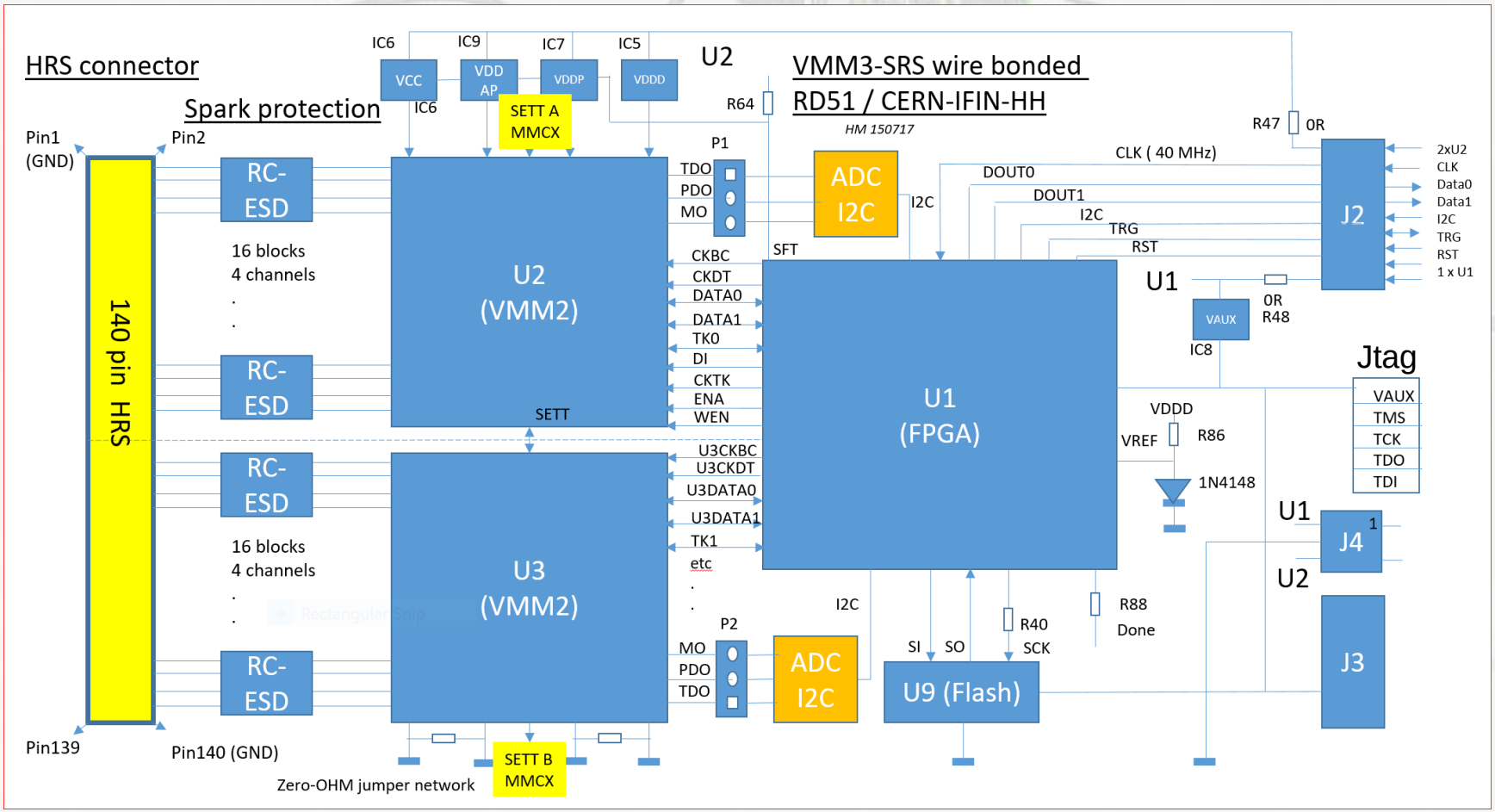
- No embargo
- Zero suppression
- Single ch. hit rates 5 MHz
- 10 bit peak resolution
- ns timing resolution
- clustering logic
- 8 different CSA gains
- 4 different shaping times
- Noise ~ 3000 e- for C_{det} = 200pF

CON

- 64 channels per chip (APV =128)
- 2x power/ chip compared to APV
- Cooling is an issue
- Availability in wafers (min25 ~ 50kEu)
- ADC dead time ~ 200 ns

*0.13 micrometer CMOS

SRS hybrid design (RD51)

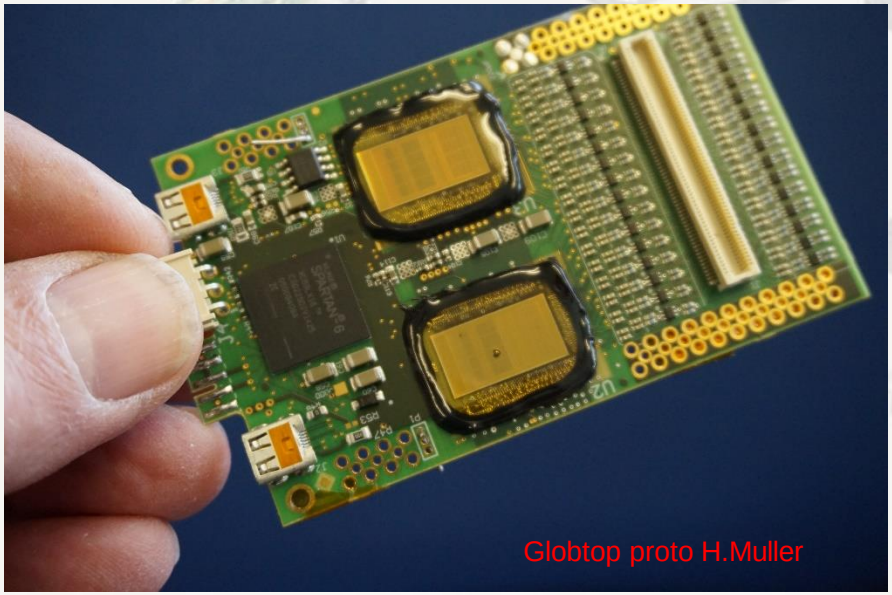


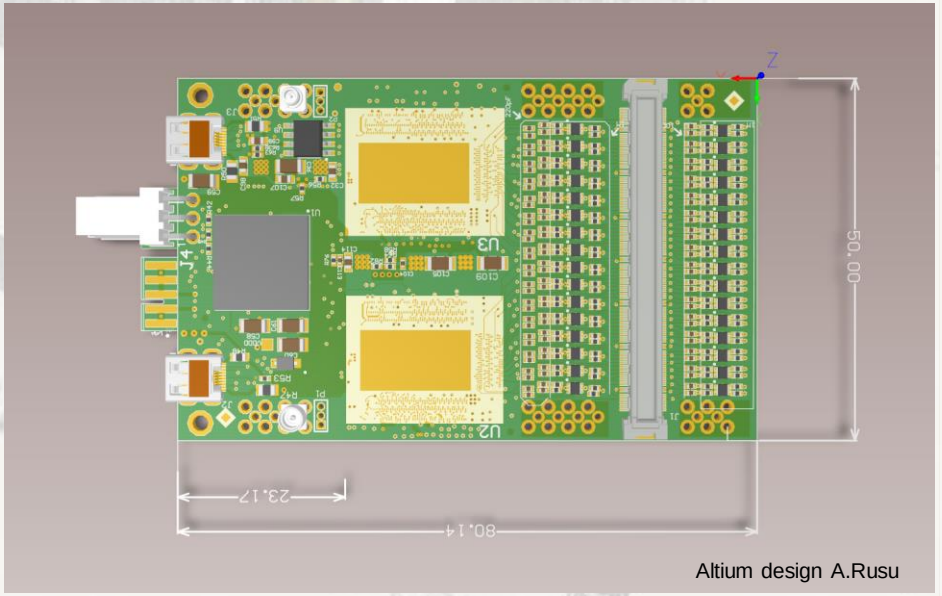
VMM hybrid finalization

(V4 with VMM3a)

VMM3 hybrid proto Nov 2017
Wire-bonded globtopped Panasonic connector

VMM3a hybrid in preparation for 2018
Wire-bonded globtopped, HRS connector
Monitoring channel ADCs, MMCX neighbor plugs,
Master-Slave capability

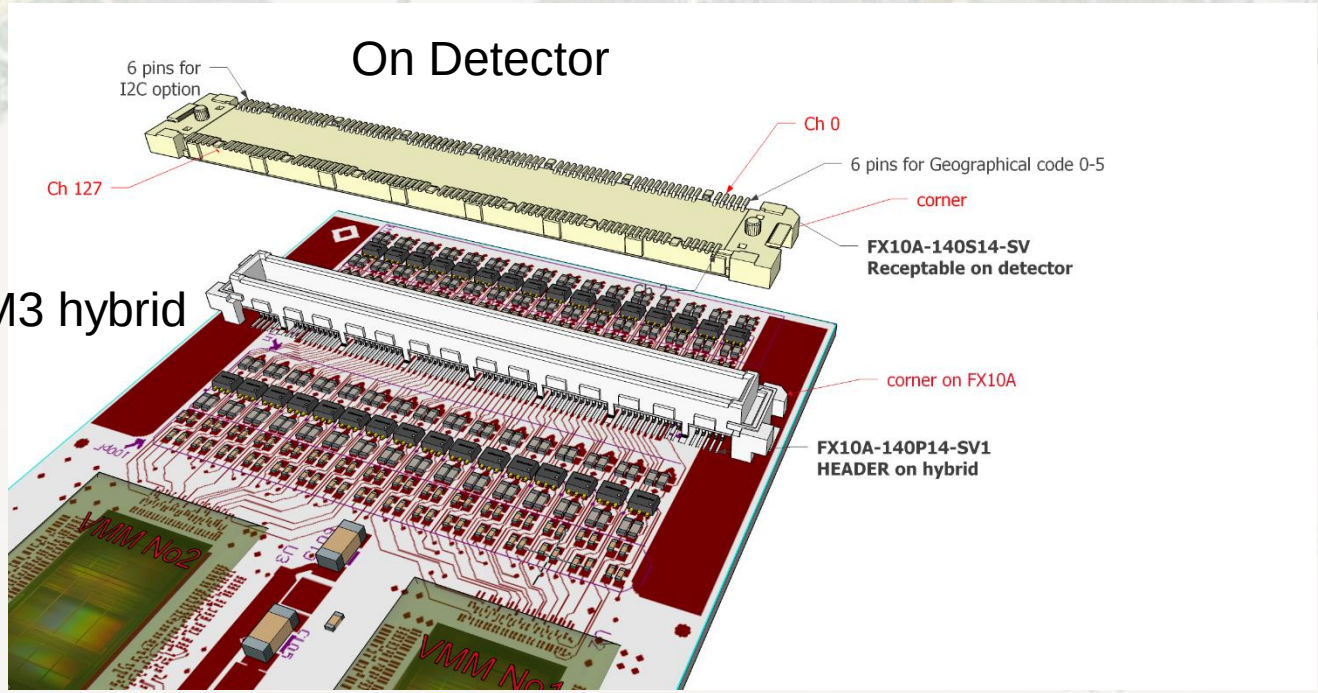




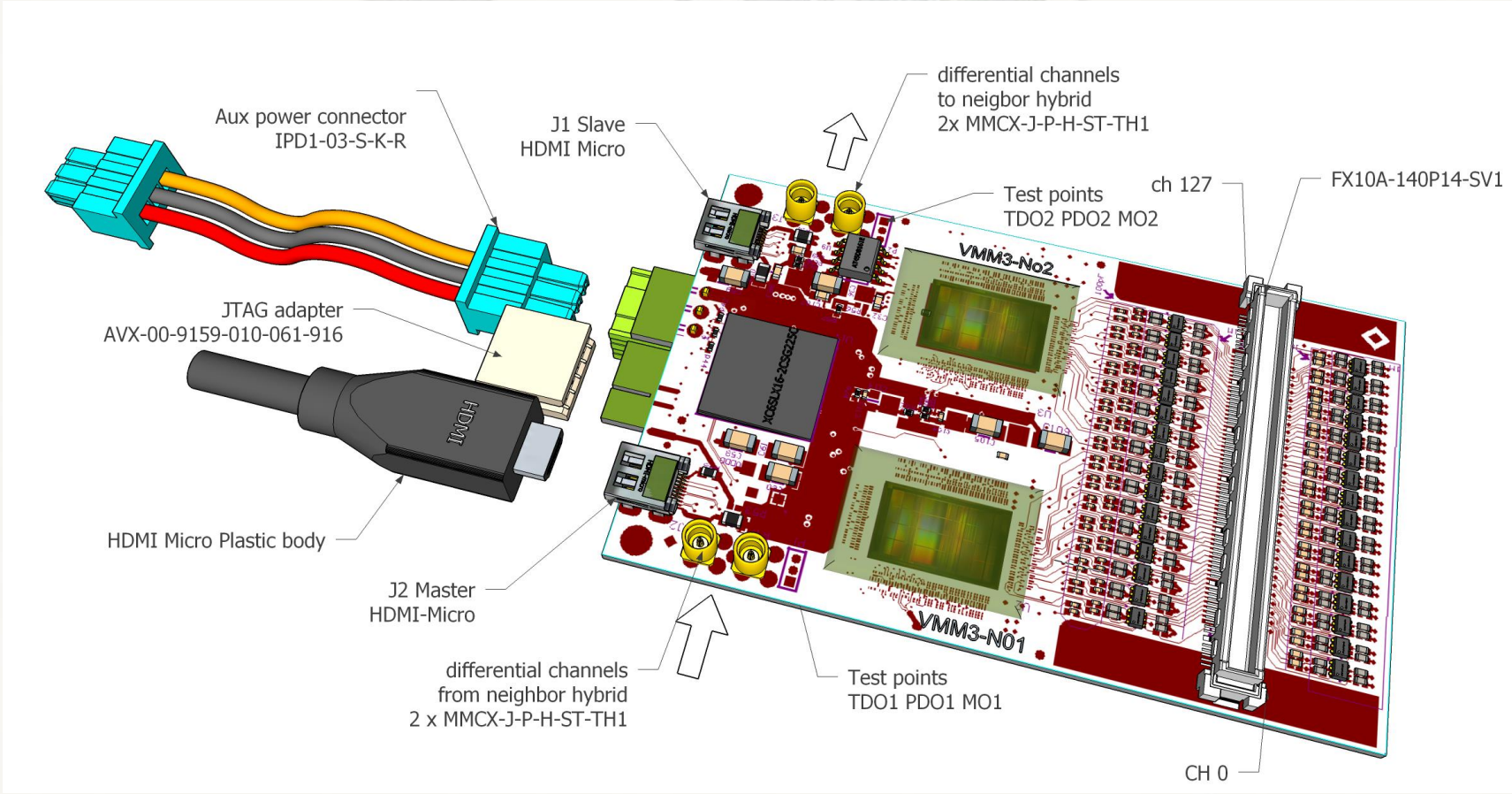
Note: globtop exceptionally transparent on 4 prototypes
will be black on all production hybrids

New HRS connector standard for MPGDs

starts with VMM hybrid V4



Connectors on V4 hybrid



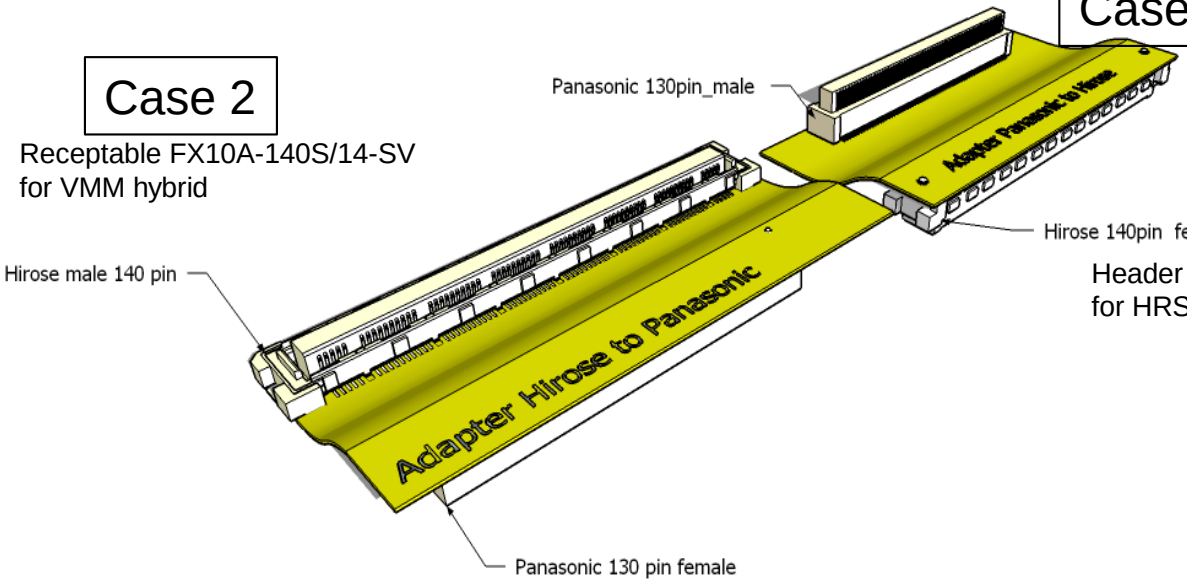
Adapters for the new MPGD connector

Case 1

receptable for APV hybrid

Case 2

Receptable FX10A-140S/14-SV
for VMM hybrid



Header FX10A-140P/14-SV1
for HRS receptable on detector

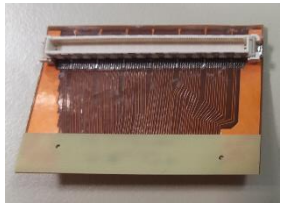


Photo Case 1 Proto (M.Bianco)

Socket for APV receptable on detector

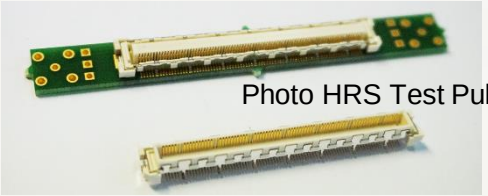
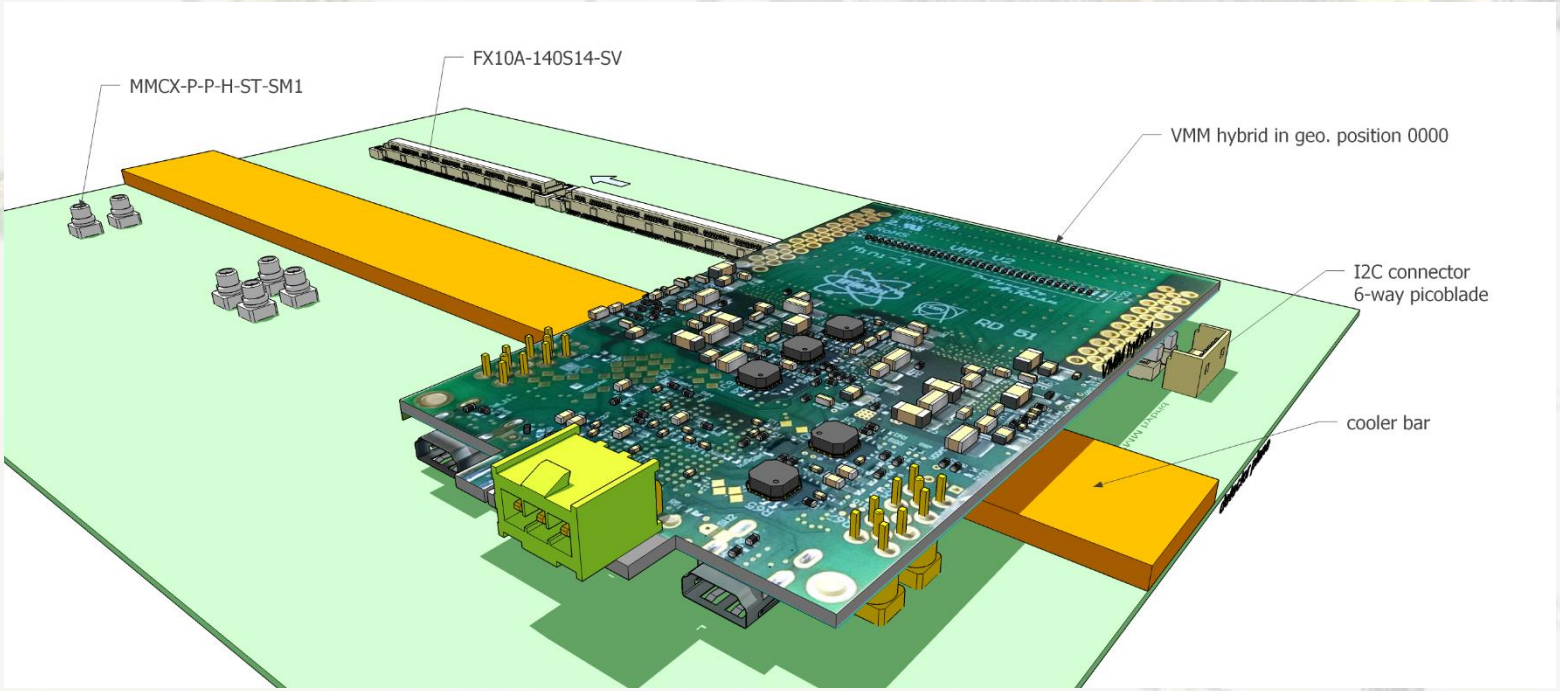


Photo HRS Test Pulse injector Proto (H.Muller)

Cooled VMM hybrids on detector frame

More on VMM cooling see talk by L. Scharenberg



DVMcard for SRS digital frontends

(like VMM)

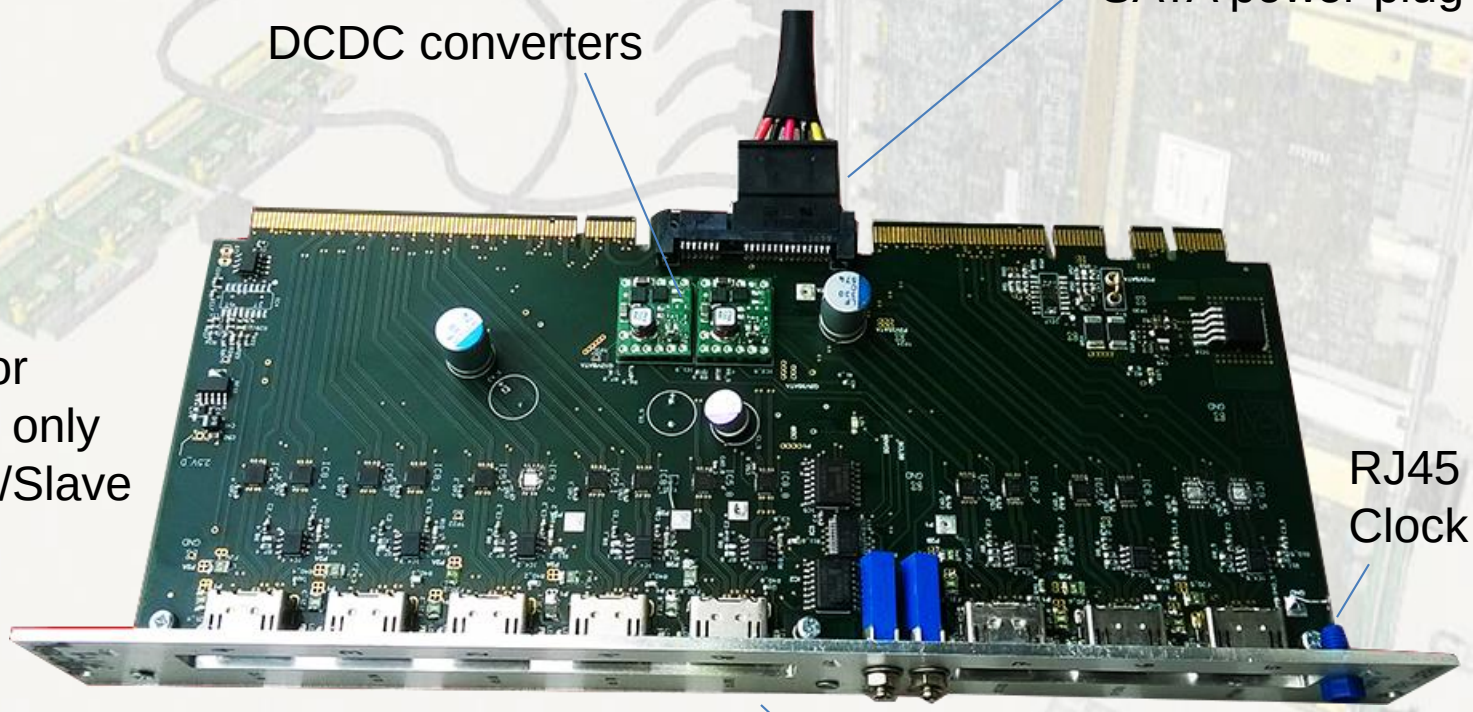
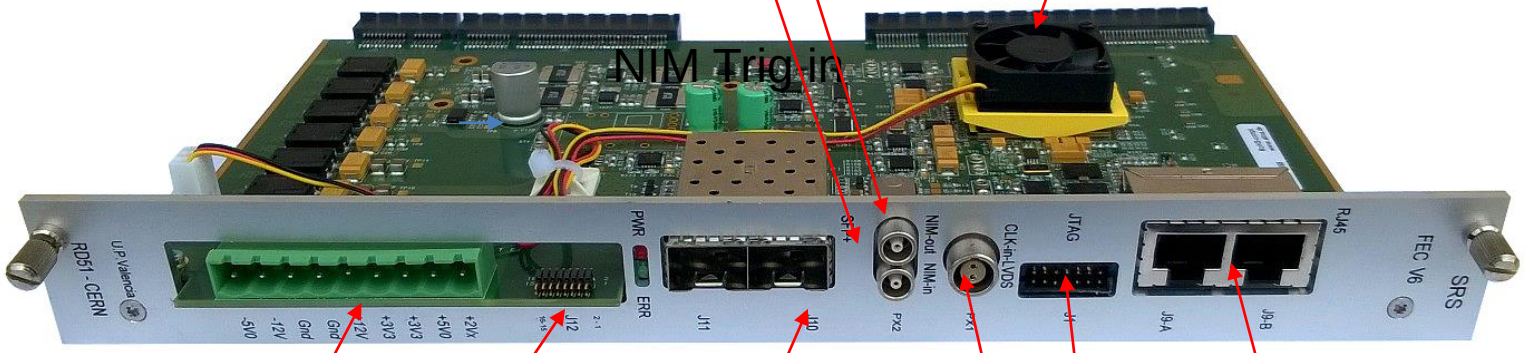


Photo DVM prototype (under revision by A.Rusu)

FEC V6 for APV and VMM readout*



3x PCIe connectors
DVMcard

Trigger OUT

Trigger IN

NIM Trig in

Virtex 6 LX130T FPGA

SRS power bus

programmable I/O
(User)

2 ports SFP+
1 Gbit Ethernet (UDP)
5 Gbit SRIO

Ext clock LVDS

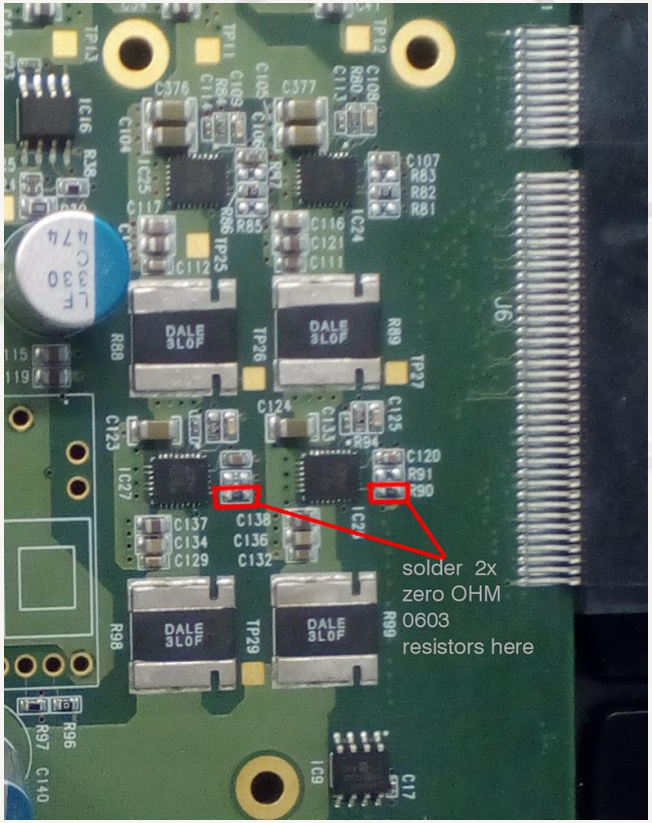
JTAG

2 ports RJ45
800 Mbps DTCC link SRU
800 Mbps link User

* different firmware for APV and VMM

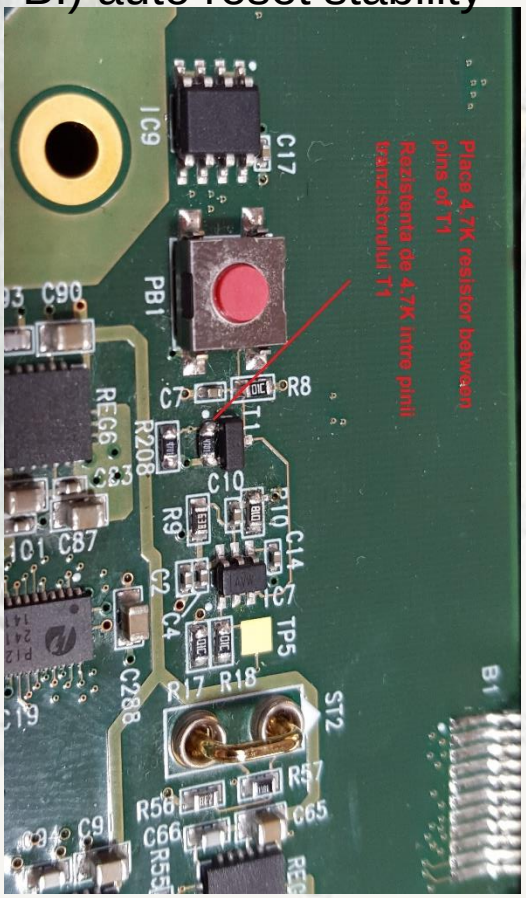
FEC-V6 resistor upgrades

A.) eliminate temperature-dependent ADC initialization problem on 4 ADC HDMI ports !!



-> add 2 x zero OHM resistors 0603
on FEC V6 until Oct. 17

B.) auto reset stability

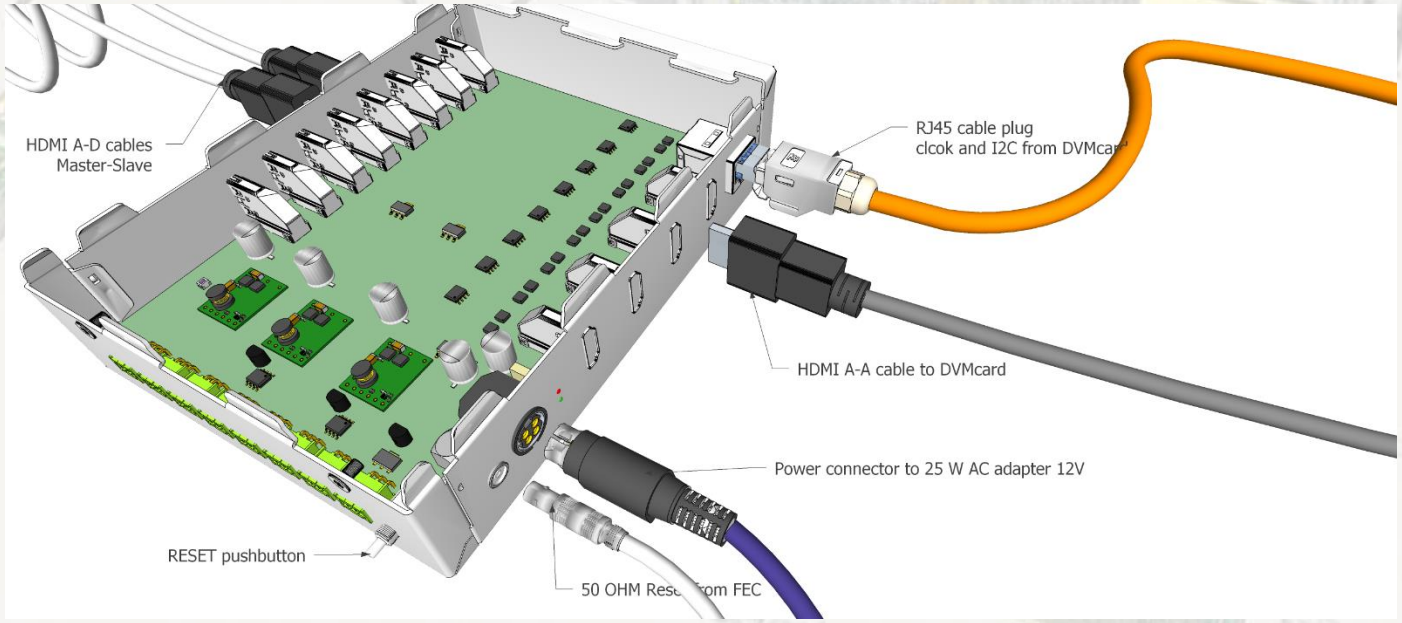


addition of one` 4.7K resistor 0603
(missing on FECs since Oct. 17)

Powerbox*

- Powerbox 1k design H.Muller
- Proto PCB design Univ. Bonn, J.Kaminski

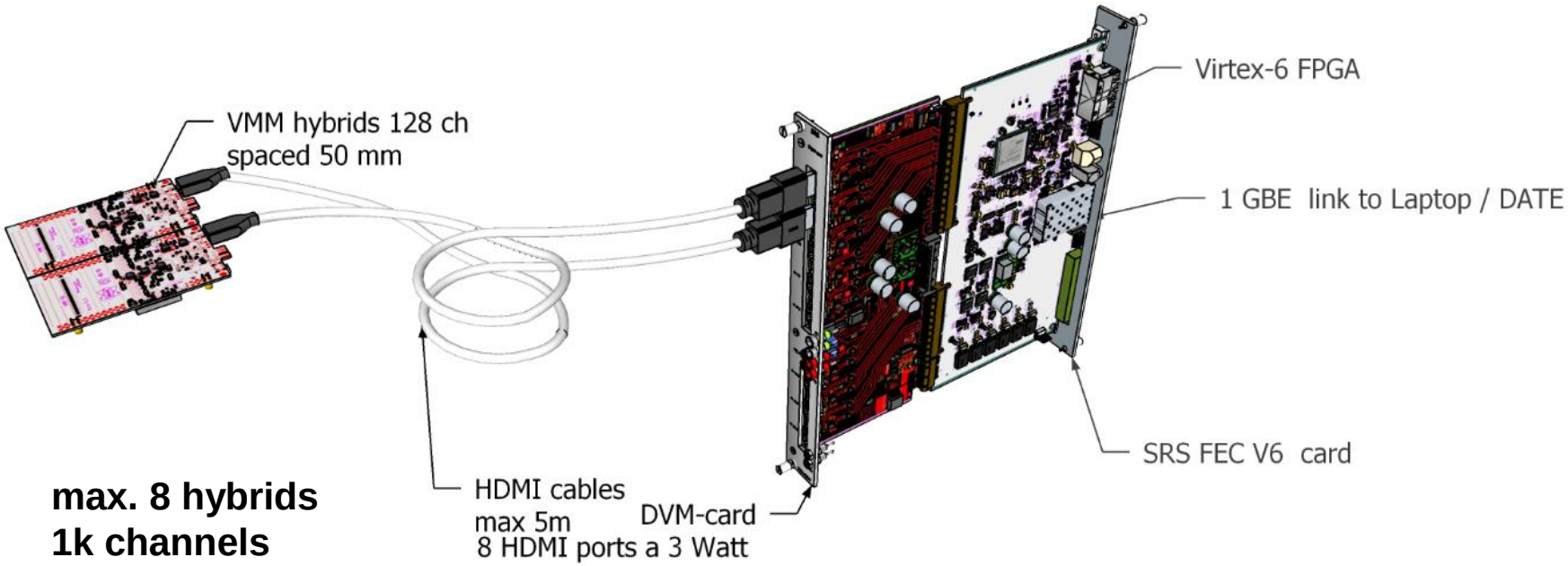
to VMM hybrids



required for:
-Master/Slave operation
-long cables to SRS frontend
-local power for hybrids

Note: Master-only operation possible with direct cables to DVMcard (max. 5m, max 8 hybrids)

Direct DVM connection
(master only)

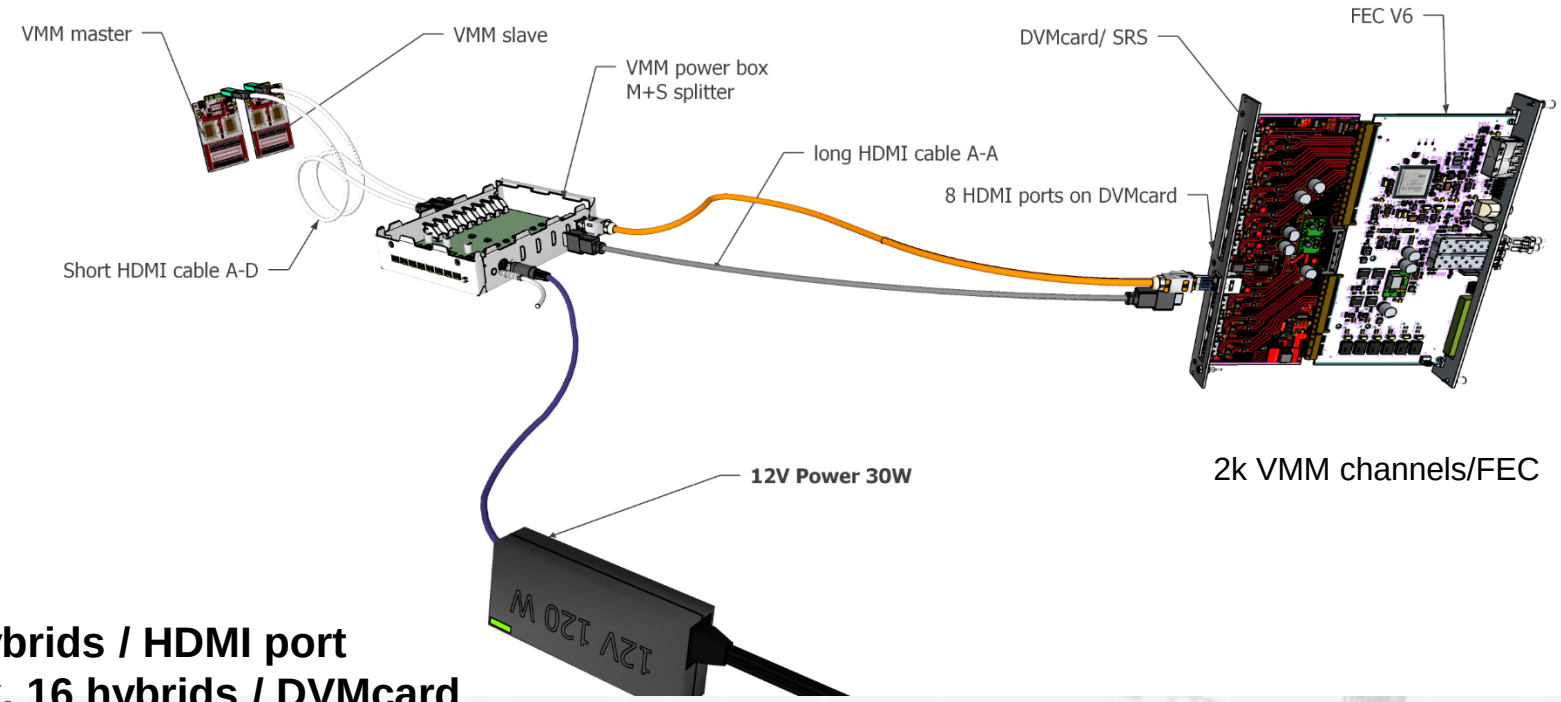


max. 8 hybrids
1k channels
(24 Watt)

1k VMM channels/FEC

Power/Splitter box

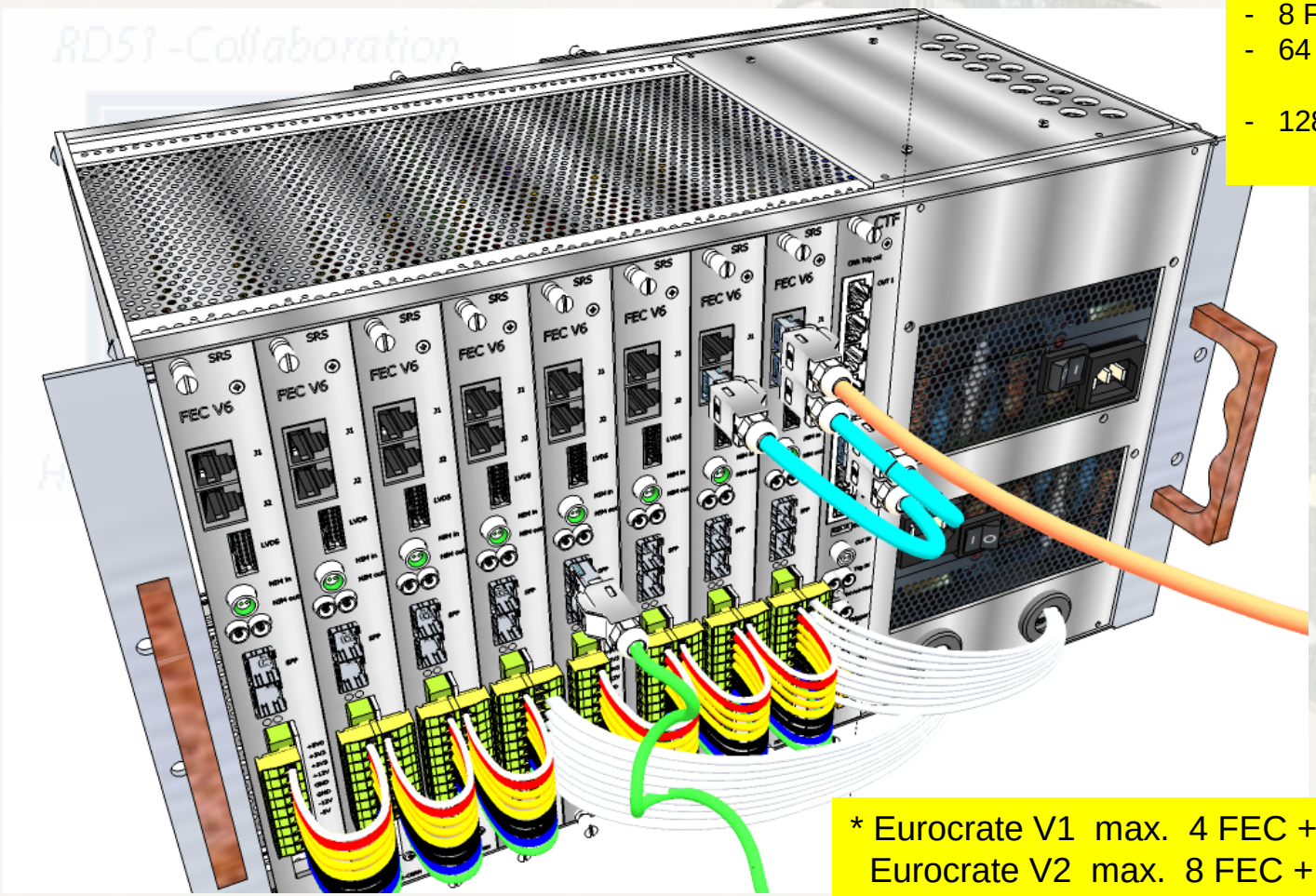
master + slave



2k VMM channels/FEC

2 hybrids / HDMI port
max. 16 hybrids / DVMcard
(48 Watt provided by powerbox)

SRS Eurocrate V2*



max. channel + power capacity:
- 8 FEC + 8 DVMcards + 1 CTF
- 64 VMM masters direct (8192 ch)
- 128 VMM M+S , 8 Powerboxes (16384 ch)

* Eurocrate V1 max. 4 FEC + 4 adapter cards + 1 CTF
Eurocrate V2 max. 8 FEC + 8 adapter cards + 1 CTF

SRS in 2018

- Phasing down of APV frontends:

  remaining APV hybrid stock O(500)

- Phasing up new VMM frontends + new connector

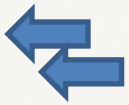
  actions and decisions:

  I. Organize VMM 3a wafer purchase (join BNL order 03/18)
  II. Develop FW + SW on 3 pilot systems for GDD lab
  III. Finalize HW upgrades, DVMcard, EUcrate V2, Powerbox
  IV. Interact with companies + CERN store for product readiness
  V. Support pilot applications, coordinate user experiences

planning sheet for SRS with VMM frontend

teams	country/town	Detector Name, type	Discussions/ Documents	VMM hybrids short term	VMM hybrids long term	% VMM chips short term	% VMM chips long term
REV 29112017							
ESS	**SE, Lund**	NMX, Neutrons, GEM	INDICO: BrightnESS task T4.1	***50***	***156***	110	343
USTC	**CN, Hefei**	Cosmic Telescope , GEM		***0***	***156***	0	343
Bonn Univ. Physics	**GE, Bonn**	Neutron, GEM		***6***	***65***	13	143
Mainz Univ, Physics	**GE, Mainz**	MAGICs, MM		***16***	***195***	35	429
Budker	**RU, Novosibirsk**	uWELL		***2***	***20***	4	44
INFN	**IT, Trieste**	Lab MPDs		***10***	***0***	22	0
Univ. o. Tsukuba	**JP, Tsukuba**	FOCAl, Si pads		***2***	***48***	4	106
GDD lab CERN	**CH, Geneva**	MPGDs, GEM+MM	INDICO: GDD meetings	***16***	***0***	35	0
Peking Univ. HEP	CN, Bejing	CMS GEM upgrade		4	48	9	106
LMU-HEP	**GE, Munich**	**Ion Tomographie, MM**		*8*	*0*	18	0
LMU-Medphysics	**GE,Munich**	**MPGDs, Si**		**8**	**40**	**18**	**88**

Total VMM hybrids short term =	**122**
Total VMM hybrids long term =	**728**
Total VMM ASICs (+10%) short term =	**268**
Total VMM ASICs (+10%) long term =	**1602**
Total VMM wafers short term =	**3**
Total VMM wafers long term =	**13**

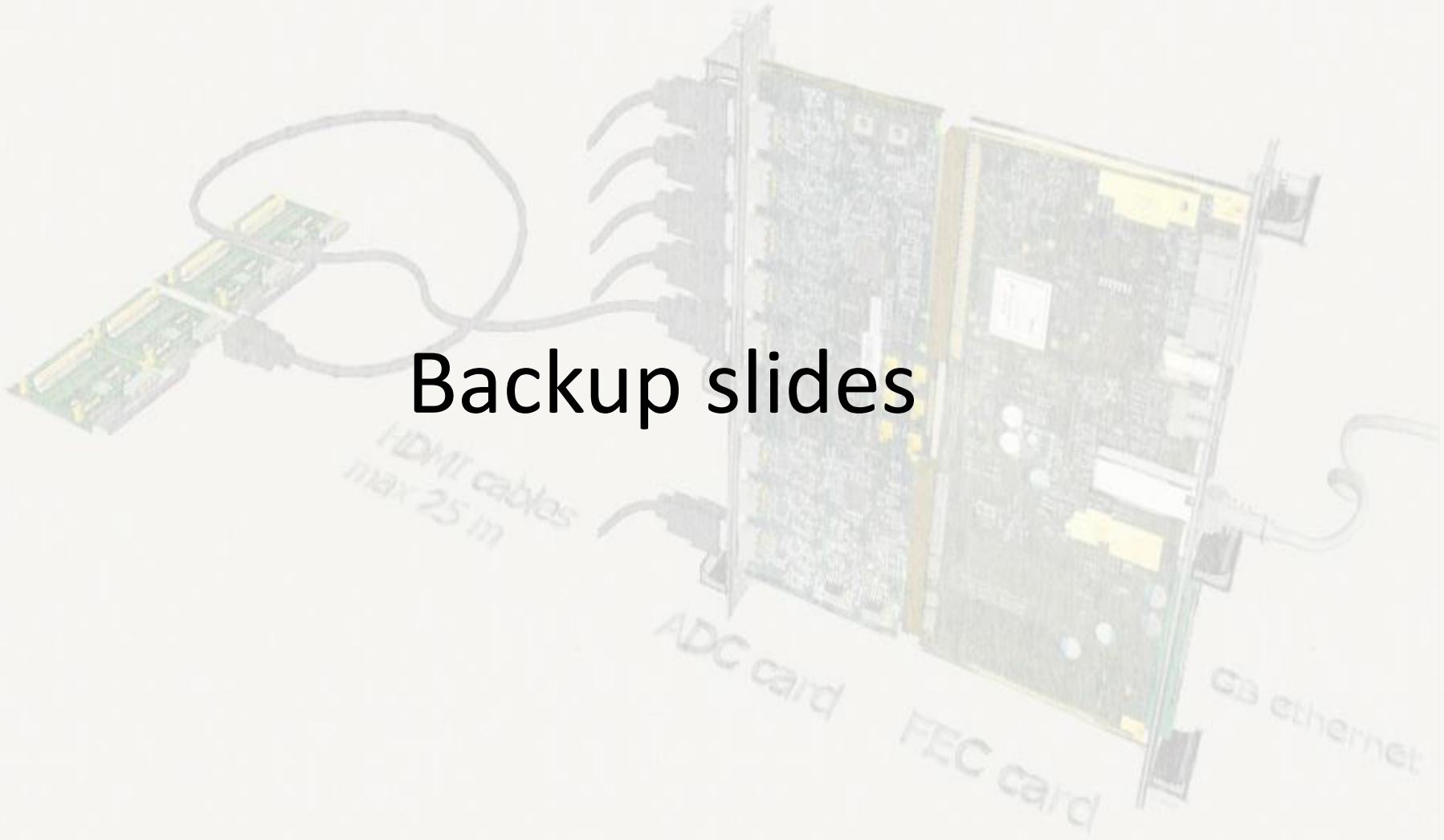


VMM SRS system requests

and preliminary budgetary channel cost (excl. TVA)

	Short term channels	Long term channels	long term channel cost	short term channel cost
			Eu	EU
ESS	6400	19968	2.5	5.0
USTC	0	19968	2.5	
Bonn Univ. Physics	768	8320	3.2	11.3
Main Univ, Physics	2048	24960	2.5	8.5
Budker	256	2560	3.4	26.8
INFN Trieste	1280	0		
Univ. o. Tsukuba	256	6144	2.9	26.8
GDD lab CERN	2048	0		8.5
Peking Univ. HEP	512	6144	2.9	15.1
LMU-HEP	1024	0		9.3
LMU-MedPhysics	1024	5120	2.6	9.3
SHORT TERM Totals	Total Nr of VMM channels	Total Nr of VMM channels		
	15616	93184		

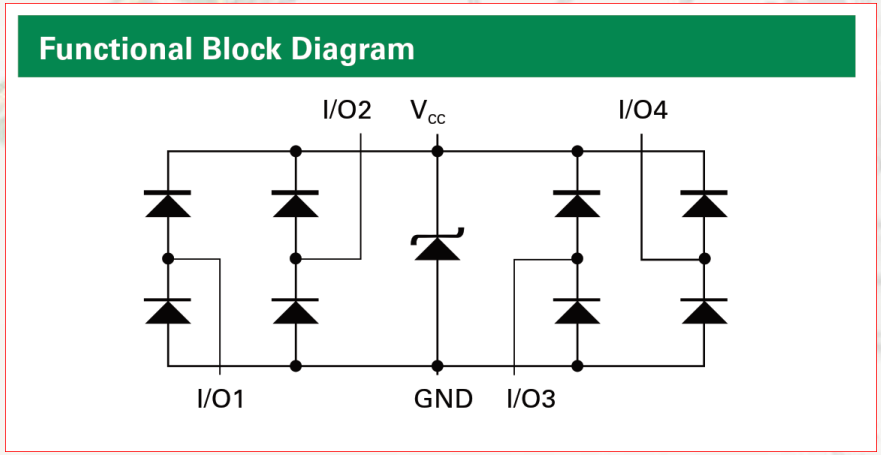
Compare to APV ~ 1.9 EU



Backup slides

Spark protection diodes on VMM3 hybrid

SP3004: quad protection in single SOT563 package*



- 0.85 pF per I/O
- max 1nA leakage @ 3V3
- air discharge safe +- 15 kV
- IEC 61000-4-4, 40A (5ns/50ns)

Same package as NUP4114 diodes used on APV hybrids (Vcc =5V), SP3004 works at lower voltage (Vcc = 3V3)

Scalable Readout Units (SRU)