Status of the readout for the ALICE TPC upgrade

14th December 2017

Christian Lippmann

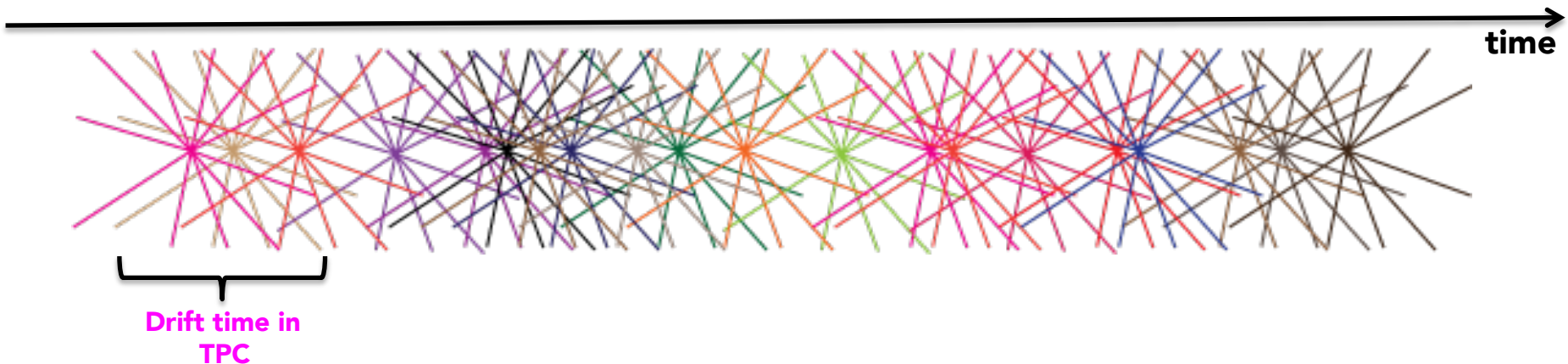GSI

ALICE TPC overview

Central HV electrode

High precision, low mass field cage
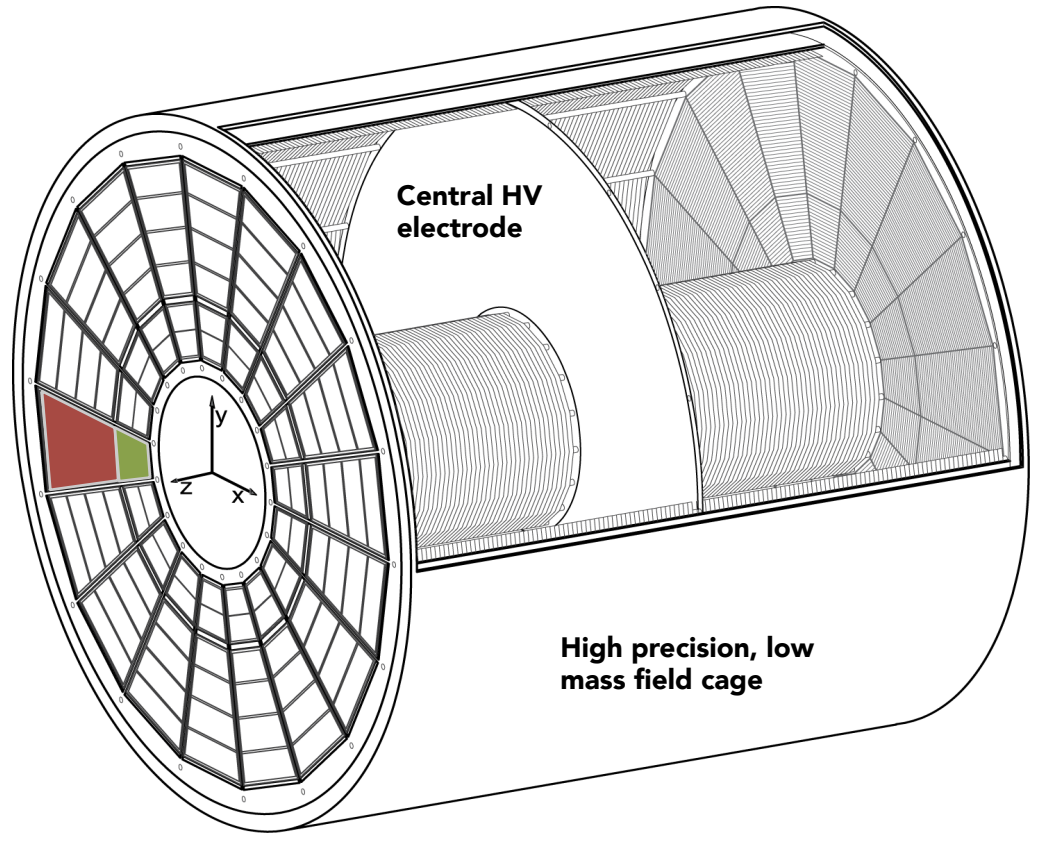
- **Diameter: 5 m, length: 5 m**
- **Gas:**
  - **Ne–CO_2–N_2,**
  - **(Ar–CO_2 in 2015, 2016 and 2018)**
- **Max. drift time: ~100 μs**
- **18 sectors on two sides**
- **Inner readout chambers: IROC**
- **Outer readout chambers: OROC**

Continuous operation

Typical data taking with TPC in RUN3**: High luminosity Pb-Pb collisions**

time

Drift time in
TPC

- Maximum **drift time of electrons in TPC: ~ 100us**
- **Average event spacing: ~20us**

- Event pileup
- Triggered operation does not make sense
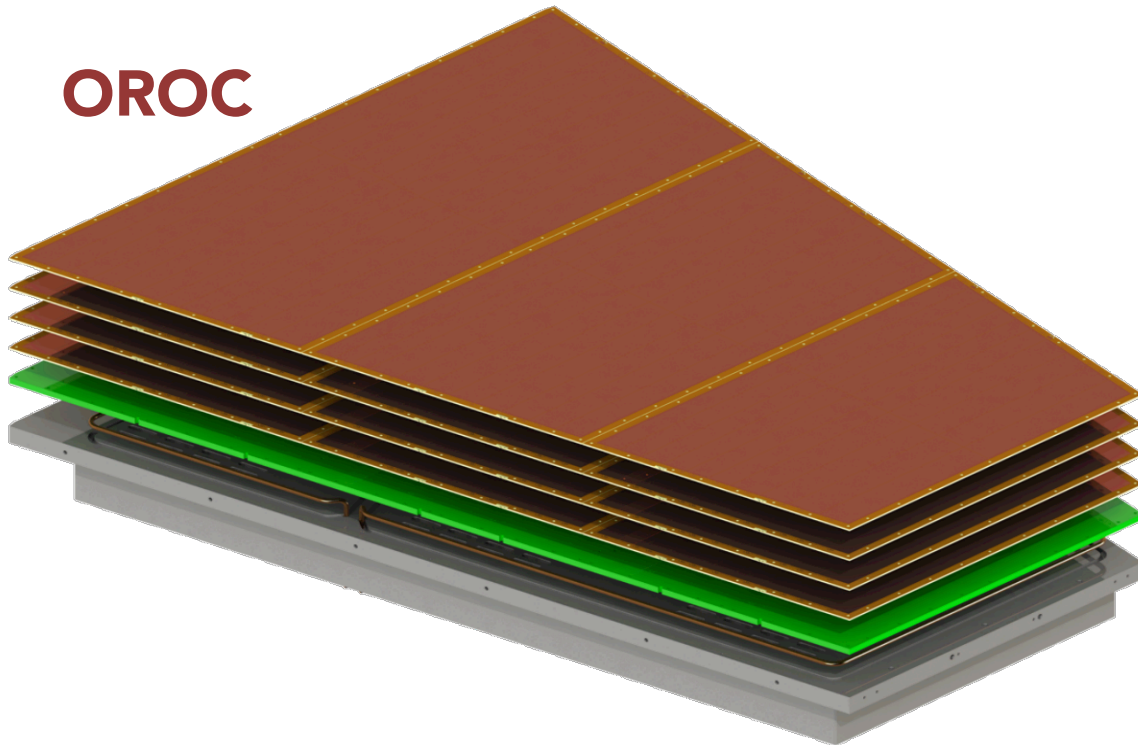- Minimize ion backflow (IBF) in different way
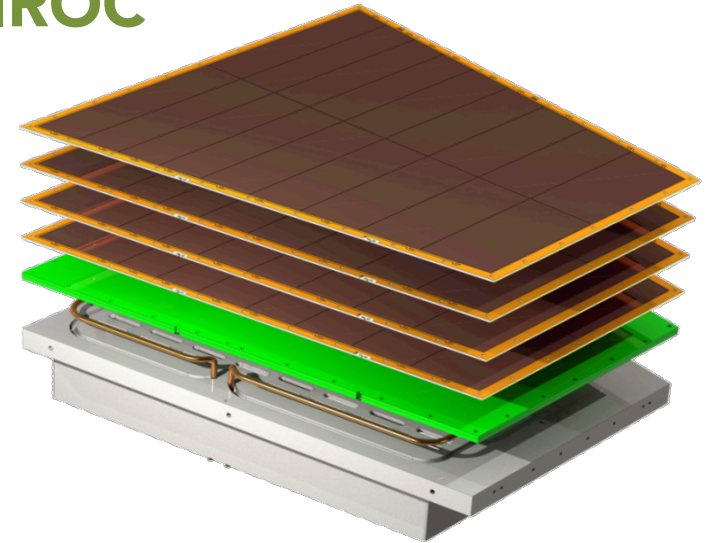
**Continuous read-out
Micro Pattern Gas Detectors**

New Readout chambers

- **Continuous read-out required:**
  - ➔ **No gating possible**
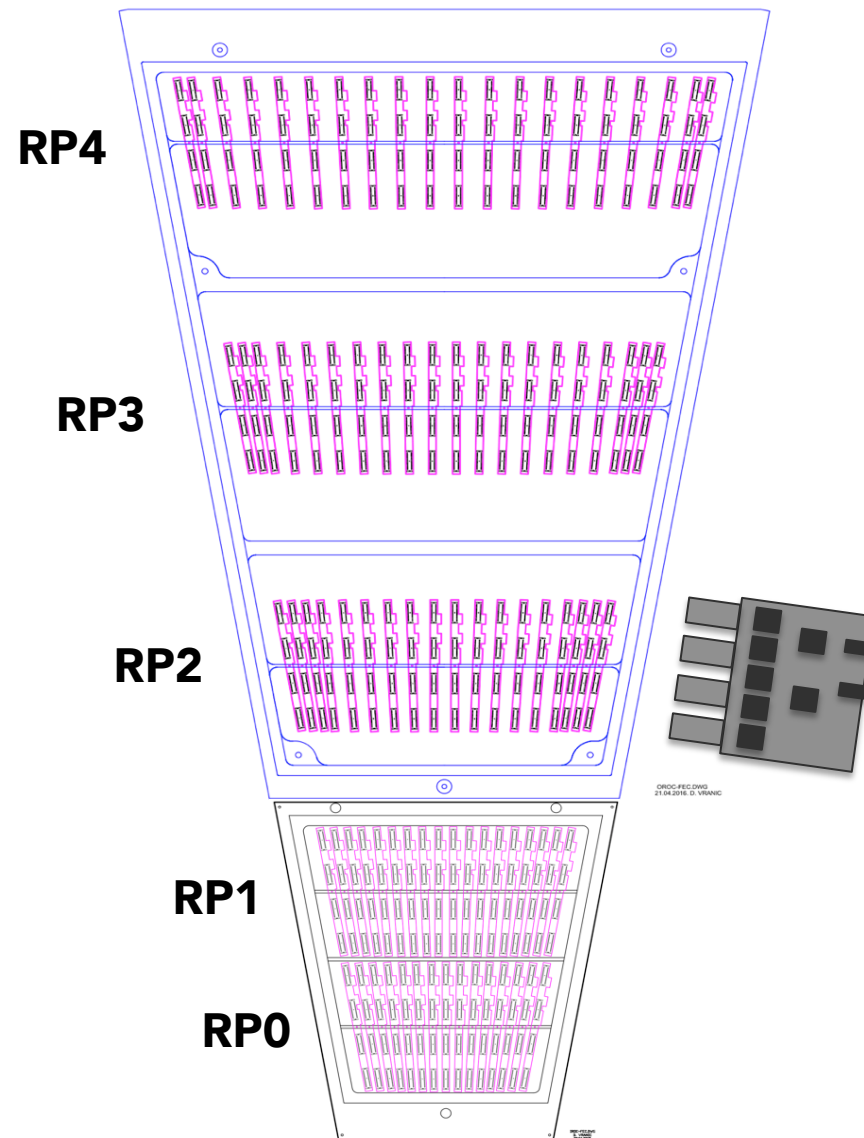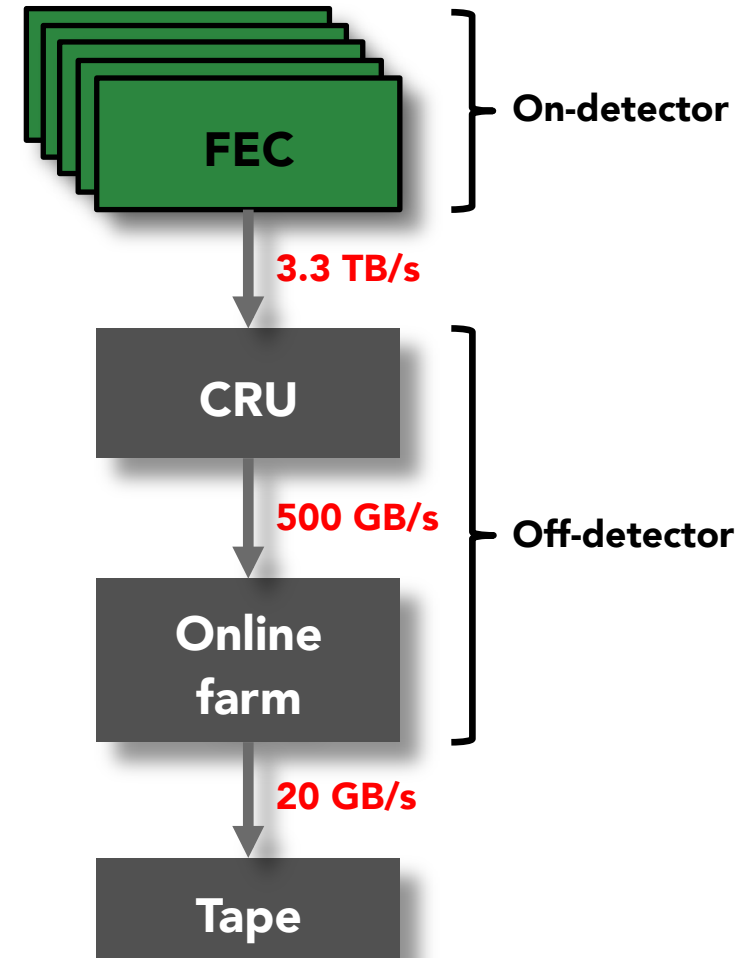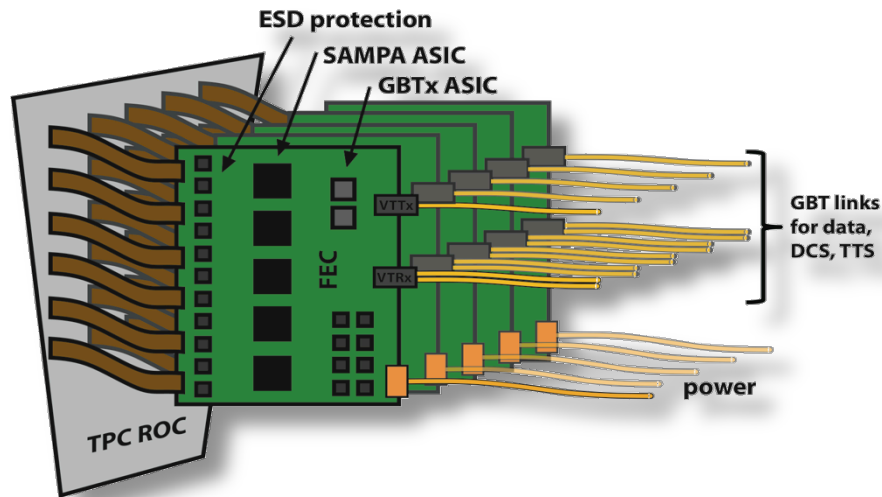 - ➔ **4-GEM stacks with low ion backflow**

OROC

IROC

TPC sector layout

- **FEE is arranged in 18 sectors on 2 sides**

- **Each sector has 5 readout partitions with up to 20 Front End Cards (FECs) each**

- **FECs are held by separae "Service Support Wheel"**

- **Weight of FEE is decoupled from TPC through flexible signal connectors**

Readout strategy

- **Continuously read all ADC values** (**no compression**)
- **Radiation hard** data and control link: CERN **GBT system**
- **Online data correction** (baseline fluctuations, common mode effect) and cluster finding in CRU (FPGA based readout card)
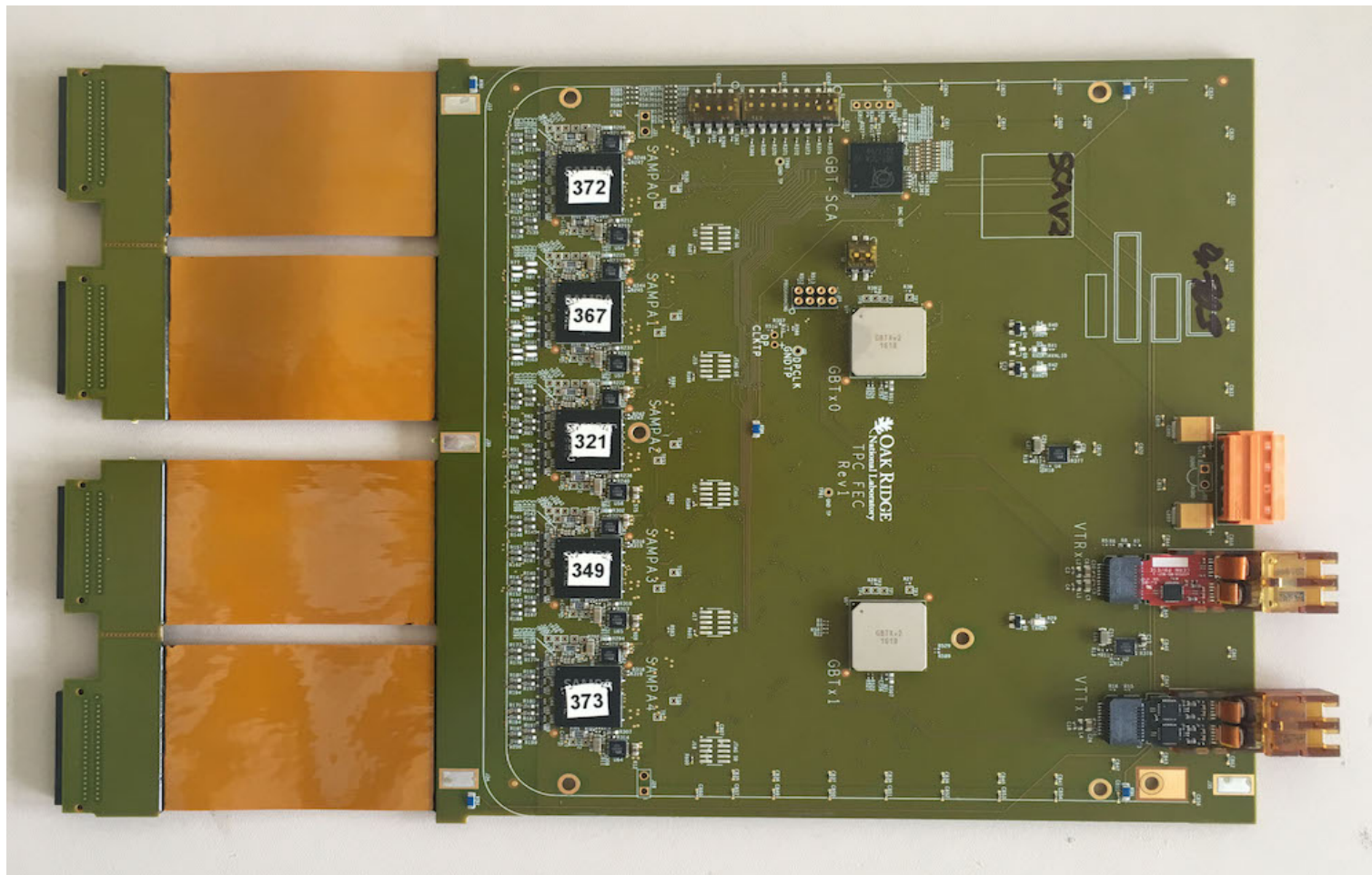

FEC — On-detector

3.3 TB/s

CRU

500 GB/s — Off-detector

Online farm

20 GB/s

Tape

ESD protection
SAMPA ASIC
GBTx ASIC
FEC
VTTx
VTRx
GBT links for data, DCS, TTS
power
TPC ROC

Front End Card schematic

- **Front-End ASIC: SAMPA**
- **On the FEC:**
  - **160 FE channels**
  - **5 SAMPAs**
  - **2 GBTx**
  - **1 GBT-SCA**
  - **1 VTTx**
  - **1 VTRx**
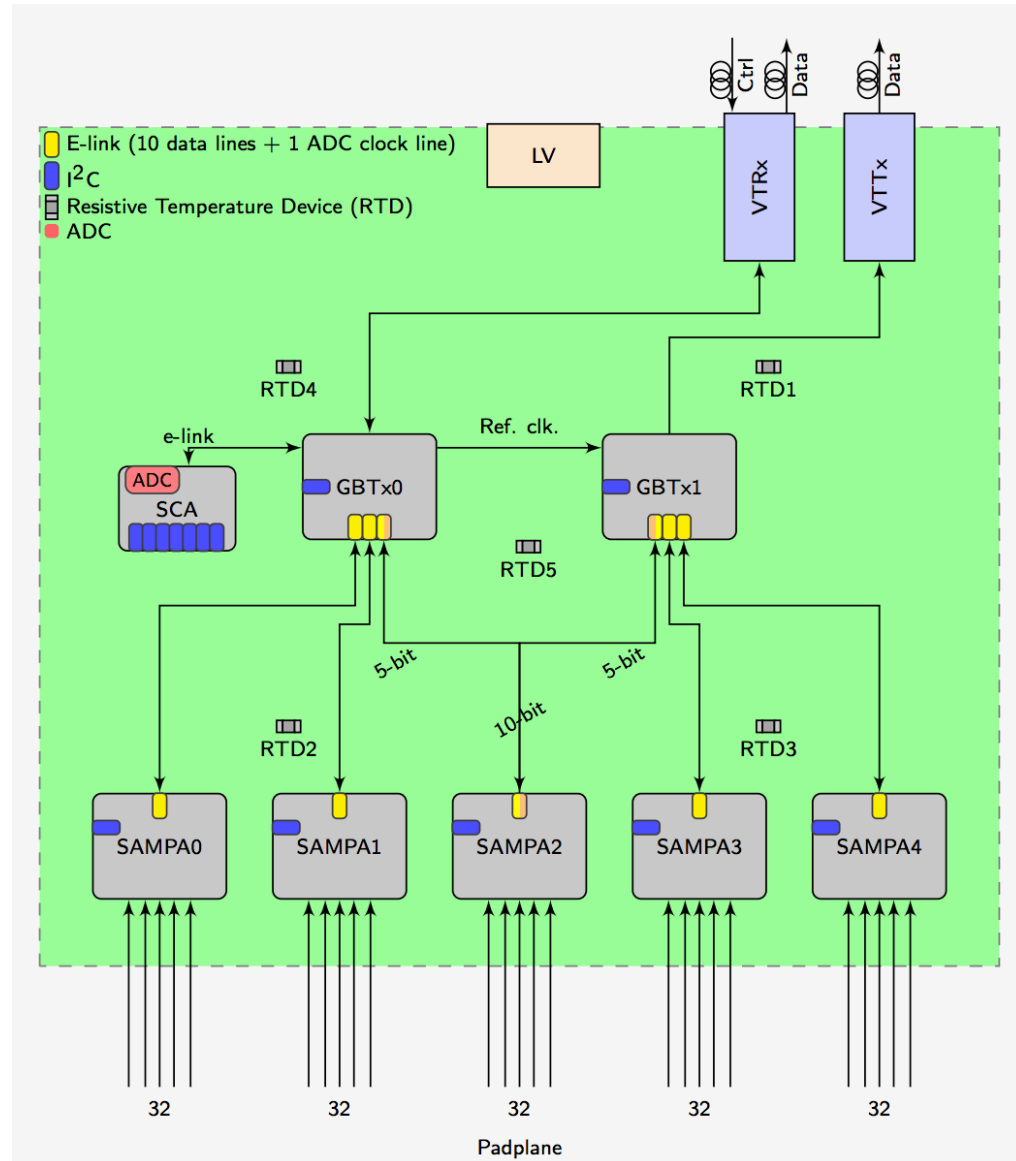
Almost final FEC (1)

TPC Front End Card Rev 1 with integrated flexible signal cables (rigid flex)
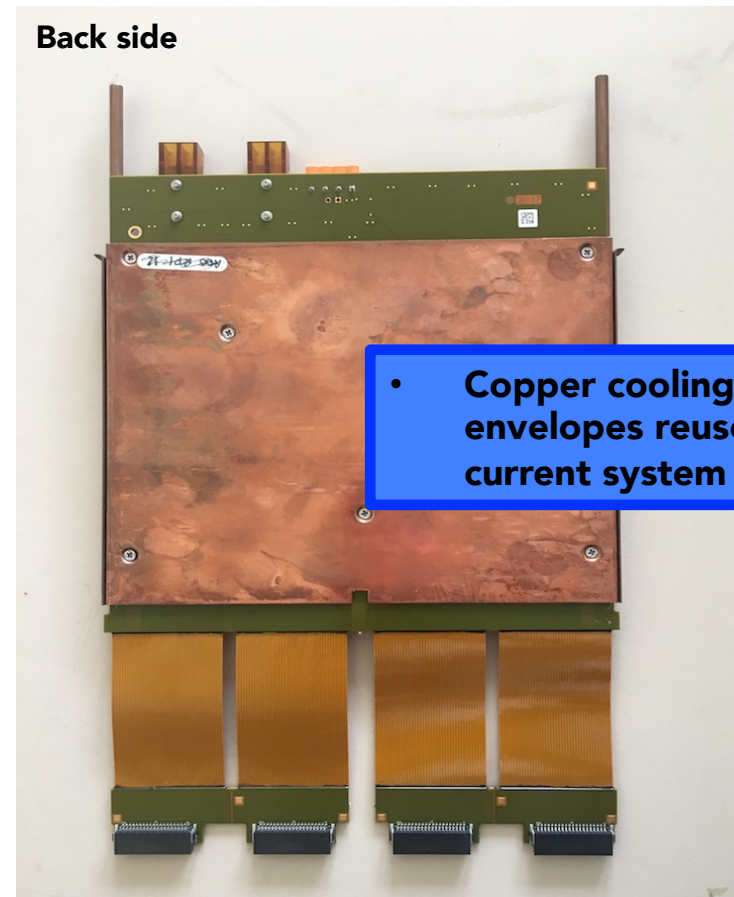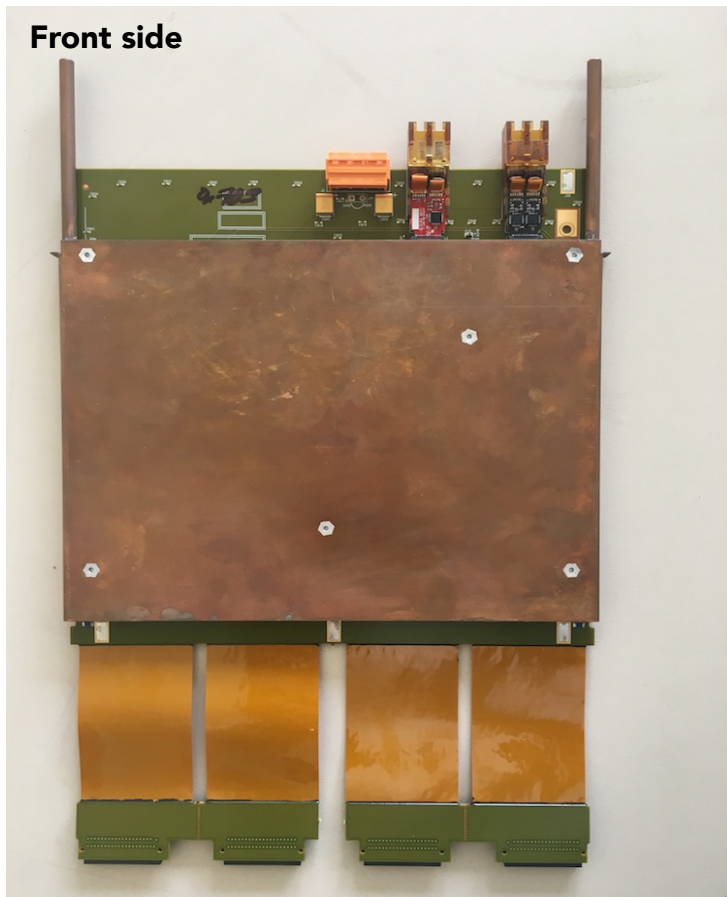
Almost final FEC (2)

TPC Front End Card Rev 1 with integrated flexible signal cables (rigid flex)

FEC integration (1)

- **FECs are installed into water-cooled copper envelopes**

Front side

Back side

- **Copper cooling envelopes reused from current system (Run2)**

FEC integration (2)

- **Decouple weight of FEE from detector to avoid mechanical deformation by use of flexible signal cables (as in RUN2)**

Current FEE on TPC

FEC in copper cooling envelope

FEE is supported by "Service Support Wheel" (SSW)
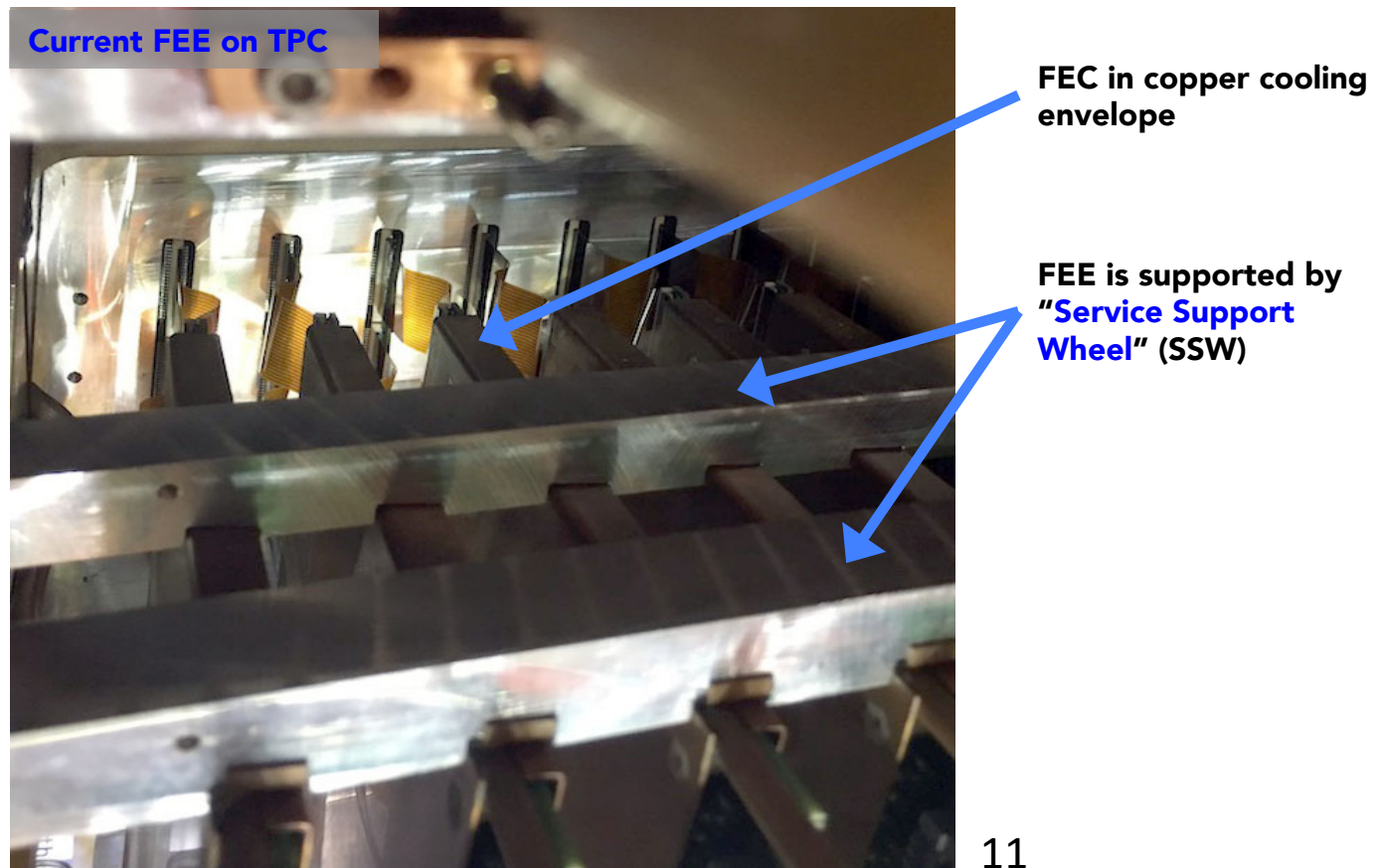
SAMPA overview (1)

- **SAMPA was designed by Sao Paulo University (Brasil) and Bergen University (Norway) for ALICE TPC and MCH systems**

  - TSMC CMOS 130 nm, 1.25V technology
  - 32 channels, Front-end + ADC + DSP
  - package size ≤15x15mm^2 (total footprint)
  - ADC: 10-bit resolution, 10MS/s, ENOB>9.2
  - DSP functions: pedestal removal, baseline shift corrections, zero-suppression
  - Data transmission: up to 11 e-link at 320 Mbps to GBT, SLVS I/O
  - Power < 32 mW/channel (Front End + ADC)

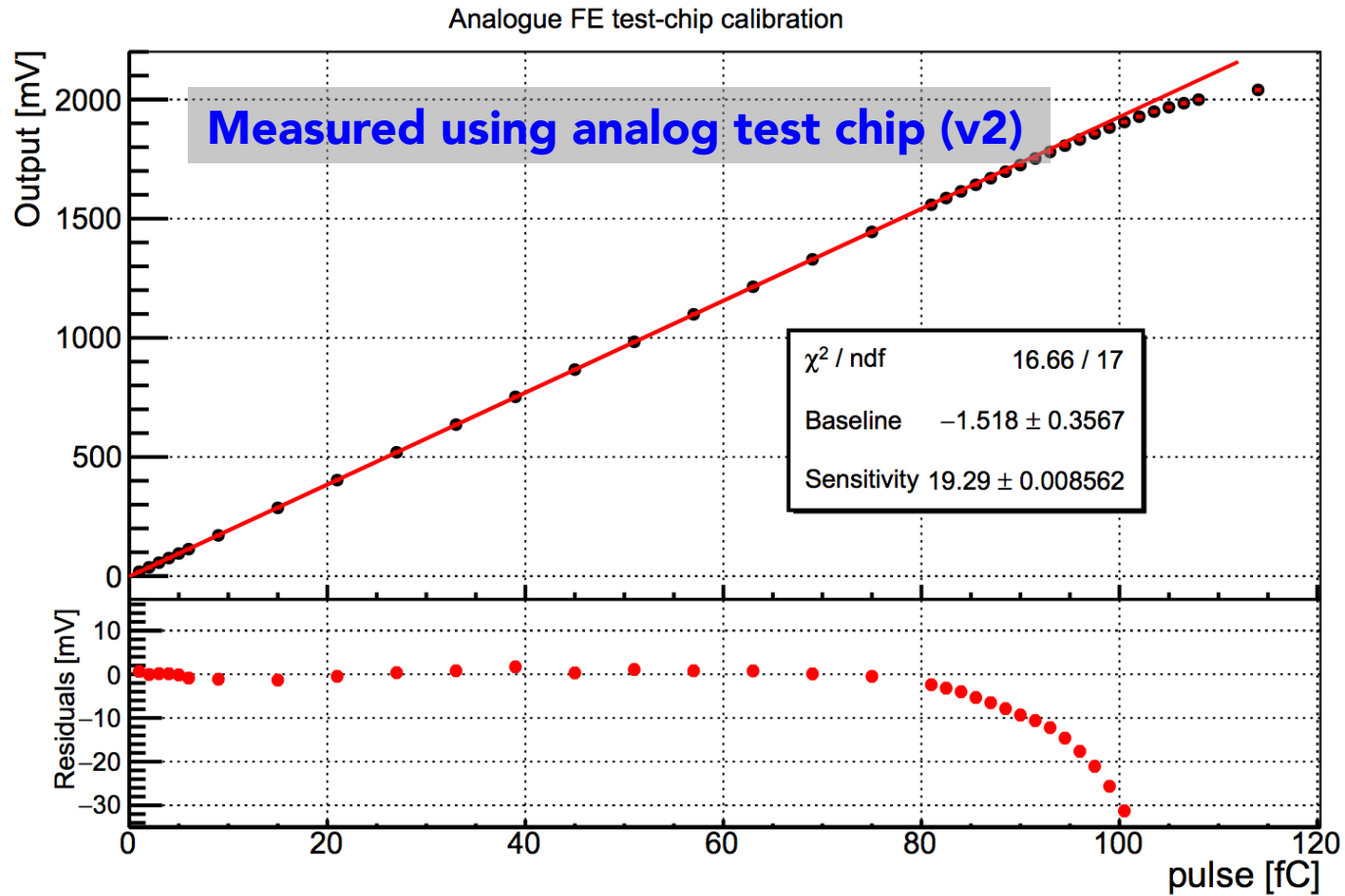| TPC Mode	MCH Mode
▪ Negative Input charge	▪ Positive input charge
▪ Sensor capacitance: 12 – 25 pF	▪ Sensor capacitance: 40–80 pF
▪ Sensitivity: 20mV/fC & 30mV/fC	▪ Sensitivity: 4mV/fC
▪ Noise: ENC ≤ 580 e$^-$ @ 18.5pF	▪ Noise: ENC ≤ 950 e- @ 40pF
▪ Peaking time: ~160 ns, return to	1600 e- @80pF
▪ Baseline return: <500 ns	▪ Peaking time: ~300 ns
	▪ Baseline return: <550 ns

SAMPA overview (2)

- **Analog FE, ADC and DSP all in one substrate, in a small package**
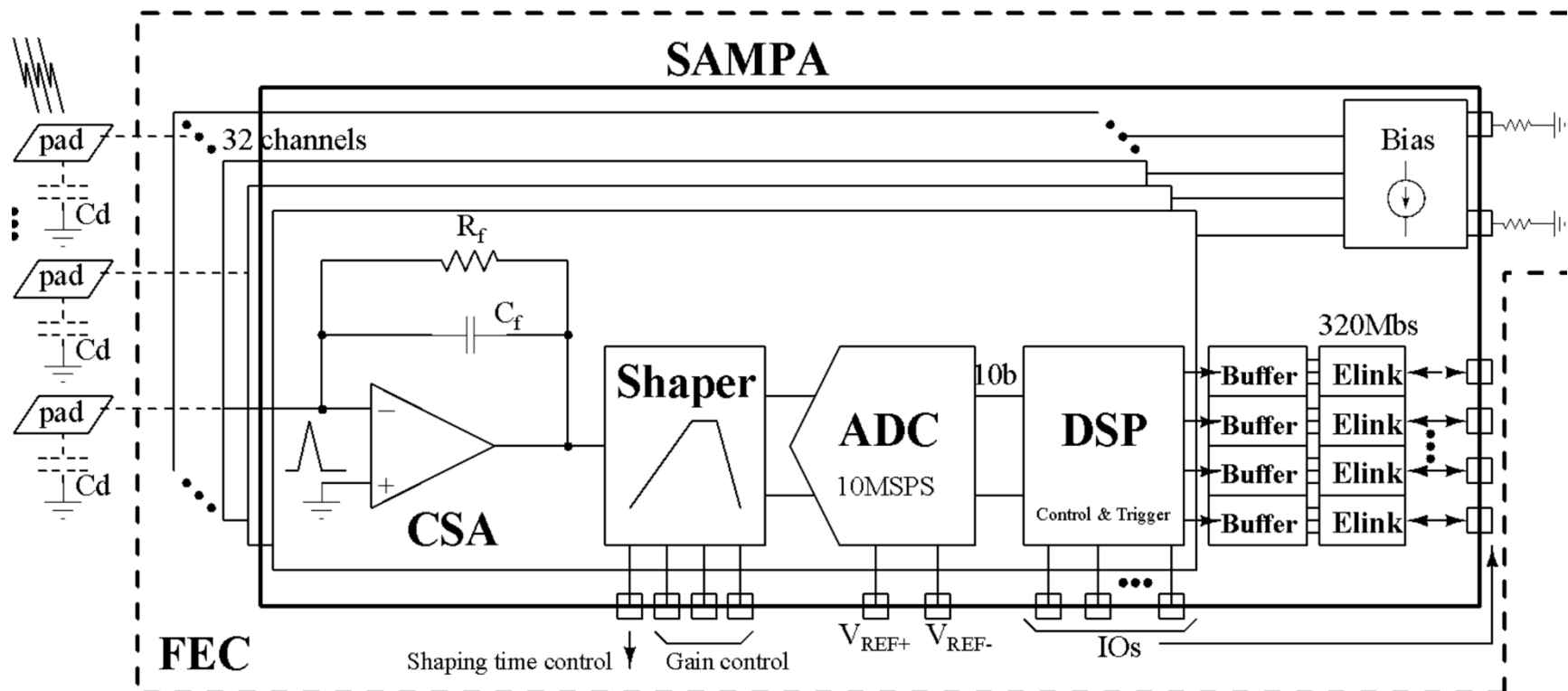
SAMPA versions: Overview

- **v2**
  - **problem with band-gap and ADC linearity**
  - **prone to Single-Event-Latchups (SELs) in the pedestal memory**
  - **saturation of CSA (9-10 nA) quite close to current expected on pads**

  Fully characterized in 2016/17

- **v3**
  - **band-gap fixed (but can also be overwritten by external voltage)**
  - **ADC improved**
  - **SEL fixed (by using well known memory cell technology)**
  - **saturation of CSA issue remains**

  Both versions under test. Potentially final

- **v4**
  - **submitted at the same time as v3**
  - **same as v3 but with factor 3 margin for CSA saturation (30 nA)**
  - **FE noise increase by ~ 4%**

Linearity

Analogue FE test-chip calibration

Measured using analog test chip (v2)

χ^2 / ndf	16.66 / 17
Baseline	-1.518 ± 0.3567
Sensitivity	19.29 ± 0.008562

- **Non-linearity < 0.1% up to about 80% of the range**
- **Non-linearity < 0.5% up to about 90% of the range**

Noise analog front end

Measured using analog test chip (v2)

Noise Analogue FE chips: 4mV/fC Pos Ch8->15

Noise Analogue FE chips: 20mV/fC Neg Ch8->15
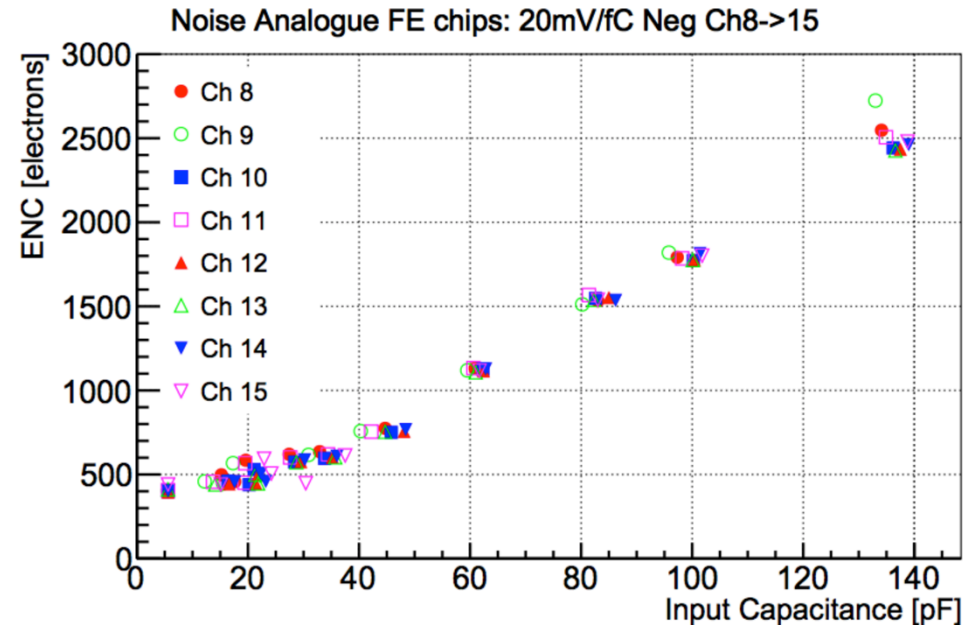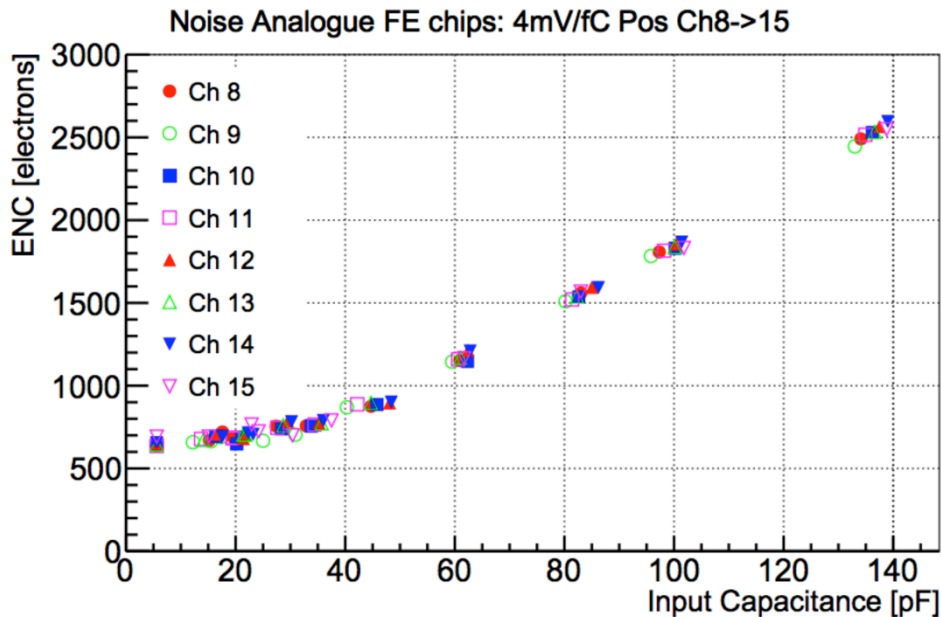
- Data does not contain ADC quantization error nor other noise sources
- Digital actvity (ADC and DSP switching, etc.) in the SAMPA has small impact in the analog frontend performance

# Digital Signal Processing (1)

- **DSP based on ALICE ALTRO**
- **Functionality:**
  - **Trigger handling with multi-event buffer and readout of pre-trigger samples**
  - **Alternatively continuous readout**
  - **Baseline correction 1 (BC1): Fixed value per channel or pattern memory subtraction**
  - **Tail cancellation filter**
  - **Baseline correction 2 (BC2): Moving average filter**
  - **Baseline correction 3 (BC3): Slope based filter**
  - **Zero suppression or Huffman compression**
  - **Cluster sum**
  - **Daisy chaining**

Digital Signal Processing (2)

- **DSP based on ALICE ALTRO**
- **Functionality:**
  - **Trigger handling with multi-event buffer and readout of pre-trigger samples**
  - **Alternatively continuous readout**
  - **Baseline correction 1 (BC1): Fixed value per channel or pattern memory subtraction**
  - **Tail cancellation filter**
  - **Baseline correction 2 (BC2): Moving average filter**
  - **Baseline correction 3 (BC3): Slope based filter**
  - **Zero suppression or Huffman compression**
  - **Cluster sum**
  - **Daisy chaining**

- **DSP can be bypassed ➔ used by TPC!**
- **DSP bypass: ADC values are continuously sent to serializers**

BC2 and BC3 principle
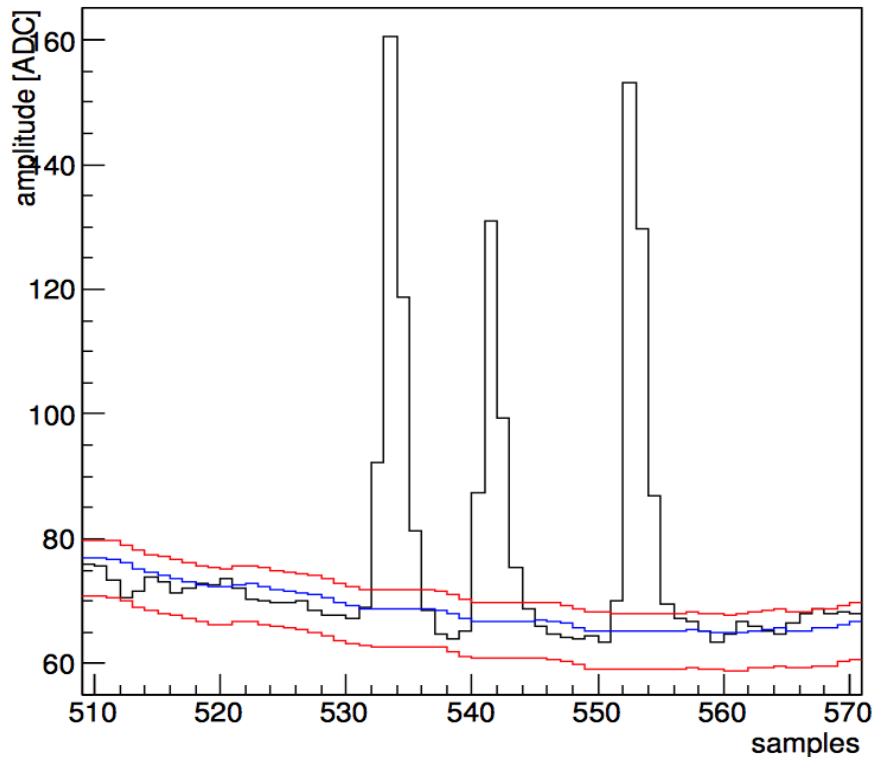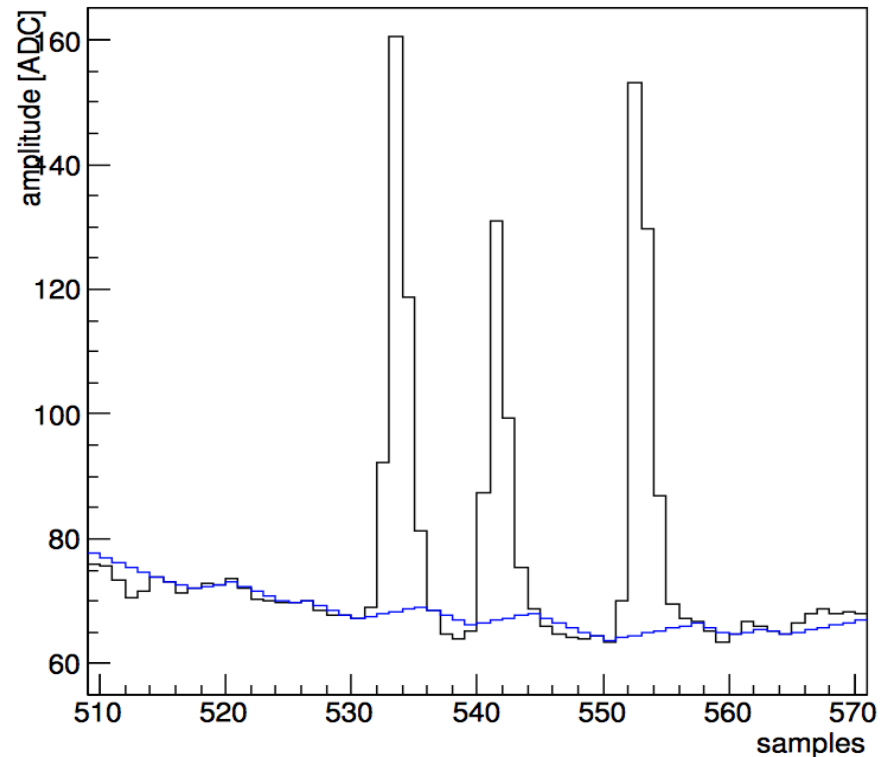
- **BC2: Moving average filter calculates average from values within settable thresholds**
- **BC3: Follows the signal limited by settable slopes**

System integration

- **Front End Card prototypes (Rev 0a) on a GEM read-out chamber**
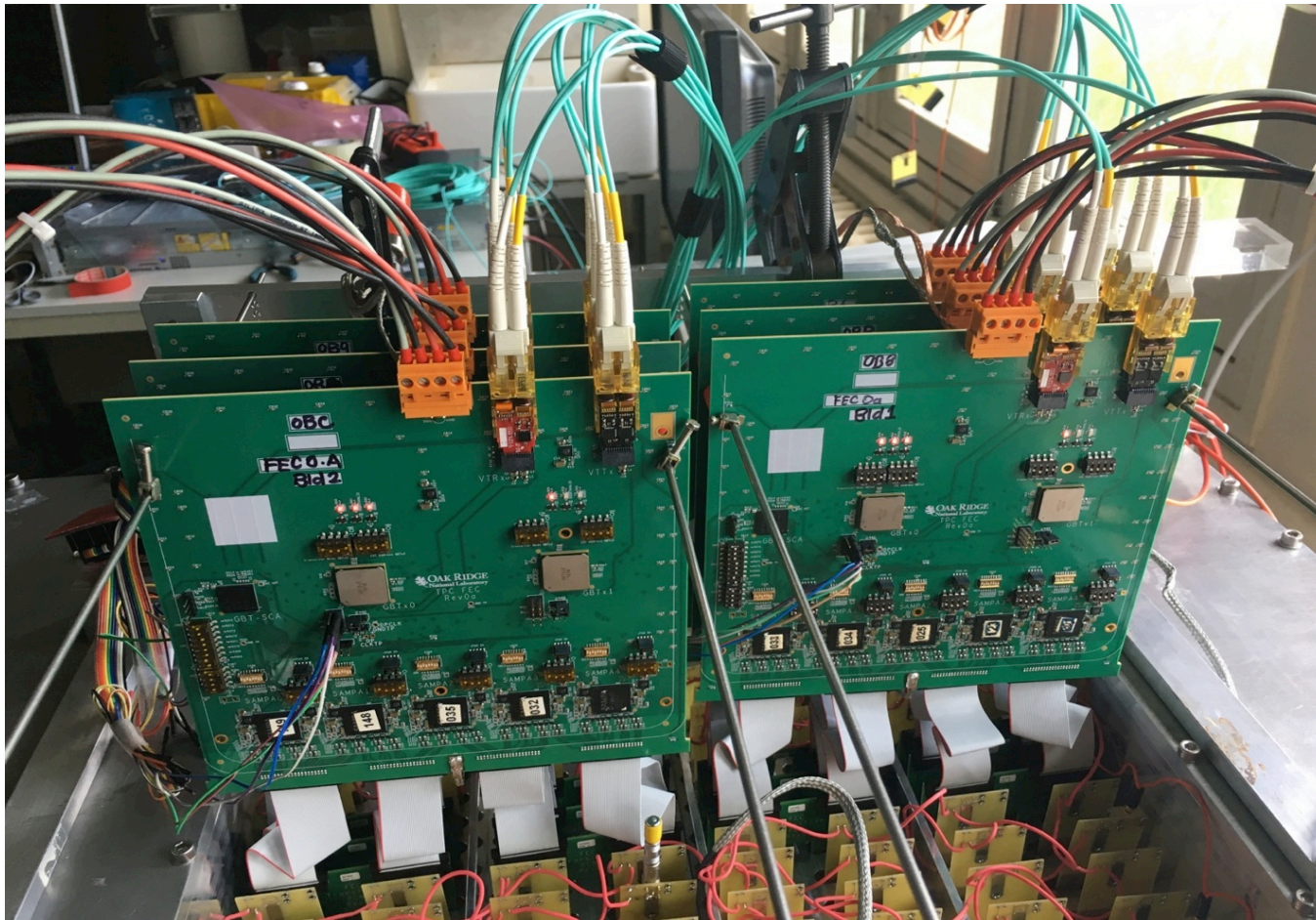
Direct readout data stream (1)

- **SAMPA data stream in direct mode is without any header**

- **How do we guarantee alignment of the data?**

- **ADC alignment can be checked as the ADC clock is transmitted as well**

- **Synchronisation (SYNC) pattern sent once at start of data taking**

- **ADC alignment and SYNC pattern have been checked in the lab with up to 6 FECs (30 SAMPAs) and no issues found**

Direct readout data stream (2)

SYNC Pattern from 5 data streams (2.5 SAMPAs)

ADC Clock

ADC Clock checking starts here.

ADC Channel 0, Time-Bin "0"

System noise

Noise distribution

Entries	160
Mean	0.9466
Std Dev	0.1003

ADC value
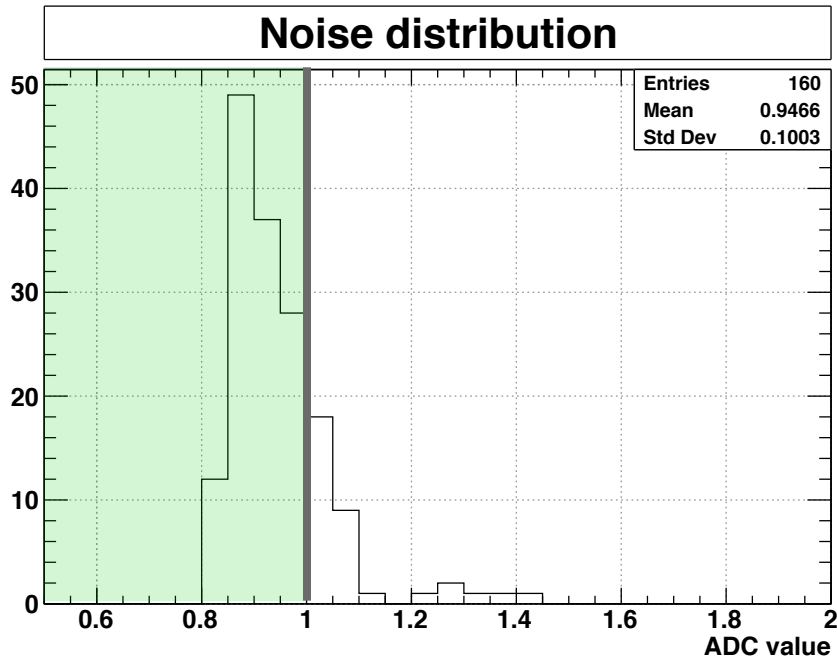
Noise histogram showing also target value of 1 LSB

ROC 0

Entries	5280
Mean x	16.18
Mean y	2.416
Std Dev x	9.729
Std Dev y	2.775

pad

pad row
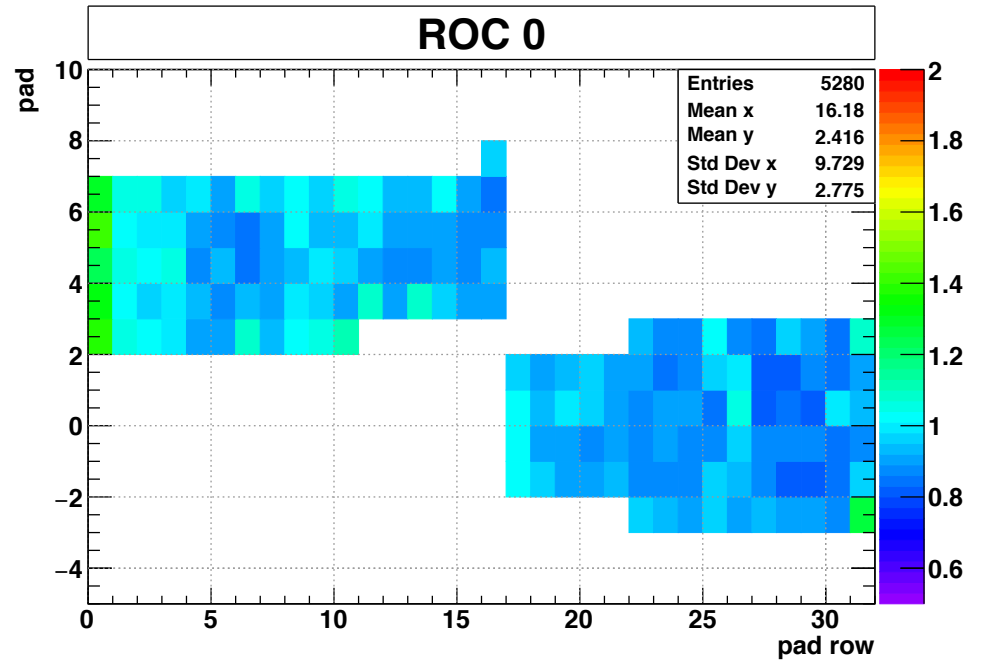
2D noise plot on detector surface

1 LSB ≈ 670 e (ENC)

Noise with HV and source (1)

- **Noise with radioactive source in center of chamber still good**
- **Load: ~ 3nA per pad, as expected in RUN3**

2D noise map on IROC with HV on

Noise with HV and source (2)
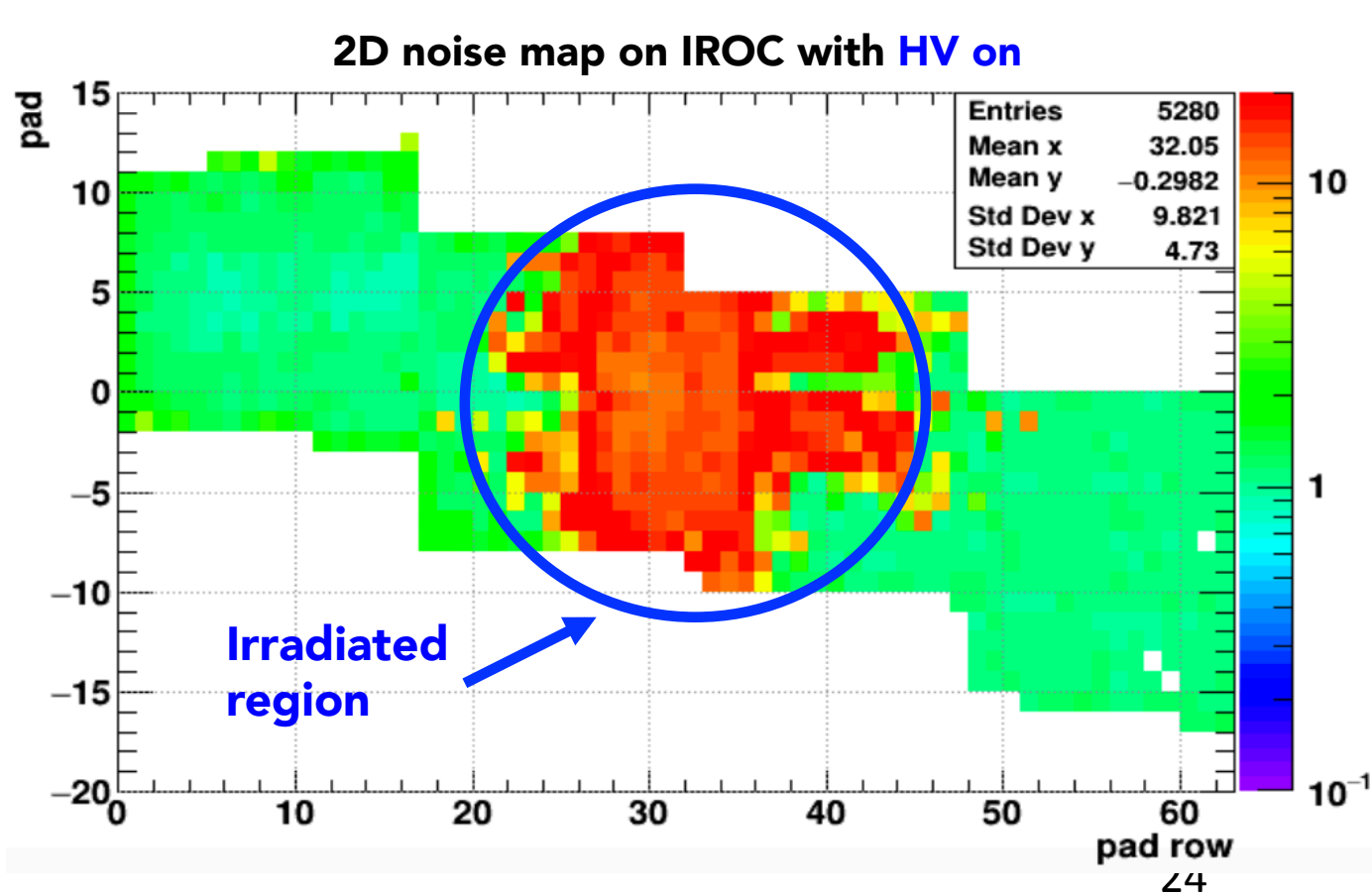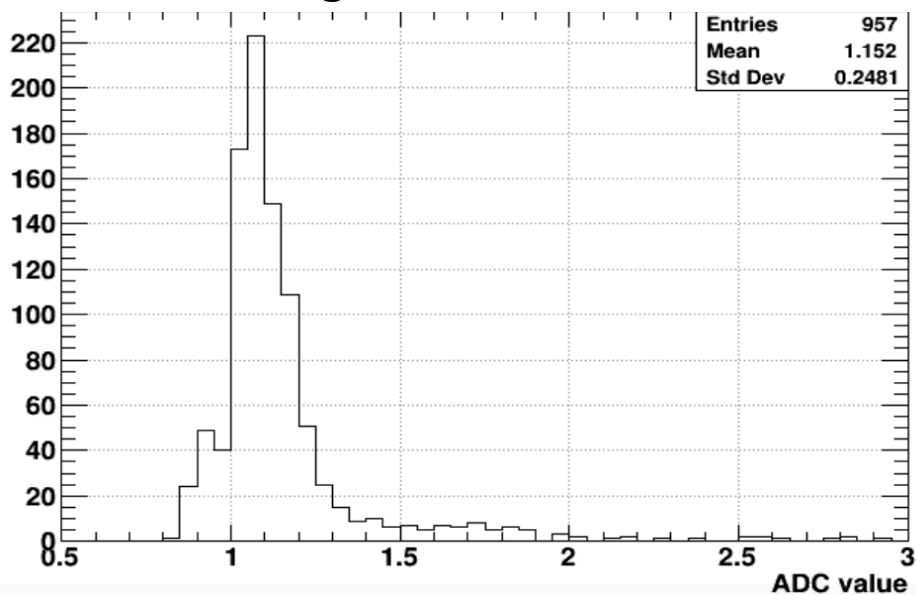
- Noise with radioactive source in center of chamber still good
- Load: ~ 3nA per pad, as expected in Run3

Noise histogram on IROC with HV on

Entries	957
Mean	1.152
Std Dev	0.2481

Noise histogram on IROC with source

Entries	957
Mean	1.235
Std Dev	0.3528
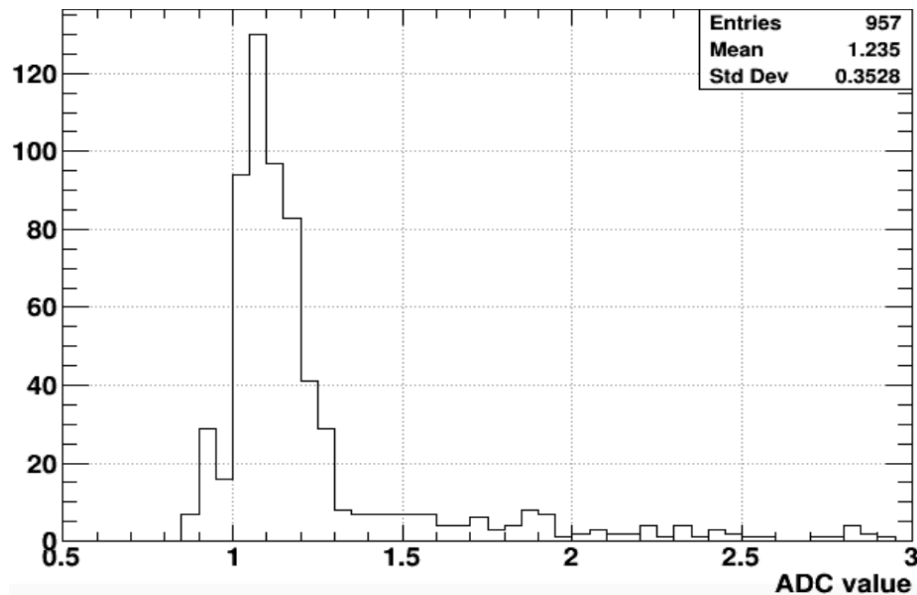
System performance

- **Beam test with one IROC at PS**
- **Example: Particle identification performance at 2 GeV/c**
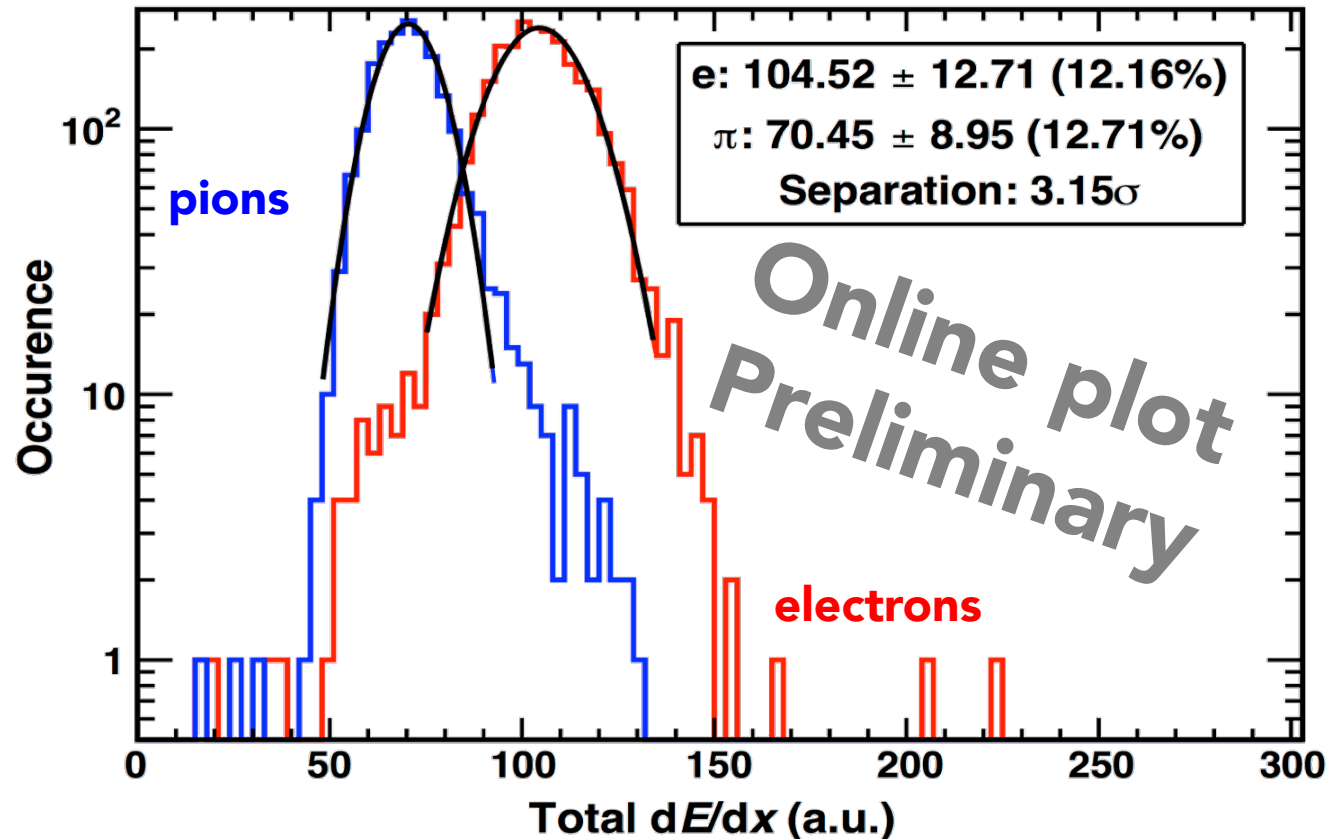
Summary and outlook

- **Major upgrade of the ALICE experiment for installation in 2019/20**

- **New TPC readout chambers based on quadruple GEM stacks**

- **New electronics for continuous readout using rad hard GBT system**

- **SAMPA ASIC with 32 channels, pre-amp, shaper, 10 bit ADC and DSP**

- **Analog and digital functionality on the same chip**

- **Very good noise, good linearity**

- **Good ADC performance**

- **Final (hopefully) SAMPA version received, under test now**

- **SAMPA and FEC mass production starts in 2018**

HV scheme

37 line HV cable: ~80m

10 kΩ

Patch box on SSW

HV module floating relative to crate

Shunt resistor for current monitoring (GEM4 top only)

HV supply and pA-meter in CR4

Chamber body

Through FEE

Pad plane

connection through end plate

Service Support Wheel (SSW)

GEM4 — segmented top side

GEM1

1 MΩ

5 MΩ

28

FEE and LV scheme

~40m

Analog voltage: + 2.25V

Pad

Analog

(1)

Digital voltage: + 3.25V

Digital

LV power
floating ground

Front-End Card

Chamber
body

connection
through
end plate

(2)

Service Support Wheel (SSW)
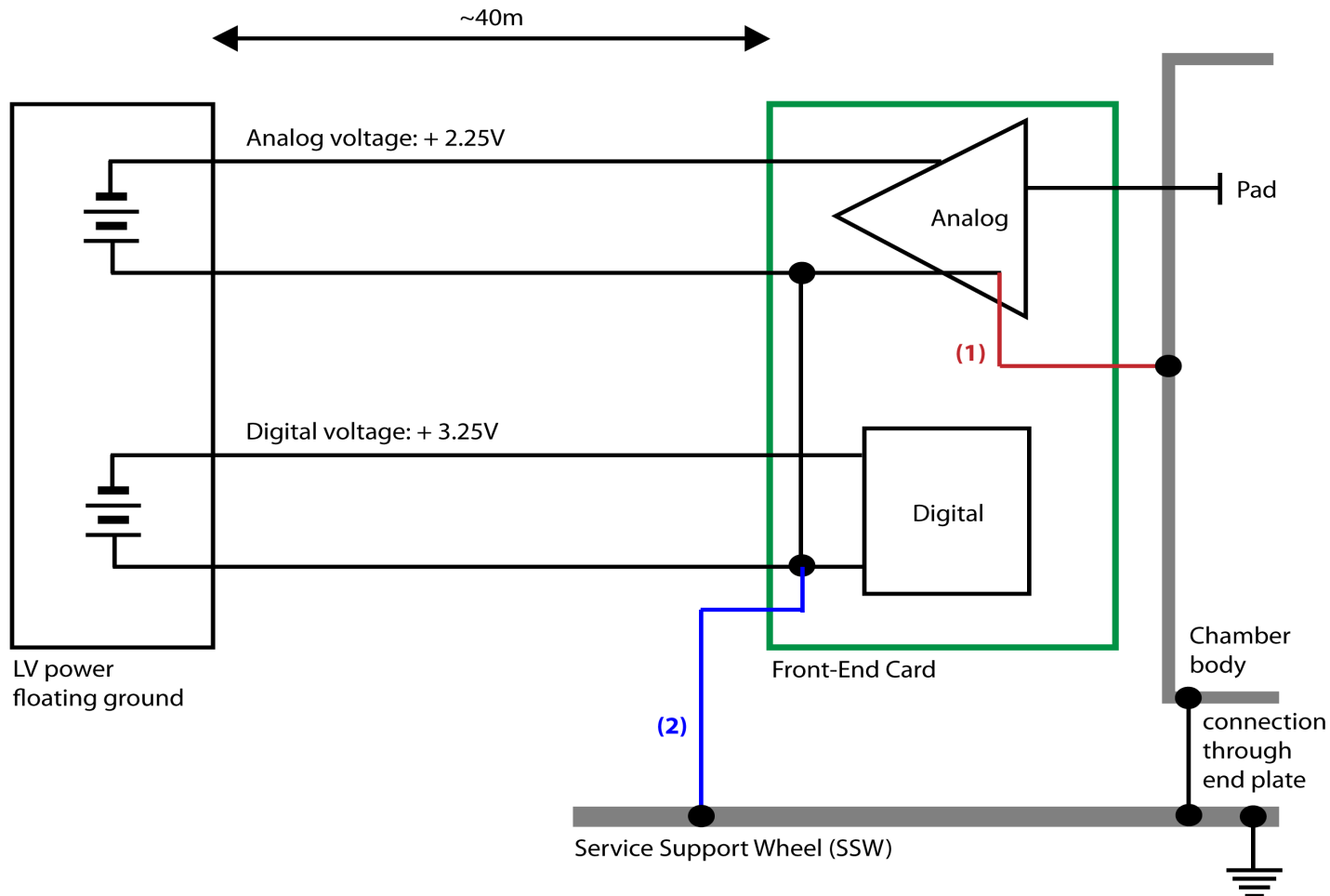
1) Low impedance ground connection from each FEC to chamber body: 1 per IROC FEC, up to 3 possible per OROC FEC
2) Low impedance ground connection from each FEC to SSW: For all FECs