RD53A
Status and Plans

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On behalf of the RD53 Collaboration

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AIDA-2020 Third Annual Meeting
24–27 April 2018 – Bologna
• **RD53**: Focused R&D program aiming at the *development of pixel chips* for ATLAS/CMS phase 2 upgrades

• The efforts of the RD53 collaboration led to the submission of the RD53A chip

• 400 x 192 pixel, 50um x 50um pixel, 20mm x 11.5mm chip

• **Goal**: demonstrate in a large format IC
  
  • suitability of *65nm technology* (including radiation tolerance)
  
  • high hit rate: 3 GHz/cm²
  
  • trigger rate: 1 MHz

  • Low threshold operation with chosen isolation strategy and power distribution

• **Not intended to be a production chip**
  
  • contains design variations for testing purposes (with 3 different versions of the analog very front-end)
RD53A - Large Scale prototype

Chip size: 20.066 x 11.538 mm²
400x192

- Submitted on 31st August 2017
- First diced chips received in Bonn 06.12.2017
- > 50 chips loaded on PCBs and under test
- Apr. 13, 2018: First bump-bonded chip test
### RD53A testing plans #1

- Two test systems:
  - BDAQ53 - Bonn University [https://gitlab.cern.ch/silab/bdaq53](https://gitlab.cern.ch/silab/bdaq53)
  - YARR - LBNL [https://gitlab.cern.ch/YARR/YARR](https://gitlab.cern.ch/YARR/YARR)  
    [https://gitlab.cern.ch/YARR/YARR-FW](https://gitlab.cern.ch/YARR/YARR-FW)

- **Debugging** of test systems (now): improvements in software, firmware, hardware
- **Functional testing** of RD53A (on-going)
- **Distribution** of setups across collaboration has started
- **Radiation campaigns** in different sites
  - Irradiation with X-rays @ CERN now on-going
  - Gammas, protons, low-dose betas, all being planned
- RD53A will be integrated into **DAQ/testbeam framework** of the experiments

RD53A chips assembled on a SCC (designed in Bonn)
RD53A testing plans #2

• Serial powering tests

• Wafer probing:
  • Bonn: developed a needle card for RD53A wafers
  • LBNL: also doing trials with their wafer prober
  • CERN: will get a copy of the Bonn needle card for CERN wafer prober
  • INFN-Torino: later

• Bump-bonding with first sensors:
  • 3 wafers under processing at IZM for bump-bonding to CMS and ATLAS sensors (April 2018)
IREF measurement and trimming

- All biases provided by internal current DACs, using an internally generated reference current IREF (4 µA nominal) derived by a Bandgap Reference circuit (independent from T, tolerant to TID)

- To compensate for process variations, we can tune IREF by means of 4-bit DAC set by hard-wired connections

- 10 chip average is 3.99 µA (expected 4 µA)
Digital scan (all FE flavours)

- Full chip responds
- Complex masking implemented
Calibration circuit (in-pixel)

- Local generation of the analog test pulse starting from 2 defined DC voltages CAL_HI and CAL_MI distributed to all pixels and a 3rd level (local GND)
- Two operation modes which allow to generate two consecutive signals of the same polarity or to inject different charges in neighboring pixels at the same time

**Injection DACs fully functional**

- Assuming 8.5fF in-pixel injection cap -> 10.08 e-/DAC
  - Close to simulation results (~11 e-/DAC)
- All biasing DACs (can be monitored using internal 12-bit ADC and are accessible on a dedicated pad) work fine
Analog scan (all FE flavours)

- Full chip responds
- High injection (30 ke-)

Occupancy ($\Sigma = 7679582$)
• **One stage CSA** with Krummenacher feedback for linear ToT charge encoding

• **Synchronous discriminator**, AC coupled to CSA, including offset compensated differential amplifier and latch

• Threshold trimming by means of autozeroing (no local trimming DAC)

• **Fast ToT counting** with latch turned into a local oscillator (100-900 MHz)

• **Improved version of the CHIPIX65 synchronous FE**
Synchronous Analog Front-end #1

- Synchronous FE fully functional and can be operated at low threshold

\[ \mu = 570 \text{ e-} \]
\[ \sigma = 75 \text{ e-} \]

\[ \mu = 77 \text{ e-} \]
\[ \sigma = 6 \text{ e-} \]
Linear Analog Front-end

- **Single amplification stage** for minimum power dissipation
- **Krummenacher feedback** to comply with the expected large increase in the detector leakage current
- High speed, low power **current comparator**
- **4 bit local DAC** for threshold tuning
- **Improved version of the CHIPiX65 asynchronous FE**
Linear Analog Front-end - Baseline/noise tuning

- Linear FE is fully functional and can be operated at low threshold
- Tuning procedure under optimization
- ENC ~ 64 e- rms
Differential Analog Front-end

- Continuous reset integrator first stage with DC-coupled pre-comparator stage
- Two-stage open loop, fully differential input comparator
- Leakage current compensation (not shown) a la FEI4
- Threshold adjusting with global 8bit DAC and two per pixel 4bit DACs
- Improved version of the FE65-P2 FE
- Test on-going
• **Bug in the A/D interface**: missing P&R constraint on the Diff. FE hit output → Varying load capacitance on comparator output → systematic variation of delay and ToT

• **This bug did not prevent the Diff FE full characterization** → Non default parameters to minimize the effect of load capacitance

• **Low threshold** achieved with 35 e- rms threshold dispersion in non-default configuration → (slower wrt nominal)
Serial Powering

• RD53A is designed to operate with **Serial Powering** → constant current to power chips/modules in series
• Based on ShuntLDO
• Dimensioned for production chip

**Three operation modes:**

- **ShuntLDO**: constant input current $I_{in} \rightarrow$ local regulated VDD
- **LDO (Shunt is OFF)**: external un-regulated voltage $\rightarrow$ local regulated VDD
- **External regulated VDD** (Shunt-LDO bypassed)
LDO: Line regulation

Internal VREF from BGR

External VREF = 0.55 V

Preliminary
ShuntLDO: Line regulation

Internal VREF from BGR

External VREF = 0.55 V

Preliminary
First results of RD53A with sensor

- 4 RD53A chips with sensor arrived in Bonn on 13 April 2018
- Image of a nut placed on the sensor backside, illuminated with Am241 source
- Hit-OR-trigger scan, LIN and DIFF FE, both set to 3 ke- threshold, un-tuned
- Need some more FW/SW development to implement auto-zero sequence for SYNC FE
Conclusions

- The **RD53A demonstrator** has been submitted in August 2017 in the framework of the RD53 Collaboration in a **65 nm CMOS technology**

- **RD53A** is alive and preliminary test results are very promising

- **Test systems** will be soon available for the institutes to test sensors with RD53A

- **First production lot** (25 wafers) bought (waiting for confirmation of delivery date)

- **RD53** design team, involving ~ 20 designers, is working to development of final pixel chips to be submitted 2019
RD53A floorplan

192 rows x 400 columns

Digital Chip Bottom (DCB)

Analog Chip Bottom (ACB)

MacroCOL Bias

70 μm

~1,500 μm

~300 μm

Digital lines

Analog lines

ADC  Calibr.  Bias DACs  CDR/PLL  POR  Bias DACs

IO frame
RD53A Pixel floorplan

- 50% Analog Front End (AFE) - 50% Digital cells

A “quad”

Digital logic

AFE

35  15

The “analog island” concept

- The pixel matrix is built up of 8x8 pixel cores → 16 analog islands (quads) embedded in a flat digital synthesized sea

- One Pixel Core contains multiple Pixel Regions and some additional arbitration and clock logic

- Pixel Regions share most of logic and trigger latency buffering

Distributed Buffering Architecture (FE65_P2 based):
- distributed TOT storage
- Integrated with Diff and Lin FE

Centralized Buffering Architecture (CHIPIX65 based (4x4)):
- centralized TOT storage
- Integrated with Synch FE
### Map of the first diced RD53A wafer

<table>
<thead>
<tr>
<th>RD53A-12C5 Wafer Map</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>RD53 Internal</strong></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th>5-1</th>
<th></th>
<th></th>
<th>6-1</th>
<th></th>
<th></th>
<th>7-2</th>
<th></th>
<th>8-2</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>2-3</td>
<td>4-2</td>
<td></td>
<td>5-2</td>
<td>6-2</td>
<td></td>
<td></td>
<td>7-2</td>
<td>8-2</td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>4-3</td>
<td>5-3</td>
<td>6-3</td>
<td>7-3</td>
<td>8-3</td>
<td>9-3</td>
<td>VDDA short</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2-4</td>
<td></td>
<td>4-4</td>
<td>5-4</td>
<td>4-4</td>
<td>6-4</td>
<td>7-4</td>
<td>8-4</td>
<td>9-4</td>
<td>good</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2-5</td>
<td></td>
<td>4-5</td>
<td>5-5</td>
<td>5-5</td>
<td>6-5</td>
<td>VDDA/VDDD short</td>
<td>7-5</td>
<td>8-5</td>
<td>good</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1-6</td>
<td></td>
<td>4-6</td>
<td>5-6</td>
<td>4-6</td>
<td>6-6</td>
<td>7-6</td>
<td>8-6</td>
<td>9-6</td>
<td>good</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1-7</td>
<td>2-7</td>
<td>4-7</td>
<td>5-7</td>
<td>6-7</td>
<td>8-7</td>
<td>unknown</td>
<td>7-7</td>
<td>9-7</td>
<td>10-7</td>
<td>power ok</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1-8</td>
<td>2-8</td>
<td>4-8</td>
<td>5-8</td>
<td>6-8</td>
<td>8-8</td>
<td>good</td>
<td>unknown</td>
<td>7-8</td>
<td>9-8</td>
<td>10-8</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2-9</td>
<td></td>
<td>3-9</td>
<td>5-9</td>
<td>6-9</td>
<td>8-9</td>
<td>VDDA short</td>
<td>7-9</td>
<td>9-9</td>
<td>good</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2-10</td>
<td>4-10</td>
<td>5-10</td>
<td>6-10</td>
<td>7-10</td>
<td>8-10</td>
<td>good</td>
<td>9-10</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3-11</td>
<td>4-11</td>
<td>5-11</td>
<td>6-11</td>
<td>7-11</td>
<td>8-11</td>
<td>VDDA short</td>
<td>7-11</td>
<td>9-10</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>4-12</td>
<td>5-12</td>
<td>6-12</td>
<td>7-12</td>
<td></td>
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- Expected yield using foundry tool: ~ 69%
RD53A Power consumption

- Direct powering
- Default bias settings
- Value mostly as expected

<table>
<thead>
<tr>
<th>Configuration</th>
<th>VDDD [mA]</th>
<th>VDDA [mA]</th>
</tr>
</thead>
<tbody>
<tr>
<td>No clock in pixel cores (at startup)</td>
<td>124</td>
<td>365</td>
</tr>
<tr>
<td>Full chip enabled</td>
<td>442</td>
<td>365</td>
</tr>
</tbody>
</table>

- On average (including Chip Bottom): 5.7 µA/pix (digital) -- 4.7 µA/pix (analog)
- In final chip less contribution from the Chip Bottom
- Further optimizations in both analog/digital pixels under investigation for final chips
RD53A main specifications

From the Spec. document

- **Hit rate**: up to 3 GHz/cm² (75 kHz pixel hit rate)
- **Detector capacitance**: < 100 fF (200 fF for the edge pixels)
- **Detector leakage**: 10 nA (20 nA for the edge pixels)
- **Trigger rate**: max 1 MHz
- **Trigger latency**: 12.5 us
- **Low threshold**: 600 e- → severe requirements on noise and dispersion
- **Min. in-time overdrive**: < 600e-
- **Noise occupancy**: < 10⁻⁶ (in a 25ns interval)
- **Hit loss @ max hit rate**: 1%
- **Radiation tolerance**: 500 Mrad @ -15° C

http://cds.cern.ch/record/2113263
Lin AFE schematic diagrams

- **Preamplifier**
  - Gain stage based on a **folded cascode** configuration (~3 uA absorbed current) with a regulated cascode load

- **Comparator**
  - Low power, **fast discriminator** (~1 uA absorbed current) including Gm stage and a transimpedance amplifier providing a low impedance path for fast switching
Sync AFE schematic diagrams

**Preamplifier**

- Telescopic cascode with current splitting and source follower
- Two switches controlling the feedback capacitance value

**Comparator**

- Offset (and mismatch) cancellation based on comparator autozero (store offset on a capacitor, and then subtract it from signal + offset)
Diff AFE schematic diagrams

Preamplifier

- Gain stage with active cascode
- Simple follower as buffer

Pre-comp

- Fully differential amp w/ resistive load
- Acts as single-to-differential converter
- Global Vth DACs generates effective differential supplies
- Local DTHn trims binary-weighted resistive load
- Sets output CM and differential OP for comp
Analog FE bias scheme

- Robust design
- Not sensitive to leakage
- “Double stage mirroring”, biasing DACs and Bandgap references already integrated/tested in CHIPIX65

Pixel array

Second stage mirroring (Macrocol bias)

Biasing DACs + first stage mirroring (ACB)
Analog bias

- **AFE area & arrangement** → 35um x 35 um aspect ratio with “analog island” arrangement
- Same bump PAD structure
- Common strategy for power, bias distribution & shielding

- **M6 V lines** for the analog bias
- **M5/M7 shield** for bias lines in the digital section of the pixel
- **AP/M9/M8 V supplies**
Pixel array logic organization

- Each Pixel Core receives all input signal from the previous core (closer to the Digital Chip Bottom)

- Regenerates the signals for the next core.

- The timing critical clock and calibration injection signals are internally delayed to have a uniform timing (within 1-2 ns)
Linear Analog Front-end - Injection-based tuning

- Linear FE fully functional
- 56 e rms threshold dispersion after tuning @ relatively high th