Update on 65nm developments in Bonn

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Outline

• Contributions to RD53 pixel chip developments (“RD53B”)
  – Digital integration & Verification
  – IO pad frame
  – CDR / PLL
  – Serializer & Gbit cable driver

• Pixel sensor capacitance measuring chip (PixCap65)
  – Pixel chip to be bumb bonded to a sensor
  – Measurement of the total and pixel-to-pixel capacitance
RD53 Pixel Chip for
ATLAS/CMS HL-LHC Upgrade
Towards ATLAS/CMS HL-LHC Pixel Chips

ChiPix and FE65_P2
64 x64 px prototypes
MPW run

RD53A
400 x 192 px. demonstrator
shared engineering run

“RD53B”
400 x 392 px.
production run

2016 2017/18 2018/19

AIDA-2020 Third Annual Meeting, 24-27 April 2018, H. Krüger
Contributions to RD53 Function Block Development

• Clock data recovery (CDR) and PLL
  – Command and clock information encoded on one differential line (@160Mbps)
  – CDR extracts command and clock information
  – PLL stabilizes the 160 MHz clock and generates
    • BCO_CLK = 40 MHz (adjustable phase)
    • SER_CLK = 1.28 GHz

• Serializer (SER)
  – Runs at 1.28Gbps
  – Generates the Gbit output stream for the hit data

• Gbit link cable driver (four lanes @ 1.28 Gbit)
  – Transmits the hit data on a low mass cable
  – Driver uses pre-emphasis to compensate cable loss

• Pad frame
  – Integration of IO blocks (driver/receiver) and voltage regulators (Shunt-LDO)
RD53 PLL/CDR/SER Function blocks

- RD53 command/data interface
  - One up-link, combining CLK and CMD \(\rightarrow\) needs clock/data recovery (CDR)
  - Four high speed (1.28Gbps) down-links \(\rightarrow\) serializer (SER) and Gbit driver (TX)
PLL / CDR

- Recover command data and clock (160 MHz) from incoming data stream
- Provide high speed clock to the serializer
Serializer

- Load 20 bit word data at 64 MHz
- Serialize data at 1.28 GHz
Cable Driver

- Current mode output stage (CML)
- Configurable pre-emphasis (3 tap FIR)
- Four 1.28 Gbit lanes per chip
Example Measurement

- CMD: 160Mbps PRBS5 from signal generator
- Measured signal: SER_OUT (data)
- RD53A state:
  - CDR supply: external
  - Default bias & configuration
  - All columns off
  - No CLK on matrix
- Jitter:
  - Peak-peak: 134 ps
  - RMS: 18 ps
RD53: Conclusion & Outlook

• RD53A works and is currently being tested
  – Characterization of PLL/CDR
  – Digital functionality
  – Powering configuration

• “RD53B” design:
  – Improvements for PLL/CDR
  – Digital design flow (continuous integration)

• Submission planning
  – PLL/CDR test chip: August 2018
  – Full size “RD53B”: Q1(2) 2019
PixCap65 Chip for Measurement of the Pixel Sensor Capacitance
Pixel Sensor Capacitance

• Pixel capacitance $C_d$ is an important parameter for the analog front-end design
  – Noise
    \[
    ENC_{\text{thermal}} \propto \sqrt{\frac{1}{g_m \cdot \tau_{\text{shaping}}} \cdot (C_d + C_f)}
    \]
  – Signal rise time (time walk)
    \[
    \tau_r = C_d \cdot \frac{C_o}{g_m} \cdot \frac{1}{C_f}
    \]
  – Charge collection efficiency
    \[
    CCE = \frac{C_f \cdot A_0}{C_d + C_f \cdot A_0}
    \]
  – Cross-talk

• Contributions to the total pixel capacitance come from
  – Inter-pixel capacitance (pixel-to-pixel and pixel to p-stop) → dominating
  – Implant to backplane
  – Implant to FE chip
  – Bump capacitance
Capacitance Measurement Method

• Charge based capacitance measurement
  – Phase 1: Charge Cd with potential U via SW1
  – Phase 2: Discharge C_D via SW0
  – Measure average current <I_U>

• Measurement principle originally proposed for precise measurement of on-chip parasitic capacitances (B. McGaughy, A Simple Method for On-Chip, Sub-Femto Farad Interconnect Capacitance Measurement, IEEE Electronic Device Letters, VOL. 18, NO. 1, Jan 1997)
PixCap65 Predecessor

- PixCap implementation for FE-I4 pixel sensors (2012)
  - PixCap (LF 150nm)
  - Connects to 40 x 8 pixels with 50µm x 250µm bump pitch
  - Individual measurement circuits for every pixel

From: M. Havránek et al., Measurement of pixel sensor capacitances with sub-femtofarad precision, NIM A 714 (2013) 83-89
PixCap65 Chip

- Submitted together with RD53A
- 40 x 40 pixel matrix, 50µm pitch
- Total- and pixel-to-pixel capacitance measurement
- Extra pixel row w/o bumps for test & calibration capacitors
- Column-wise enable for reduction of switch leakage
Pixel Cell Block Diagram

- Individual programmable clock and voltage routing per pixel:
  - Four switches per pixel: two PMOS plus two NMOS
  - Four global clock nets: CLK0, CLK1, CLK2, CLK3
  - Three global voltage lines: VM1, VM2, VM3 (VM0 = GND)

- Pixel configuration shift register
  - Enable clock lines CLK_EN[3:0]
  - Static bias SEL[1:0]

SEL[1:0] Static bias
0 0  GND
0 1  VM1
1 0  VM2
1 1  VM3

CLK_EN[3:0] Function
0 0 0 0  No clock enabled, static bias active
x x x 1  CLK0 enabled (NMOS to GND), static bias off
x x 1 x  CLK1 enabled (NMOS to VM1), static bias off
x 1 x x  CLK2 enabled (PMOS to VM2), static bias off
1 x x x  CLK3 enabled (PMOS to VM3), static bias off
Measurement Example

- Dummy pixel with connection to a internal test capacitor ($C_{\text{INJ}}$, single RD53A injection capacitor)
- Design value: 8.533 fF (w/o parasitic extraction)
- Measured value: 8.318 fF

\[ C = \frac{slope}{\Delta V} \]
Bare Chip Pixel Capacitance

- Bump pad + parasitic capacitance of the pixel switches: ~11.77 fF

Top pixel row has systematic capacitance dispersion due to non regular dummy metal filling pattern at the top edge of the matrix.
PixCap65: Conclusion & Outlook

- Pixel capacitance measurement for 50µm bump pitch pixel sensors
- Can be bump bonded to any sensor size (i.e. no special sensor size needed)
- Precise (sub fF) measurement of total and pixel-to-pixel capacitance
- Wafer scale bump bond deposition is done (@ IZM, on RD53A wafer)
- Waiting for FC to various sensors