

14.4. Readout systems for innovative calorimeters

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WP 14.4

April 25th, 2018

- **Milestone 58:** Definition of optical and electrical coupling of readout, interface functionality and DIF design
- **Deliverable 14.5:** Common running of calorimeter prototypes
- **Deliverable 14.6:** Adaptation of readout system for operation in compact LC detectors



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Milestone 58: Definition of optical and electrical coupling of readout, interface functionality and DIF design

Verification: DIF data sheets

Date: Months 24, delivered

MS58	Definition of optical and electrical coupling of readout, interface functionality and DIF design	14	M24	13/04/2017	Achieved	Report (http://cds.cern.ch/record/2259907)
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describes status for AHCAL DIF (produced), SDHCAL DIF (in design) and SiECAL DIF (aim for 2018)

Test bench for ASIC tests (no deliverable/milestone)

Description of subtask 14.4.2: “This activity includes test benches for front-end ASICs of highly granular calorimeters as e.g. those developed in WP4. The test bench is a prototype for mass tests for LC Experiments capable to serve experiments with similar front-end electronics.”

Status: testboard for AHCAL ASIC (SPIROC2E) in BGA package built, **has been used for the “mass testing” for the ASICs for the next large prototype (~600 ASICs)**

Deliverable 14.5: Common running of calorimeter prototypes

Deliverable: Data acquisition system to allow for a common data taking of different highly granular calorimeter prototypes in beam tests at CERN and DESY. These tests should provide data files containing events synchronised between the subsystems.

Date: Month 36

Status:

- **within WP5: EUDAQ2.0 released in June 2017**
- **in July 2017: combined testbeam of CMS HGICAL and CALICE AHCAL prototypes**
- **in September and October 2017: several more short periods of combined HGICAL + AHCAL running**
 - **extended HGICAL setup**
 - **consolidated DAQ (mainly the HGICAL part)**

HGCAL + AHCAL data taking in October 2017

- 5 days in H6 at SPS: 18 – 23 October 2017 (originally foreseen for CMS tracker)
- fixed installation without stage -> no position scan possible
- data taken:
 - muons @ 120 GeV
 - pions: 50 – 120 GeV
 - electrons: 20 – 80 GeV
- HGCAL hardware:
 - 20 modules (was 10 in July)
 - one layer in FH with 7 modules
 - observed strong dependence of noise on the way how modules are grounded triggered further investigations
- AHCAL hardware
 - as in July
 - working reliably
- synchronisation:
 - after a fix to the SYNC board firmware: same number of triggers seen in all detectors
 - routine common running



on

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Figure 5.12: Seven 6" silicon sensor modules, equipped with SKIROC2-CMS ASIC, mounted on a copper support/cooling plane during the 2017 beamtest campaign.

Experience from common HGICAL + AHCAL running

- **quick integration of two calorimeters with very different trigger concepts**
 - **only possible thanks to EUDAQ**
 - **inclusion of wire chambers also straight forward**
 - **use of HGICAL SYNC board (instead of TLU) possible because of clear definition of standards for master clock and control device**
- **data taken in this testbeams provided important input for HGICAL TDR (handed in in December 2017)**
- **more testbeam with a (nearly) fully equipped HGICAL prototype + AHCAL prototype planned for 2018**
- **overall a big success!**
 - **shows the strength of having a (relatively) simple versatile high-level DAQ system**

Deliverable 14.5: Common running of calorimeter prototypes

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Date: Month 36

Status:

- **within WP5: EUDAQ2.0 released in June 2017**
- **in July 2017: combined testbeam of CMS HGCALE and CALICE AHCAL prototypes**
- **in September and October 2017: several more short periods of combined HGCALE + AHCAL running**
- **plans for 2018:**
 - **2 week of CMS HGCALE + CALICE AHCAL testbeam at SPS in October 2018**
 - **2 weeks of CALICE SiECAL + CALICE SDHCAL testbeam at SPS in September/October 2018, plan to use EUDAQ**
 - **SDHCAL has already tested previous EUDAQ version, feedback taken into account for EUDAQ2.0**
 - **SiECAL plans to test EUDAQ once new hardware fully under control**
- **overall: requirements of Deliverable 14.5 fulfilled, first draft of writeup exists**

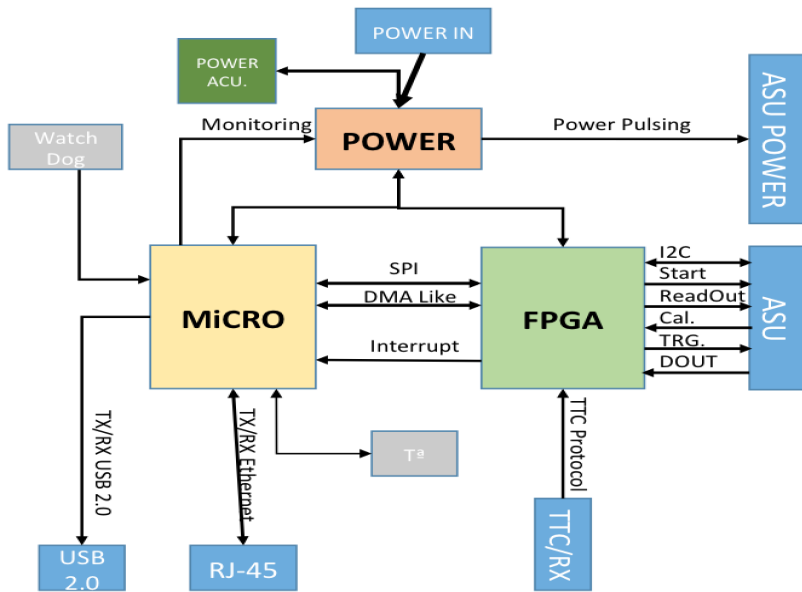
Deliverable 14.6: Adaptation of readout system for operation in compact LC detectors

Date: Month 44

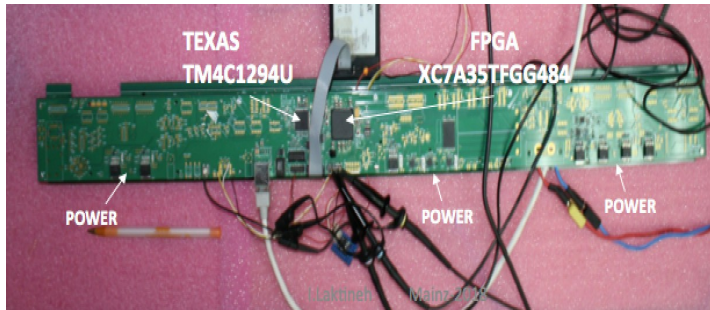
Status:

- **SiECAL DIF:** see talk by Dominique Breton (Dirk filling in)
- **SDHCAL DIF:** new version to operate a whole detector plane with 1 DIF only developed by CIEMAT
- **AHCAL DIF:**
 - space constraints less stringent than for ECAL
 - current generation of interfaces already designed with limited space in mind
 - no further optimisation planned at the moment

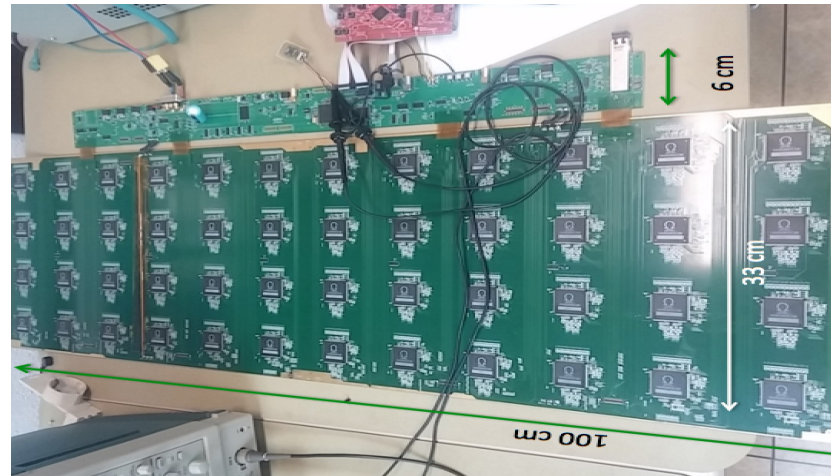
DIF sends DAQ commands (config, clock, trigger) to front-end and transfer their signal data to DAQ. It controls also the ASIC power pulsing



- Only **one DIF per plane** (instead of **three**)
- DIF handle up to **432 HR3 chips** (vs **48 HR2** in previous DIF)
- HR3 **slow control** through **I2C bus (12 IC2 buses)**. Keeps also **2 of the old slow control buses as backup & redundancy**.
- **Data transmission to/from DAQ** by **Ethernet**
- **Clock and synchronization** by **TTC** (already used in LHC)
- **93W Peak power supply** with super-capacitors (vs **8.6 W** in previous DIF)
- Spare I/O connectors to the FPGA (i.e. for GBT links)
- Upgrade **USB 1.1** to **USB 2.0**



The firmware is being developed. DIF to be tested with large ASU equipped with HR3.



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Summary

- **Milestone 58: Definition of optical and electrical coupling of readout, interface functionality and DIF design**
Date: Months 24
status: milestone report delivered
- **Deliverable 14.5: Common running of calorimeter prototypes**
Date: Months 36
status: task fulfilled, first draft of writeup exists
- **Deliverable 14.6: Adaptation of readout system for operation in compact LC detectors**
- **Date: Months 44**
- **status: on track**