Silicium-Tungsten ECal Development at LAL: Control and Readout Electronics

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Introduction

- Latest developments proposed by LAL group for a Silicon-Tungsten electromagnetic Calorimeter in ILD.


- AIDA2020 WP14 Deliverable 14.6: Adaptation of readout system for operation in compact LC detectors
  
  1. Power Pulsing: Proposal to use new ultra-flat capacitors on all ASUs of the Slab (order 10 ASUs per slab).

Ecal Constraints

The Challenge: a very Compact Detector!

Constraints:

- Spatial constraints:
  - limited space between layers
  - Limited space at the end of a slab
  - Control & Readout electronics at the extremity of the Slab
  - Signal Integrity over the Slab

- Low power consumption: power pulsing

- Thermal uniformity

- Mechanical Assembly process
Ecal Electronics
Space Constraints

Space constraints for the Active Sensor Units (ASUs):
- Maximum Height for Electronics (including PCB): depends on number of layers (20-30)
  - For final design: x.x mm?
  - For prototype: (PCB + components for the SKIROC-2 BGA option): ~ 3mm

Current ASU Electronic board design:
- PCB thickness (FEV 12): 1.6 mm
- SKIROC BGA height: 1.4 mm
  Total: 3 mm

Space constraints for the Slab Interface Board (SL-Board):
- L-shape (even and odd ASUs) Dimensions: see below.
- Maximum Height: ~ 12 mm
Power-Pulsing: New ultra-flat Capacitors

Proposal: new ultra-flat capacitors on all ASUs for the AVDD decoupling resulting in:

- Peak current reduction: especially through the connectors
- No voltage drop along the slab
- Homogeneous peak power dissipation during power pulsing.

- 400 mF capacitor/ 15A (peak Current) at the end of the SLAB to 140 mF / 1.5 A per ASU.

Reminder of power consumption values:
- DVVD (3.3V) 11 mA/chip, total 180 mA/ASU
- AVDD (3.3V) / Chip: 90 mA/chip during ACQ, 20 mA during Conversion, 0.01 mA idle measured in house and compared with measurements by Stephane Callier (Omega)

- Distributing the capacitors along the slab permits reducing current between ASUs by a factor ~50-100.
- The current peak is local.
- The current delivered for charge reloading of the capacitors will be actively limited at the extremity of the Slab.
Ultra-Thin Supercapacitor
DMH series
DMHA14R5V353M4ATA0
35 mF / 4.5 V

Life time has to be checked, depends on voltage and temperature...

Integrated capacitors permit the peak current of ~1.5A to be local during power pulsing => recharge is limited to a total of ~150mA...
Control & Readout Electronics

The new developments for the control and readout electronics to satisfy D14.4 (space constraints of an LC Detector):

- **SL-Board**: Digital interface board situated at the extremity of the Slab, based on a MAX10 FPGA, which handles:
  - Control & readout of the chained ASUs (SKIROC interface)
  - Interface to the CORE acquisition module through a kapton cable (rigid+flexible) in order to have flexibility for the connection inside the detector (45° angle)
  - Local 40MHz oscillator and remote USB interface for standalone control of the Slab (permits independent testing of Slab interface and kapton communications).

- **CORE-Module**: Control & Readout module that handles a column of Slabs, for the prototype phase.

**CORE Module** : Control & Readout Module

**SL-Board**

Even ASU
Odd ASU

SL-BOARD

SLAB extremity

Hirose FX18-100 pin, 0.8 pitch

Kapton cable Rigid+Flexible

USB

Gbit UDP

Optical link

HDMI from CCC
Core Module connector:
7 common differential pairs for sensitive signals, 30 individual pairs for control and readout, 14 common lines, GND

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<td>Clk</td>
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Signals

| Rx_i  |
| Tx_i  |
| ADD[0]|
| ADD[1]|
| ADD[2]|
| ADD[3]|
| Spare ...
| GND ...

Full design of ILD compatible electronic services started that includes parts described above
The Acquisition Module

The Control & Readout Acquisition system will be based on an existing mother board that handles:

- Control & Readout through USB/Ethernet/Optical fiber
- Distribution of the clock and fast commands

- There are existing low level C-libraries. (LAL-ML protocol)
- This LAL development is already used for other experiments.
- The Detector specific CORE Daughter board is under development as well as its Kapton cable.

Ex of a Long Slab: 8 ASUs

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**Diagram Details:**

- **HV**
- **SL-BRD**
- **ASU/WAFER**
- **Gradconn Interconnexion**
- **HDMI for current CCC interface**
- **Existing CORE MOTHER**
- **Little adapter board**

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**Legend:**

- ASU/WAFER: Active Silicon Units/Wafers
- Gradconn: Gradational Connection
- HDMI: High Definition Multimedia Interface
Global Architecture Scheme

Overall design
- .... compatible with ILD constraints
  - Little space consumption for connection between slabs and CORE Modules
  - CORE Mother can be placed at the forefront of barrel, Daughter between Ecal and Hcal
- ... assures compatibility with other AIDA2020 developments
  => Paves way for combined beam tests (other calos, trackers etc.)
- Expect first version of system to be in place for summer 2018
- SL-Board is delivery for AIDA2020 and P2IO/HIGHTEC

CCC: Clk and Control Card
CORE Module/Mother/Daughter : Control and Readout
SL-BRD : Interface board to Slab

Control PC
- Gbit UDP/USB/Optical Fibre
- HDMI 1-5m
- Clk, Fast Commands

ZedBoard
- Serial Link To PC (RS232) (optional)
- Beam Control

Control & Readout Kapton

ASU/WAFER

~ 2 x 15 slabs

HV Kapton

Data : 40 /80 Mbits/s
Status of development: 
SL_board

Design is well advanced:
• Board schematics is final
  • Main constraints: low power but good signal integrity
  • Based on Altera MAX10 mixed CPLD/FPGA low power technology
  • High versatility for test and debugging
• PCB design:
  • Placement is difficult due to reduced space but well on track
  • Routing is already partially done
Status of development: CORE_kapton

Core Module connector (100 pins):
7 common differential pairs for sensitive signals, 30 individual pairs for control and readout, 14 common lines, GND

SL_board connectors (40 pins):
7 common differential pairs for sensitive signals, 1 individual pair for control and readout, 14 common lines, GND
Status of development: CORE_daughter

- **CORE_daughter**
- **Kapton interface** (100 pins)
- **Motherboard interface** (100 pins)
- **Cyclone IV FPGA**
- **Kapton buffers and transceivers**

- ~12 cm
- ~6 cm
Conclusion

- LAL group has been reinforced for the electronics developments since last summer.

- Proposal to use new ultra-flat capacitors on each ASU to
  - Reduce the peak current going through the connectors
  - To avoid voltage drop problems along the slab during the Power-pulsing
  - Lifetime of new capacitors to be verified

- Development of a new Control and Readout digital interface that fits the space requirements for the final design: SL-Board + Kapton cable.

- The acquisition module will be based on an existing CORE-Mother and a dedicated core daughter which is under development.

- Goal: to have a set of all the new boards by this summer.

- Deliverable D14.6 is on track