OVERMOS
CMOS HR detector for HEP applications

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Overview

• OVERMOS1 description
• First test results of irradiated / non–irradiated OVERMOS1
• TCAD simulations
• Conclusions and next steps
OVERMOS is a CMOS MAPS project demonstrator. Its main purpose is to investigate and understand radiation effects in HR CMOS structures, with a view to developing reliable TCAD models. It is fabricated using:

- TowerJazz 180 nm Hi-res 18 um thick epitaxial layer 1kOhm – cm
- CMOS DPW - originally proposed for DECAL of ILC to increase CCE by housing RO in PW -
- ‘Small’ n-collecting nodes
- Multi diode arrangements within pixel
OVERMOS description

- The PASSIVE pixels feature different arrangements of the collecting 4 x 4 um2 nodes.
- The ACTIVE pixels, i.e. with in-pixel electronics, allow analogue readout of the pixels.
All the pixels in the OVERMOS1 include a p++ region around each diode to reduce cross talk from neighbouring ones.

The OVERMOS1 ASIC ‘basic passive’ has been tested before and after n-irradiation for DC. Laser induced charge collection studies in progress.
OVERMOS n-irradiation

- OVERMOS devices have been irradiated at Ljubljana in October 2017 to 1E13, 5E13,1E14 and 5E14 n fluence
- Estimated around 30% of fluence consisting of high energy neutrons (> 100keV)
OVERMOS DC tests

Changes in Ilk and BV characteristics vs. fluence
Average of 10 pixels + \( \sigma \)

T = 21 \( ^\circ \)C

\( \Phi = 0 \)
\( \Phi = 1 \times 10^{13} \)
\( \Phi = 5 \times 10^{13} \)
OVERMOS DC tests

Changes in Ilk and BV characteristics vs. fluence
TCAD simulations

- .gds layout of single passive pixel 40 x 40 um2

- 3D TCAD simulations are being performed to investigate accuracy of modelling capabilities
- Individual doping profiles for OVERMOS were obtained using SPROCESS, to simulate a (simplified) CMOS fabrication by TJ foundry
• Inclusion of surface charge effects at Si/SiO2 boundaries, B segregation in SiO2, crystal orientation (<100>) and interface stresses
• Final mesh 273868 points, 10 non-Delaunay elements around the SiO2/Si interface
**TCAD simulations**

- Result is a 3D pixel mesh with realistic doping profiles

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**Epi-Bulk**

- **NW**
- **PW**

**SIMS profiles**

**B-segregation effect**

**SiO2**

- **epi**

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**AIDA 2020 – Bologna, Italy, 24 - 27 April 2018**
TCAD simulations

SiO2/Si trap density 1-2e11

SRV=1e4

Vbias

GND

Depletion region vs. Vbias

TCAD DC results:

• Depletion region
• Internal electric field
• Impact ionization

SiO2

M1

BSG

AIDA 2020– Bologna, Italy, 24 - 27 April 2018
TCAD simulations

- TCAD DC results:
- At around 50 V bias the strength of $F_z$ is close to ‘typical’ $F_{max}$
TCAD & Test results
Leakage currents & BV

\[ \langle I_{lk} \rangle + \sigma \ 10 \ pixels \]

\[ I_{lk} \ \text{TCAD} \ 0 \ \text{OxQ} \]
\[ I_{lk} \ \text{TCAD} \ 1.7e11 \ \text{OxQ} \]
\[ I_{lk} \ \text{TCAD} \ 2e11 \ \text{OxQ} \]

\( I_{lk} \) taken with CS4200, \( I_{\text{compl}} = 1E-7 \)
TCAD simulations with quench resistor 1E6

II model: UniBo + interpolation of avalanche driving forces

\[
\alpha(F_{ava}, T) = \frac{F_{ava}}{a(T) + b(T) \exp \left[ \frac{d(T)}{F_{ava} + c(T)} \right]}
\]

\[
F_{ava,n} = \frac{n}{n+n_0} \left( F \cdot J_n - F_{ava} \right) + \frac{n_0}{n+n_0} |F|
\]
Conclusions and next steps

- OVERMOS device has been designed to investigate and understand radiation effects in HR CMOS structure
- A number of devices have been n-irradiated up to 5E14 fluence and are being characterised for DC and charge collection
- 3D TCAD simulations, relying on SPROCESS, to simulate CMOS process fabrication, have been implemented
- DC simulations up to BV match very well test results for non irradiated structures
- We are going to investigate implementation of various radiation damage models in TCAD to verify their accuracy
- From changes in $I_{lk}$ and BV characteristics we are trying to infer changes in $N_{eff}$ and compare them with those obtained by other means (i.e. TCT)
- Charge collection test using IR laser to compare with TCAD simulations
Backup
OVERMOS Active Pixel

charge amplifier

shaper
Backup

OVERMOS Laser Test

OVERMOS in metal box to reduce EMP noise

OVERMOS Under Laser 100x optics