

Status of the 3DIC project

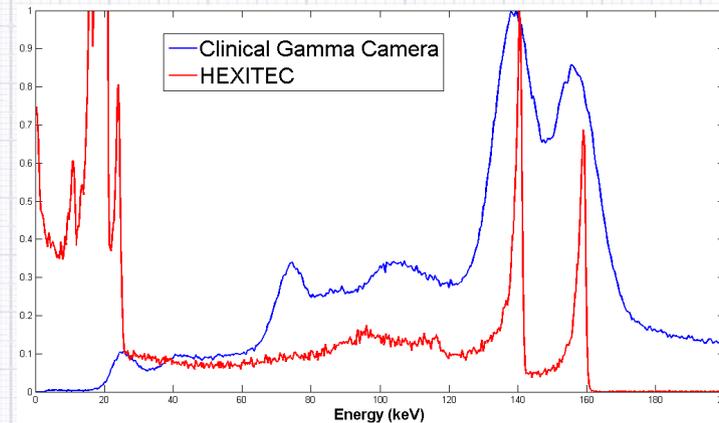
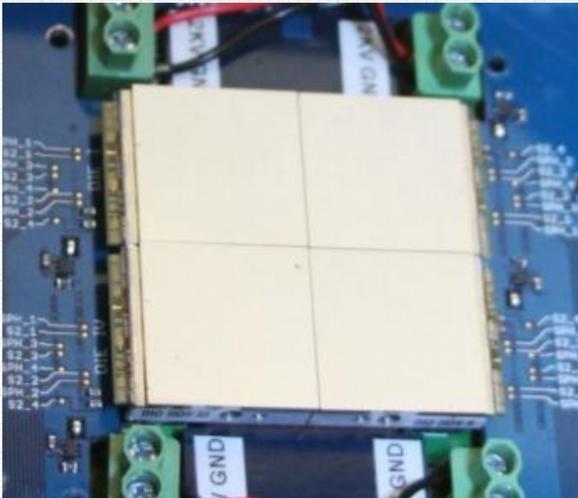
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Patrick Sieberer - student

P. Seller - STFC(RAL)

Background

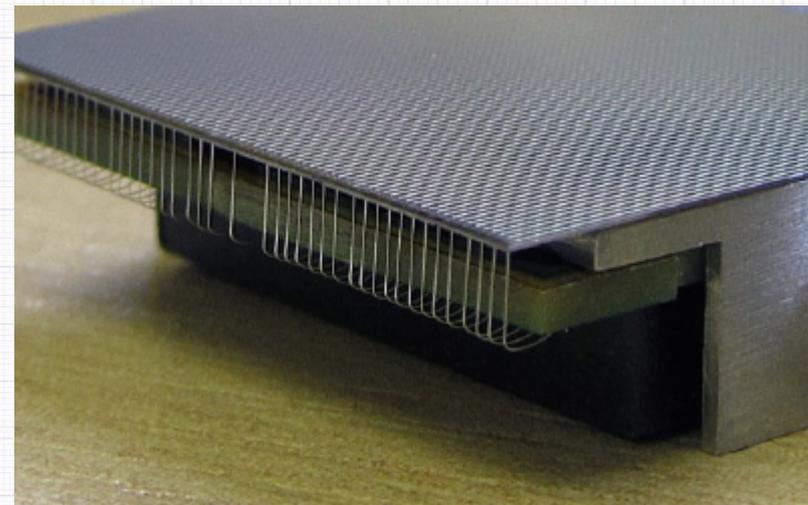
- Demonstrate that 2-tier 3D pixeldetector readout ASIC with vias in every pixels can be done “via last”
 - Analogue tier based on proven Hexitec platform



- Digital tier contains a 12bit (10bit) digitizer in every pixel and readout.

Hexitec 4S

- The STFC group (no Uppsala participation) did develop a 4-sided buttable version of Hextic with I/O made minimal and redistributed to the rear face of the ASIC
- ASIC thinned down to 120 μm
- TSV 70 μm DRIE cut with redeposited SiO_2 through the 120um thick silicon. The metal via is mostly copper connecting to the Al pad. Process done by T-Micron (JP)
- Generally successful demonstration of via-last process.
- Problems encounter are high contact resistance in I/O pad and non flat ASICs after thinning

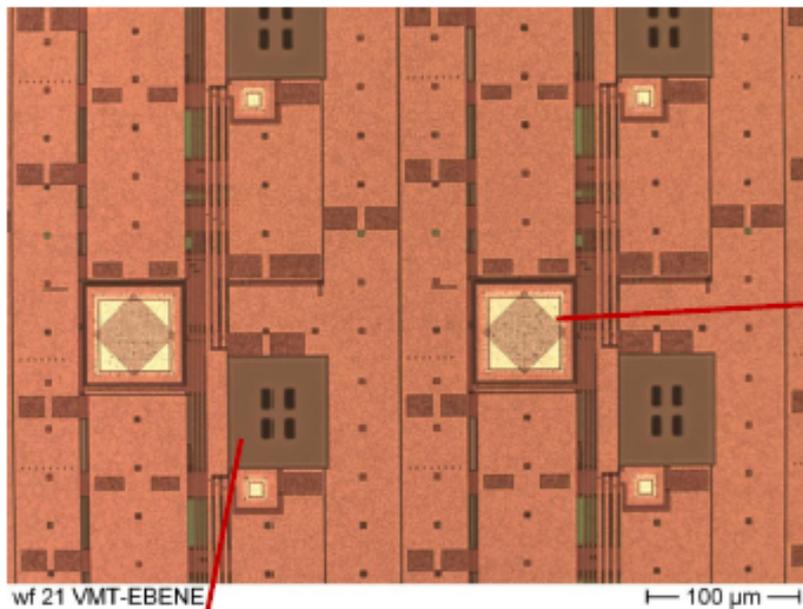


Specifications 3DIC

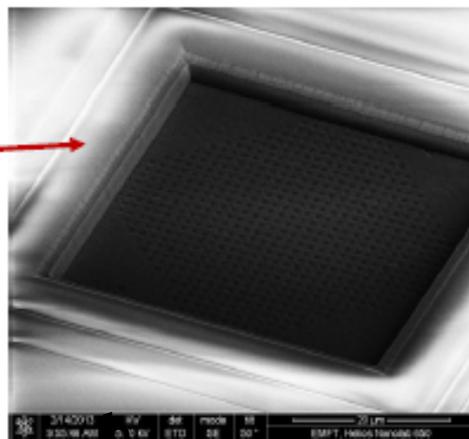
- Technology ASIC: AMS 0.35 μm
- 40x40 pixels
- Effective pixel pitch 250x250 μm
- 4-side buttability
- Digitization modes 12 and 10 bits
- Output of “hit-pixel”
- Each pixel should be able to handle 2 hits/readout (~deadtimeless operation)

First round

- 12 wafers containing both tiers produced, tested and shown to be well functioning. (pre-AIDA)
- In 2011 EMFT were contracted to thin the “Analogue” wafers
- In 2012 EMFT were contracted to finish the SLID bonding (there was an unfortunate long delay between these two steps because of contract issues)
- The first SLID parts were delivered in Mid 2013 (rather than end 2012)
- The first full wafer of SLID parts were delivered in Oct 2013

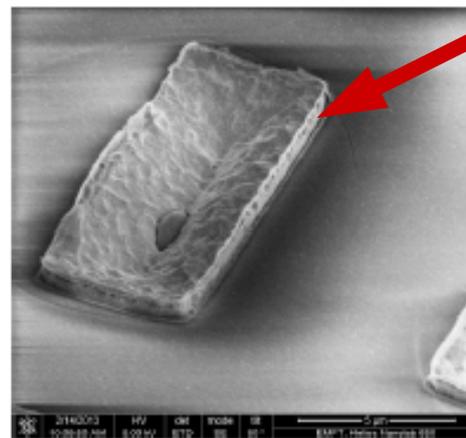
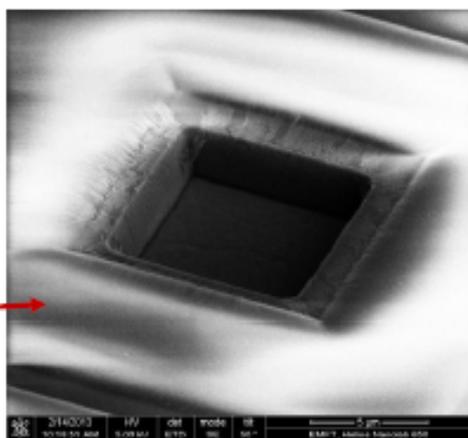
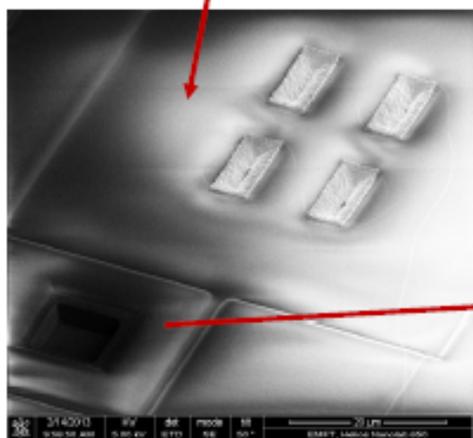


- View of pad and in-chip areas after tungsten etch and oxide opening to device pads;
- Resist is still on top of oxide



- Oxide on device pads is removed

3µm x 10µm TSV



Division Nanomaterials,
Devices and Si Processing – NDS

Armin Klumpp
Device and 3D-Integration

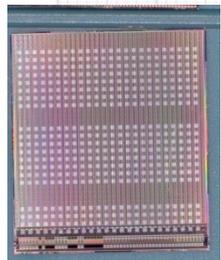
Fraunhofer
EMFT

Deliverables (& lessons learned)

- TSV processing and contact metalization went generally OK
- Excessive stress induced in the thinning process (to 50 μm) and this had to be modified to stop the wafers cracking
- Back side metalization critical and is one of the main worries.
- EMFT delivered a wafer of SLID bonded ASICs and some non-bonded parts



Analogue (top)



Digital (bottom)

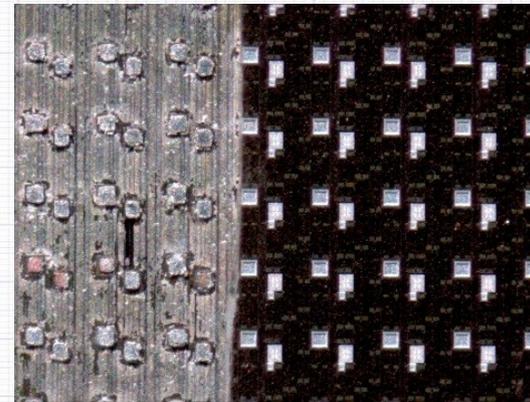
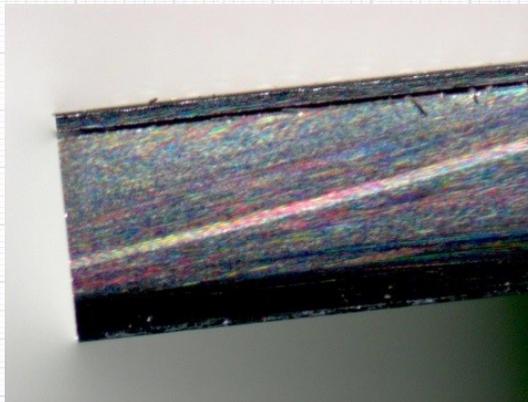
- 9 proper devices (thin top analogue to thick digital) on the wafer that are properly SLID bonded together
- 10 thin top digital bonded to thick analogue. The SLID bonds are not functionally and the devices have a non-functional checker-board Al pattern on top surface. These do have good wire bond pads so can be connected to test boards.
- 5 thin analogue and 5 thin digital ASICs. One analogue ASIC went for stress imaging at ANKA.

Cont.

The full SLID wafer is visibly very poorly bonded (Fig 2) and we do not expect any good devices but there could be valuable indications by using the new system. We have used some ASICs from the wafer but there were only 6 devices worth taking from the wafer.

Analogue
SLID

Digital



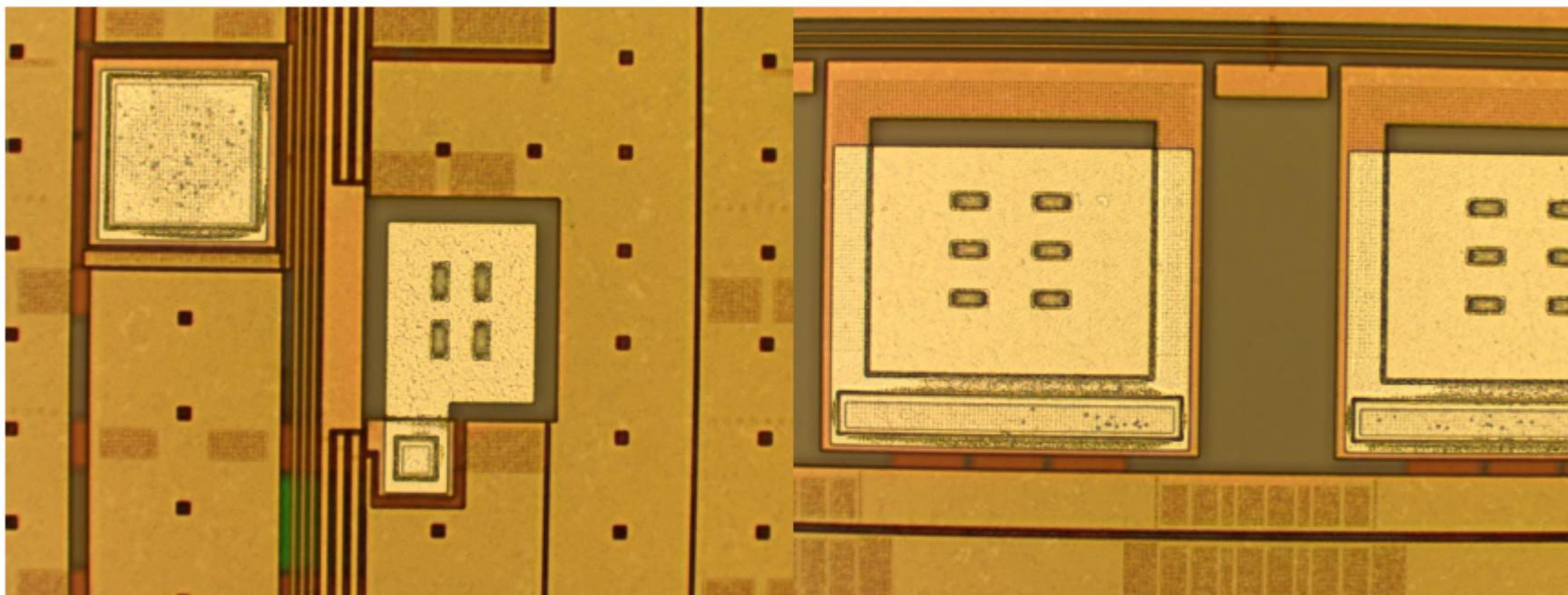
← Digital (bottom) ← Analogue (top) →

EMFT agree, that the device SLID looks very poor and there will be very poor yield. 3DIC is still strategically important for them and they have committed to continue the development. They agreed to reprocess devices Free Of Charge if we can provide more wafers.



Second round

- Reduced depth of TSV and therefore remaining silicon thickness to 24 μm
- Tungsten filling successful to the bottom of the TSV
- Single TSVs without isolation trench to improve mechanical stability nearby through contacts
- Backside preparation shortly before metalization of TSV contacts

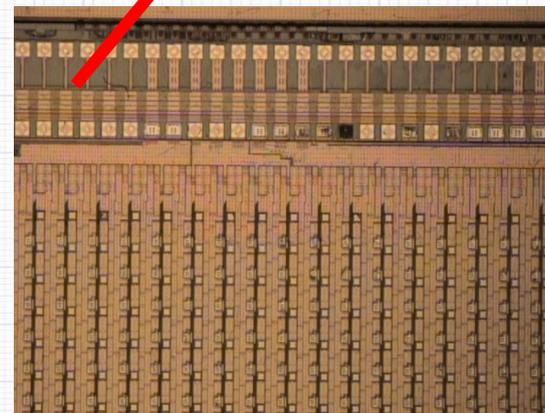
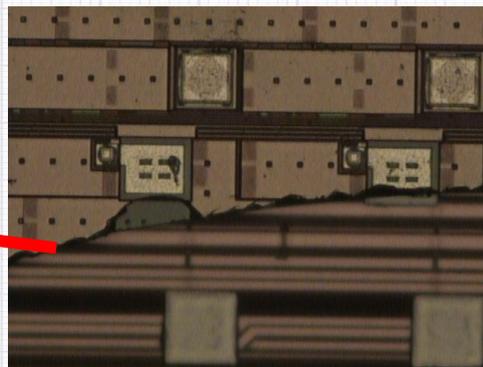
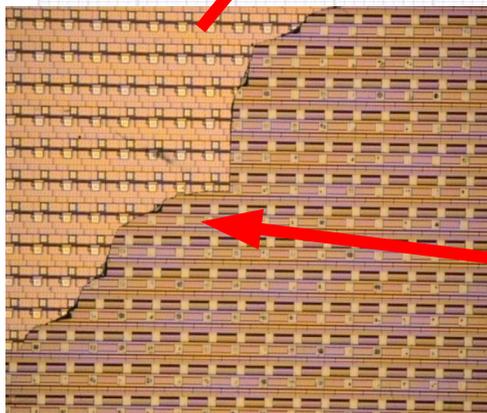
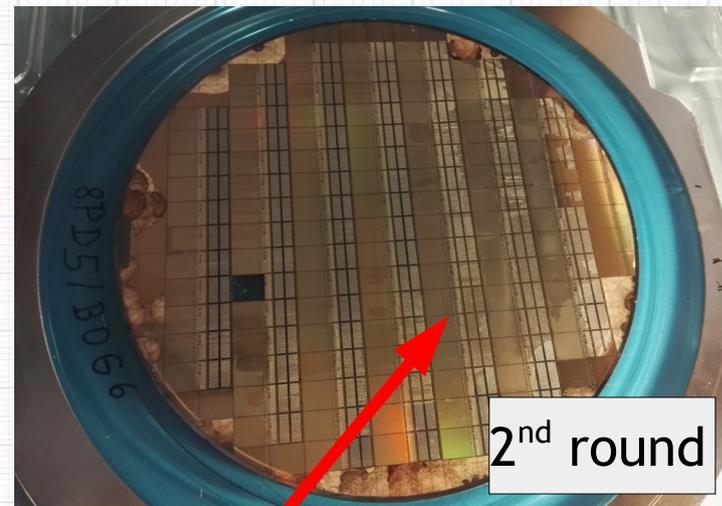
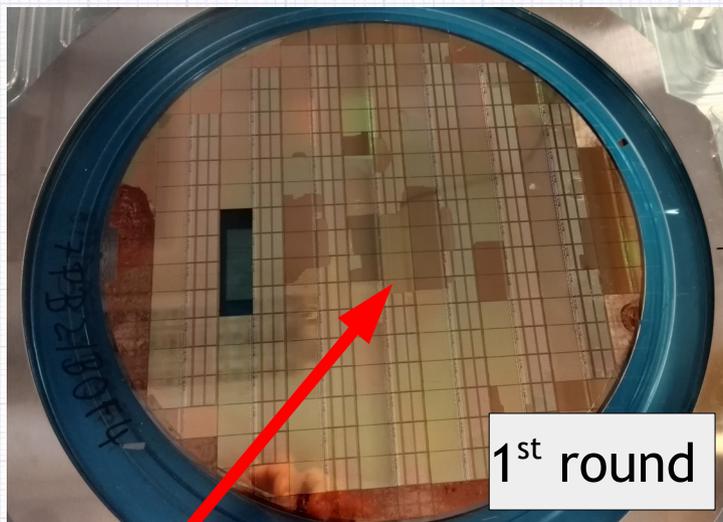


- Aluminium contact of TSV to device within array

- Aluminium contact of TSV to device at bond pad

First look

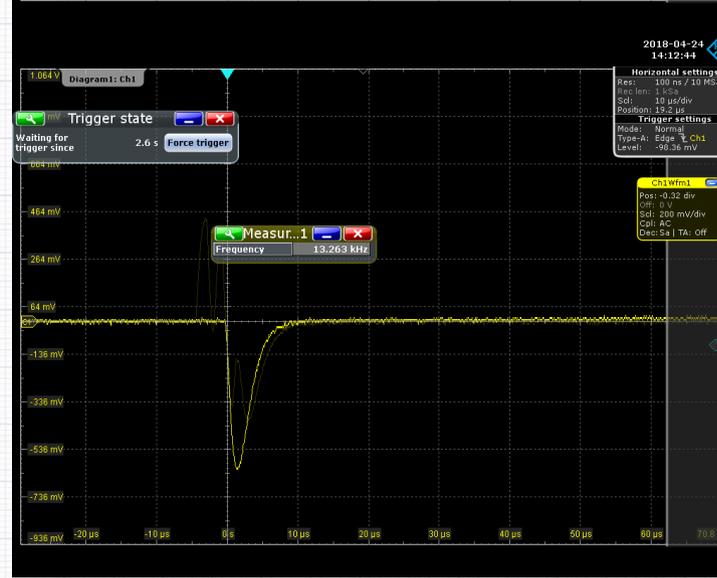
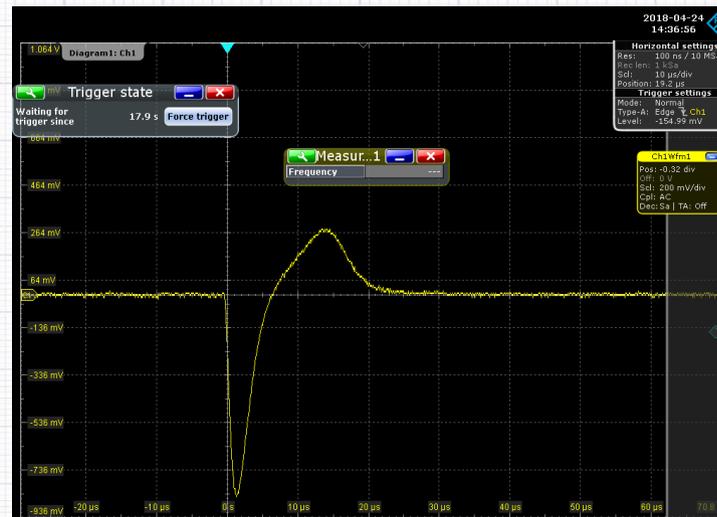
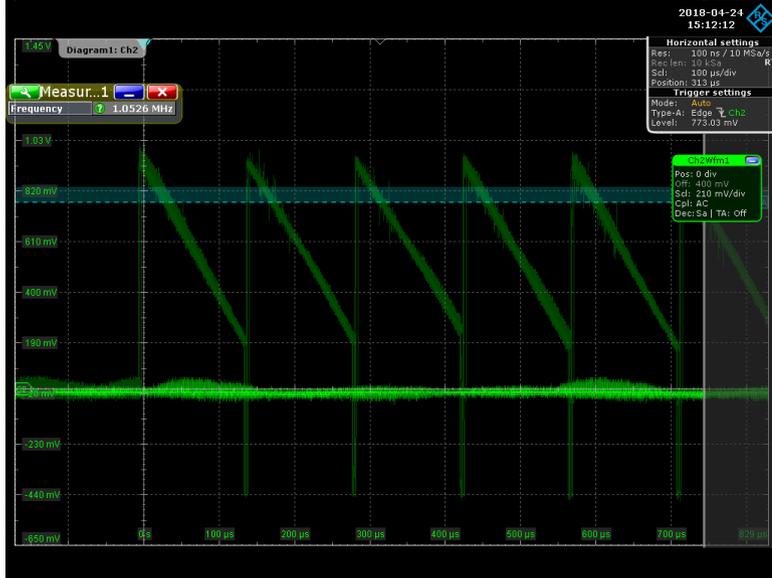
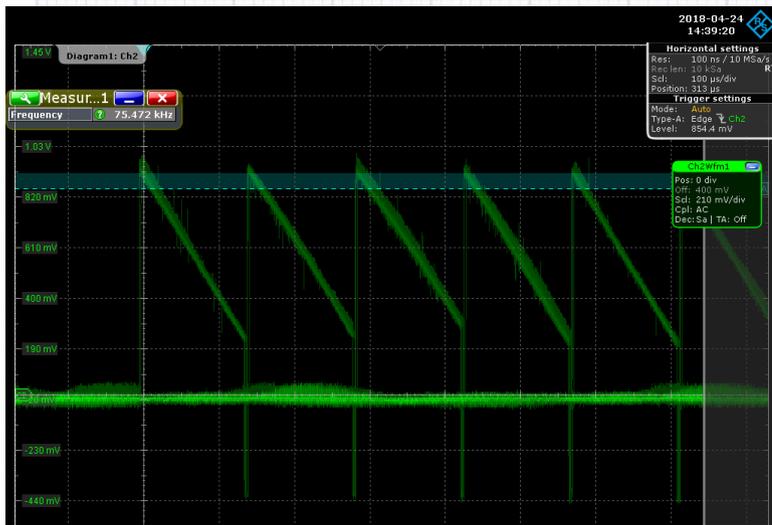
- The reprocessed wafer do not show any adhesion problems between the two tiers.



Some measurement results

- We have bonded a few chips and done some measurements.
- 12, 1st round chips tested
- So far only 3 2nd round chips tested.
- Trend is the same in both rounds.
- Few chips only digitally working. Correlated with no analogue current drawn
- Few chips with working analogue side. Correlated with analogue current but some draw “normal” amount of digital current.
- No chip yet with analog and digital working at the same time.
- Indication on only one chip that there is a resistive path due giving a little elevated consumption. “Typical” failure mode is low or no current to the part not working.

Scope images





Next steps

- More 2nd round chips in preparation still to be measured this week.
- Perform on “promising” chips a parameter scan in hope that they come to life (modifications to the LabVIEW project).
- Strategy for chip pathology before FIB/SEM studies.
- Perform FIB/SEM studies on a few chips.