

## **Development of fast-timing large RPCs**

*Prototypes of large, high-rate RPCs are designed, built and tested as well as a dedicated readout for time response optimisation. The concept is validated by exposing large RPC prototypes to test-beams and accessing their performance, namely their high-rate capabilities and their fast-timing properties.*

**D13.2** High-rate characterisation of large-size RPC prototypes (*qualification at high intensity beam lines of large-size prototypes of optimised RPCs optimised for the rate response and the fine time*) M44

1st year	Conception and construction of large RPC/MRPC, Test of PETIROC, TDC
2d year	Design of optimized PCB for RPC/MRPC, integration of TDC into PETIROC (in collaboration with WP4)
3d year	Realization of a prototype, development of DAQ system (in collaboration with WP5&WP14)
4 <sup>th</sup> year	Beam test and validation & final report

# High rate fast timing RPC

-A high rate RPC ( $> 1 \text{ kHz/cm}^2$ ) has been developed both with Bakelite and low resistivity glass as electrode.

-Excellent timing FEE (PETIROC) is developed and being upgraded

The following scheme is proposed for the CMS RPC upgrade

## Principle:

To use the 2D readout with good timing FEE (PETIROC)

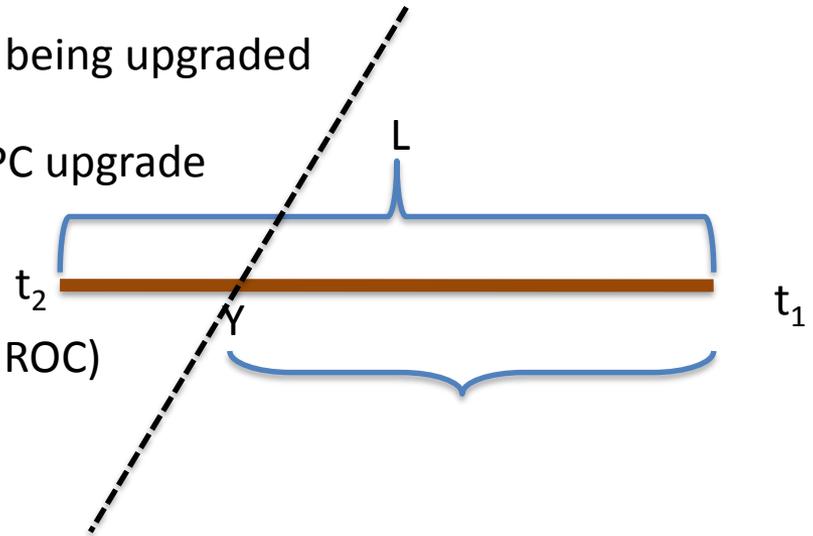
## Motivation

1) Better  $\gamma$  determination

$$Y = L/2 - v \cdot (t_2 - t_1)/2 \rightarrow \sigma(Y) = v \cdot \sigma(T_2 - T_1)/2$$

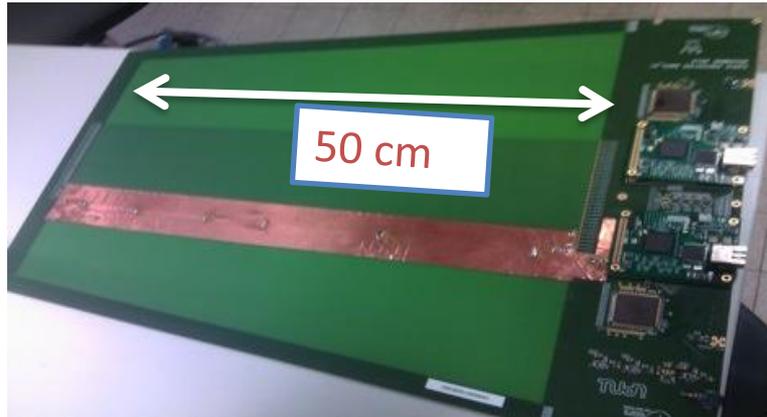
2) Less channels ( $2/\eta$  rather than 5)

3) In addition, with 2-gap RPC of 1.4 mm gas gap 0.5 ns absolute time resolution could be achieved  $\rightarrow$  noise reduction and better Muon and HSCP trigger performance

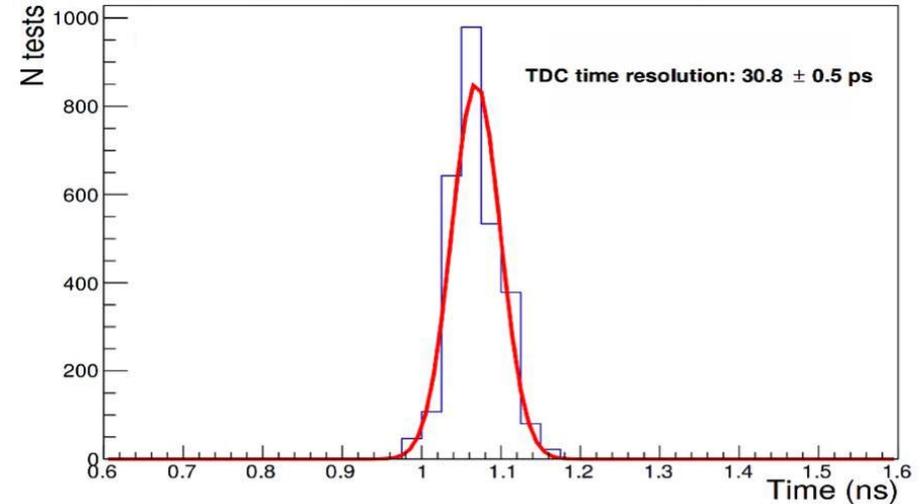


# CMS RPC Electronics

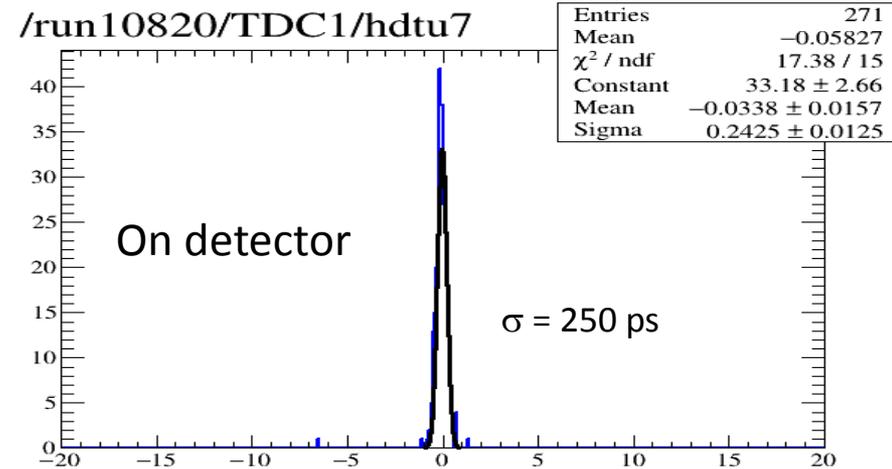
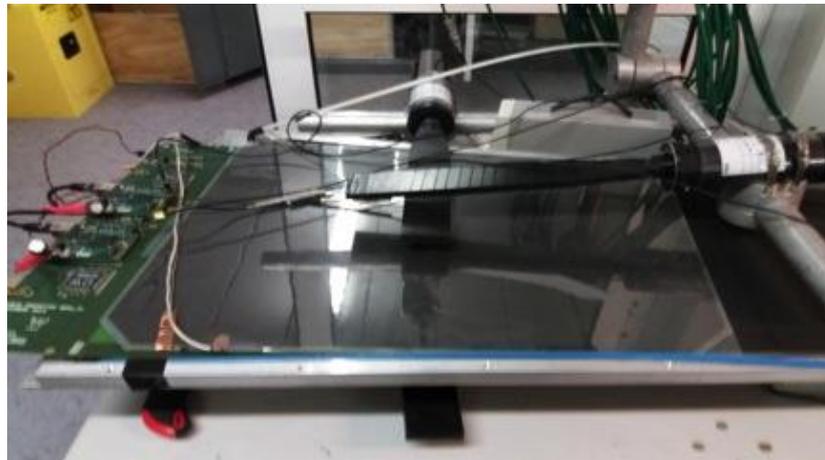
First demonstrator : 32 on-detector strips with 3.5 mm pitch and 32 off-detector return strips 1 mm pitch  
→ 64 channels = 2 PETIROC + 2 TDC (Delay Line TDC on FPGA  
→ , 10 ps of LSB)



## By charge injection on the strips



## Using cosmic rays

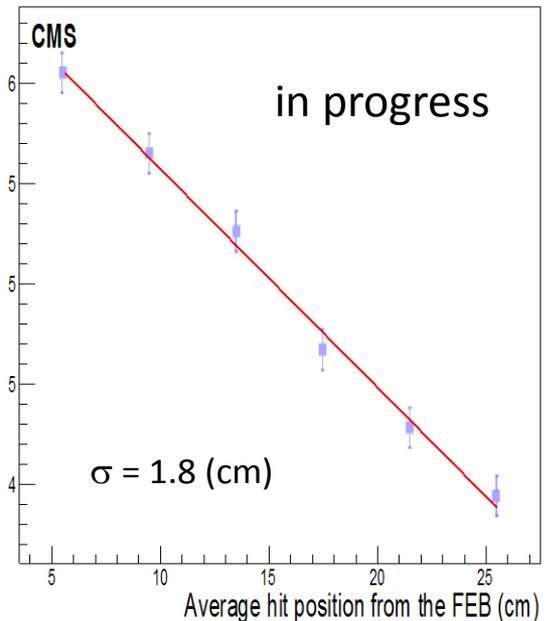
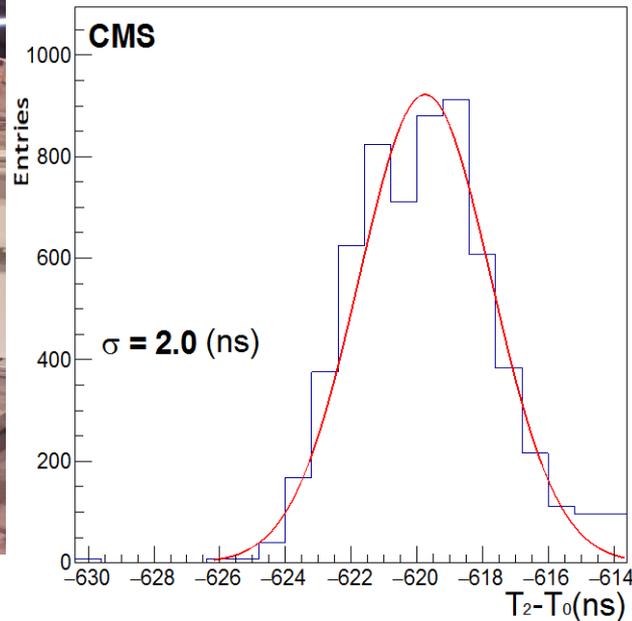
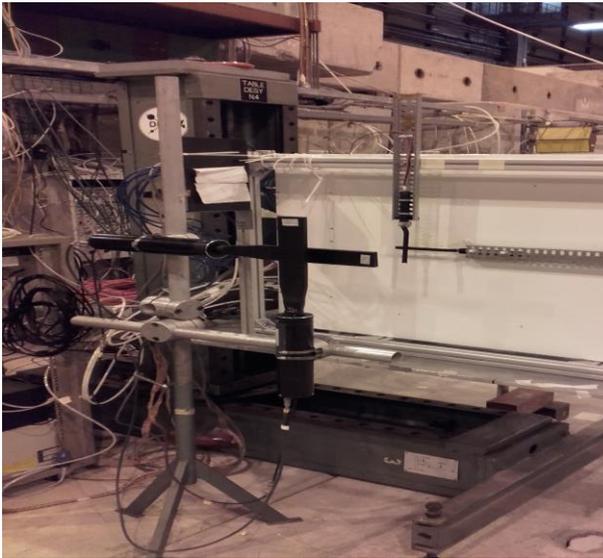
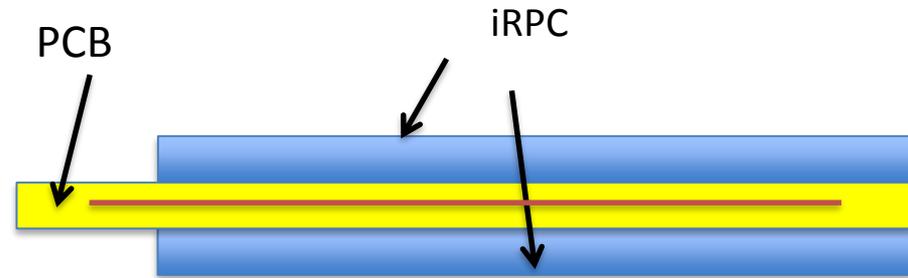


- Only one detector
- Scintillator resolution correction not included
- Cluster size correction improvement not included

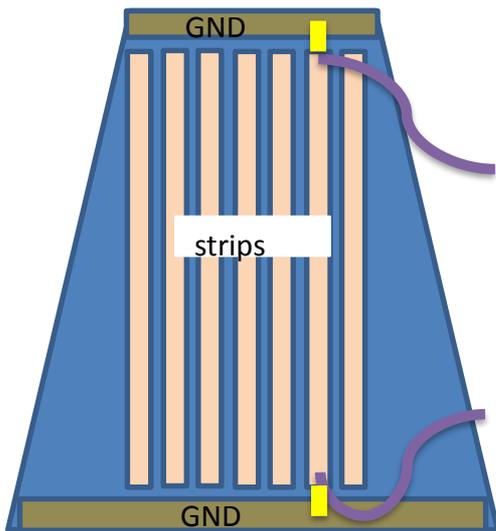
The readout electronics was then tested on iRPC detectors in TB:

- 2 iRPC chambers :1.4/1.4mm and 1.6/1.6 mm
- Scan studies were performed using moving tables (< 1mm resolution)

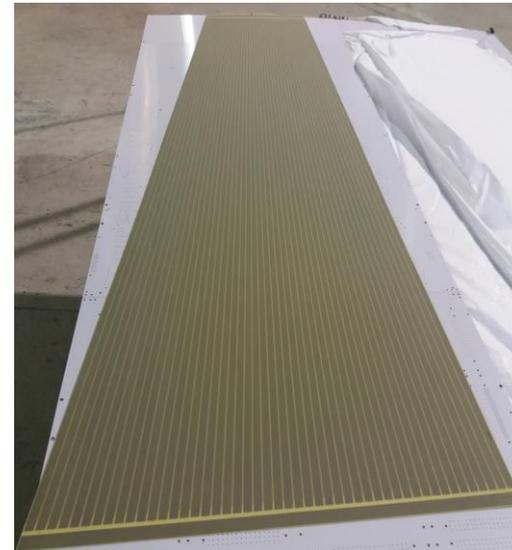
- A DAQ system using external trigger built with small scintillators (few cm width) was used



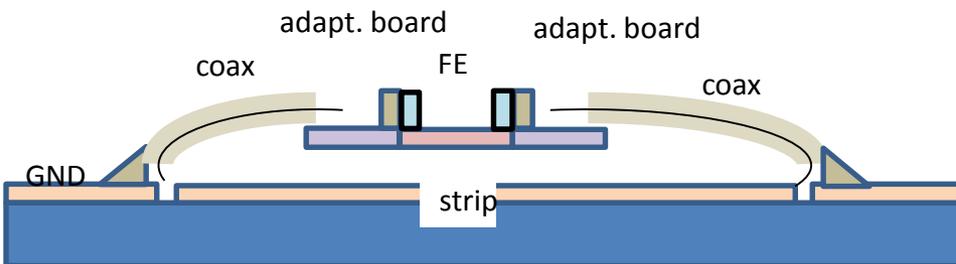
To read out CMS RE3/1 and RE4/1 RPC, long PCBs (160 cm) are needed. No possibility to have 6-layer PCB of large size. Two solutions are proposed: **First solution** :One layer PCB with strips. Return-strips are replaced with coaxial cables with the same impedance (company found : ELVIA).



Two large PCB are needed for the readout of one RPC chamber



6 petiroc of 32 ch are needed



This solution is equivalent to the one already tested but simpler and cheaper. Still, we will produce a large PCB with return strips on the edges to compare the two schemes

To estimate the strip impedance, several methods were used.  
 Varying a termination resistor, TDR, RLC meter

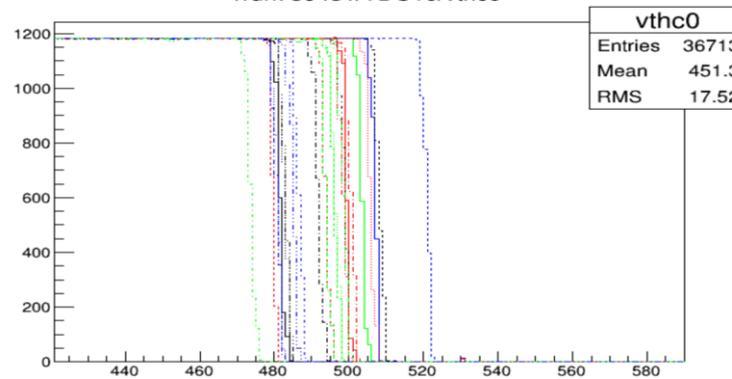
Frequence (kHz)	Cote	Cp (pF)	Gp $\mu$ S	LS (nH)	Rs (m $\Omega$ )	Zc ( $\Omega$ )
1	Large	574	0.157	723	273	275
10	Large	622	6.4	577	275	84
100	Large	450	63	541	292	39
500	Large	337	342	503	362	38.2
1000	Large	284	600	492	416	38.6
2000	Large	244	934	482	467	43.5
1	Etroit	595	0.170	720	275	271
10	Etroit	620	6.4	583	277	84
100	Etroit	450	62	547	294	40
500	Etroit	337	344	510	362	38
1000	Etroit	284	600	499	414	41
2000	Etroit	244	934	487	461	44

At high frequency (fast RPC signal) the impedance value is around 42  $\Omega$ ,  
 Using 50  $\Omega$  coaxial cables is a cheap solution. Modifying the strips width or  
 producing 42  $\Omega$  coaxial cables could be envisaged.

Electronics board equipped with PETIROC and delay-line based TDC were conceived and produced.

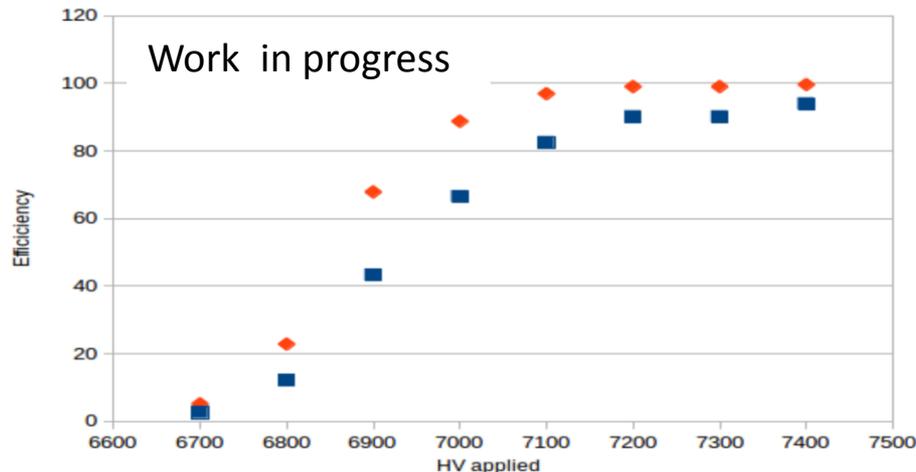
PETIROC ASICs were calibrated by changing the 8-bit DAC value of each channel to:

- adjust the pedestals
- adjust the S-curve



A dedicated DAQ (**LyDAQ**) system was developed. It allows the readout the TDC channels and associate their content them to the trigger signal ( this is injected in one of the TDC channels)

Preliminary results on detector are encouraging

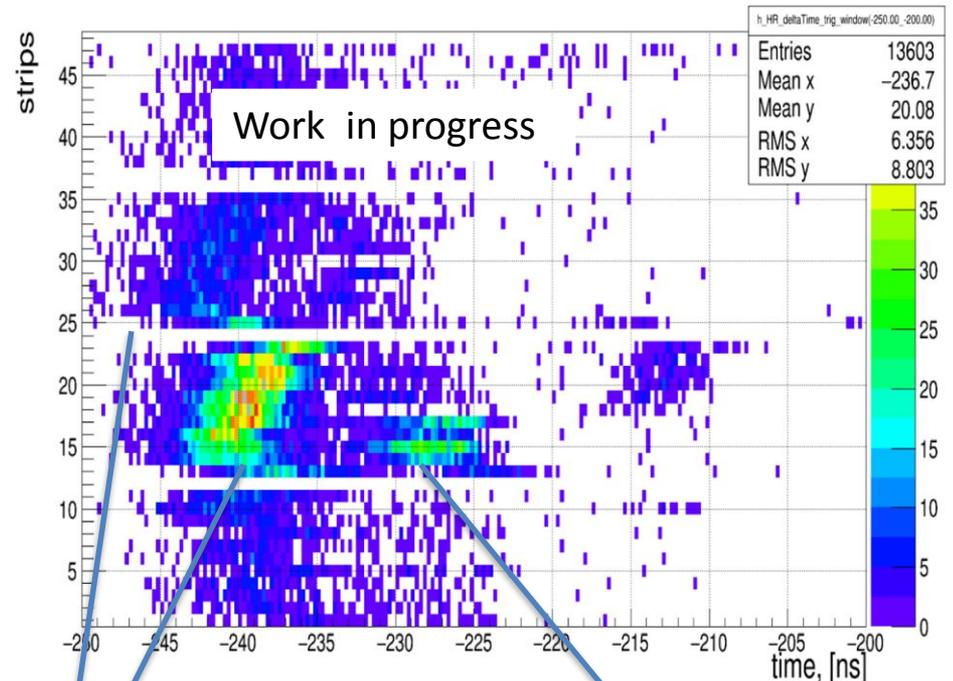
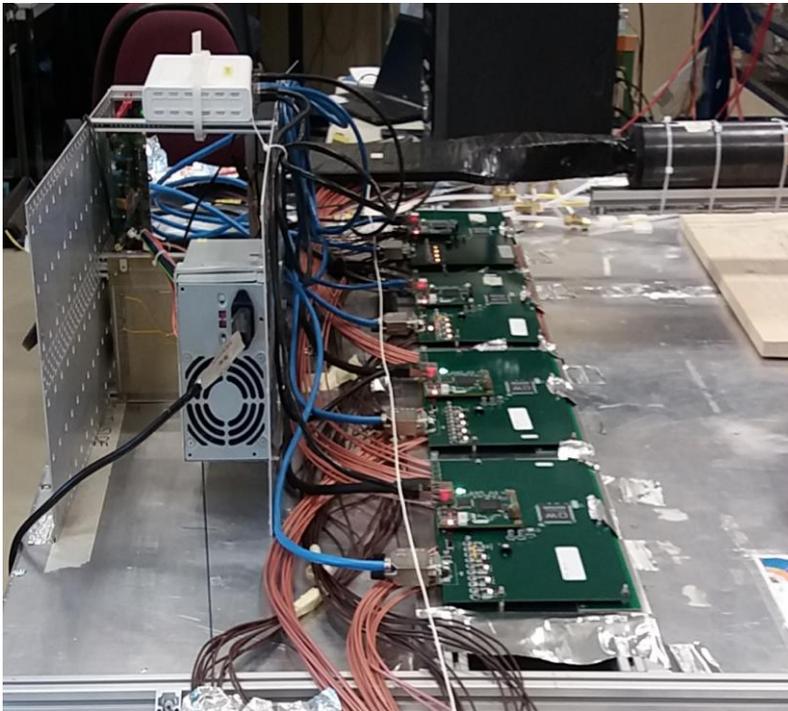


**Red**: efficiency of at least one of the two channels associated to one strip

**Blue** efficiency of having two channels associated to one strip

Readout system is being tested in cosmic bench on RE3/1 chamber.

First results showing good efficiency (>90%) with average time resolution of 200-300 ps leading to 2-3 cm spatial resolution



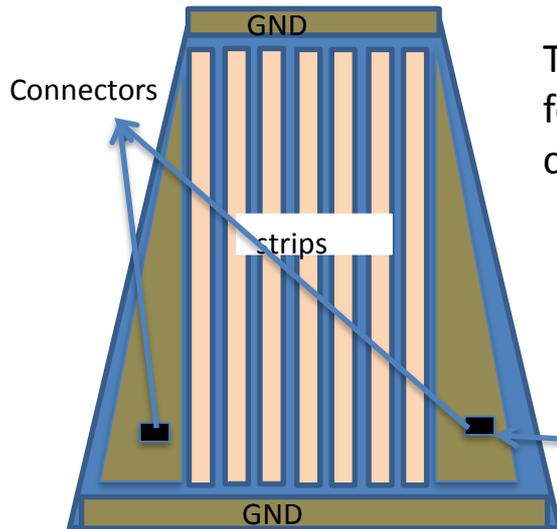
Missing channels

Mis-matching  
channels

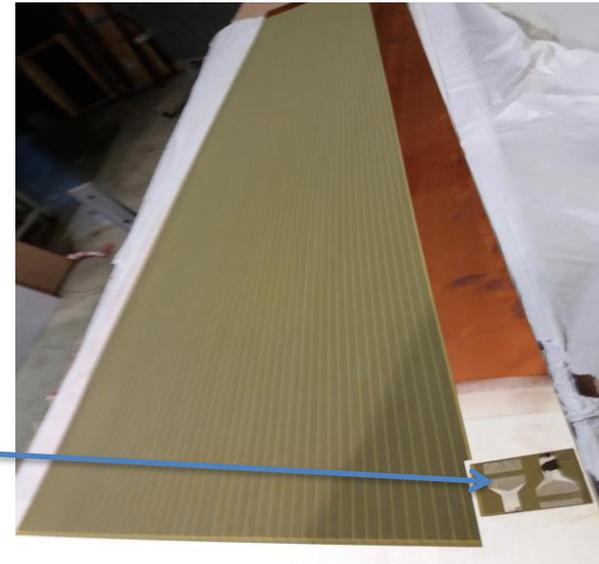
To read out RE3/1 and RE4/1 RPC long PCB (160 cm) are needed.

No possibility to have 6-layer PCB of large size. Two solutions are proposed:

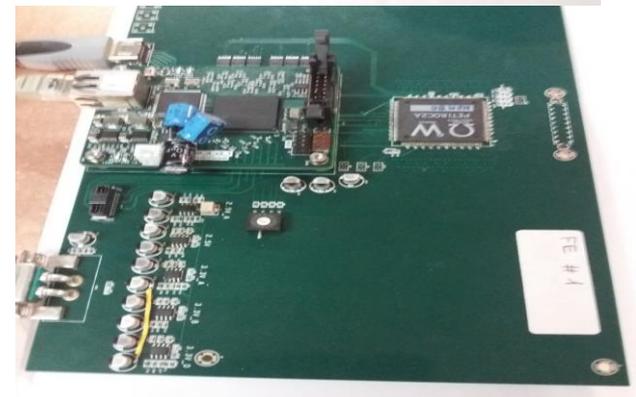
**Second solution** : “3”-layer PCB with strips and return-strips are replaced with the same impedance. Same as for small PCB but without the readout electronics.



Two large PCB are needed for the readout of one RPC chamber



Flex will transmit the signal from the two ends of strips to the FEBs



This solution is as simple as the previous one and provides well controlled impedance

-To completely validate the readout electronics on large RPC CMS chamber using a few FB boards in TB ( this week)

-TDC with new FPGA with more resources to allow the TOT exploitation is being developed. Time resolution of 17 ps is obtained for rising/falling signal measurement and 20 ps for TOT with a dead time of 2 ns.

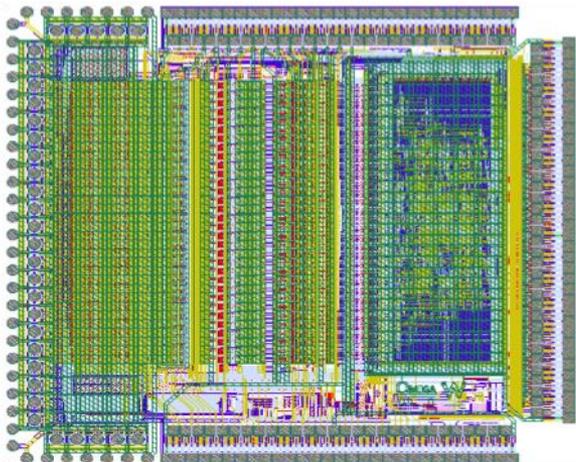
-In parallel TDC chip is being developed in collaboration with WP4 (see M. Dahoumane's talk) aiming for better performance while reducing power consumption.

#### Next steps

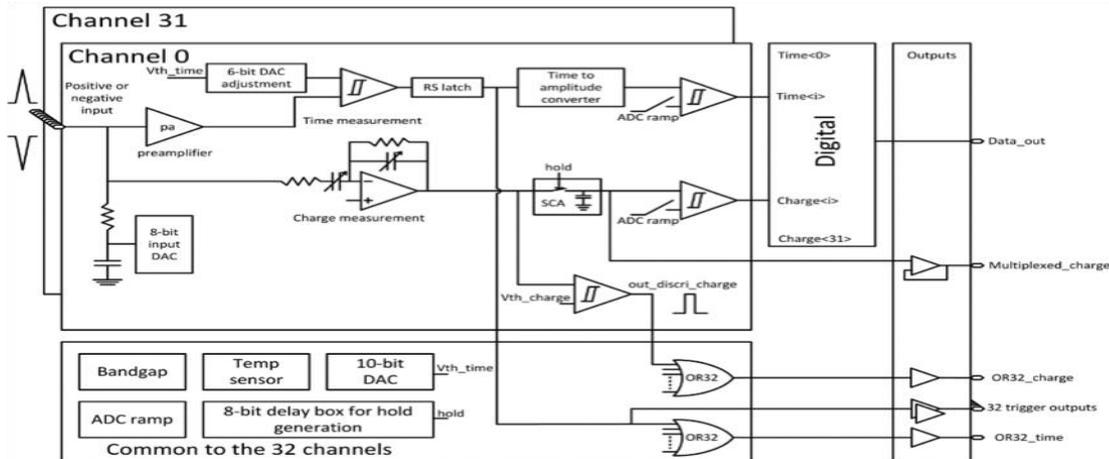
-Assemble the FE boards in one hosting the Petirocs in addition to the Master FPGA to communicate with the CMS DAQ/Trigger system.

- Upgrade the Petiroc from 32 to 64 channels (for compactness, not a technological challenge) and go for TSMC 130 nm ( in synergy with the HGCal ROC) for better radiation hardness even though the expected rate where the FE board is to be fixed is not high (fluence of a few  $10^{12}$ )

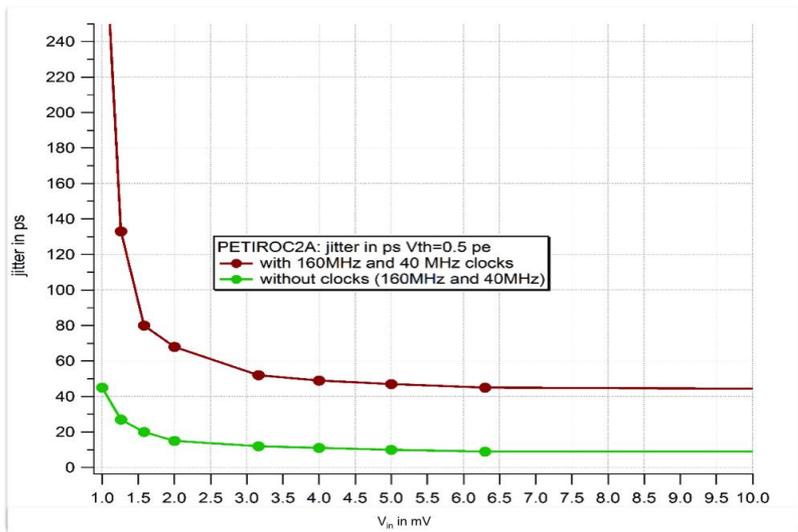




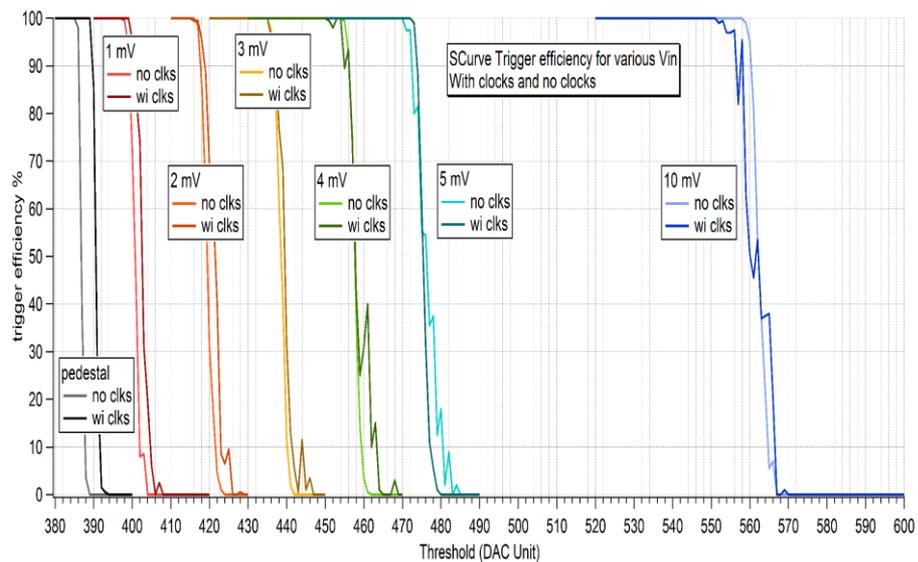
PETIROC ASIC, 32ch, SiGe 350 nm technology



Petiroc scheme : only the preamplifier output will be used



Time resolution as a function of the injected charge  
 1 mV corresponds to about 55 fC



Petiroc S-Curves :

1 DAC unit corresponds to about 3.5 fC

Backup