

Status report

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Design of a Multi Chip Module for a general purpose readout system for MPGD:s

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(on behalf of the Lund group)

Reminder

The goal of the full project: Construct a TPC with excellent position resolution and two-track separation.

This requires:

Small readout pads ($\leq 1 \times 6 \text{ mm}^2$).

The channel density of the readout electronics has to match the small pad size.

- The aim of the project is thus to produce front-end electronics comparable in size to the readout pads.
- This readout electronics can be used in smaller MPGD-detectors for applications in various other fields like medical diagnostics, material science at XFEL, and for investigations at ESS.
- The readout electronics is based on the **SALTRO16 ASIC**, which integrates the analogue and digital processing in the same chip.
- The size of the die itself is about $8.7 \times 6.2 \text{ mm}^2$, which corresponds to a channel occupancy of $3.37 \text{ mm}^2/\text{channel}$.

Eight SALTRO16-chips are mounted on a **Multi-Chip-Module (MCM) board**, which also contains a CPLD, connectors and passive components. This increases the channel occupancy to $6.4 \text{ mm}^2/\text{channel}$

The total number of SALTRO16-dies is 840, delivered in different batches to a French company, which is doing the packaging.

From an initial visual inspection of a limited number of dies, the company got the following impression:

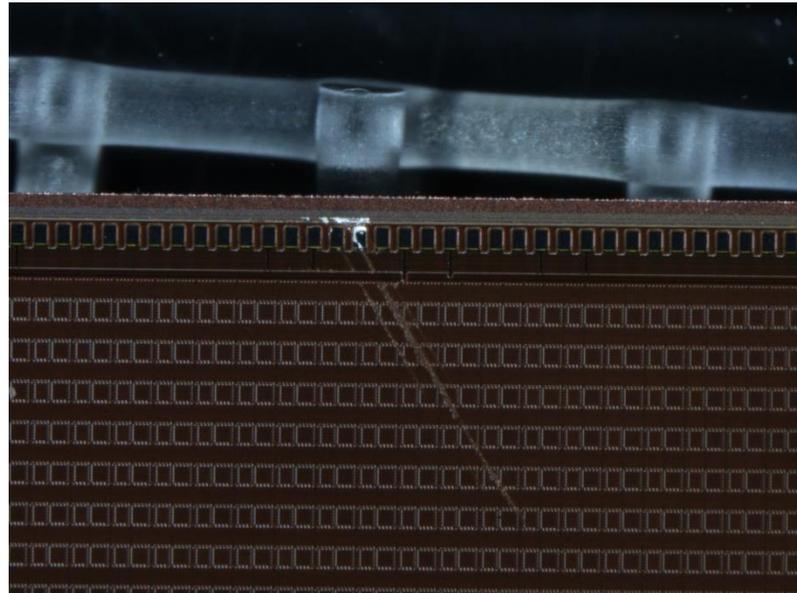
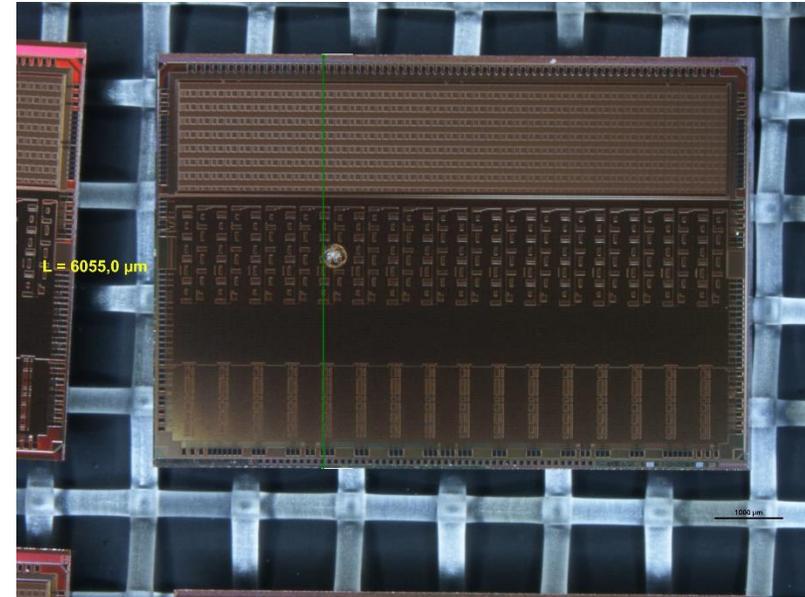
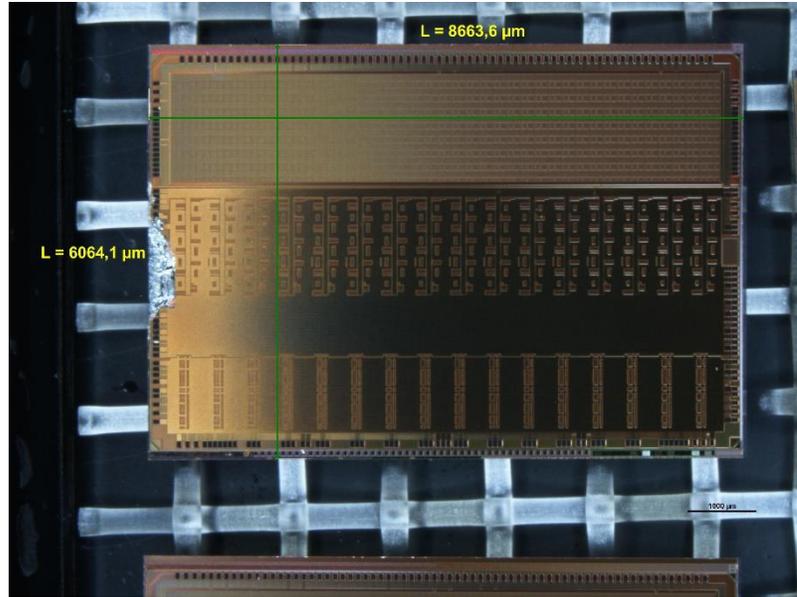
- Saltro n°3 in Waffle packs from CERN (70 units) => 8602 x **5846** μm^2 (good quality)
- Saltro n°4 in Waffle packs from CERN (70 units) => 8604 x 5971 μm^2 (good quality)
- Saltro in Gel Packs from CERN (about 100 units) => 8663 x 6055 -**6111** μm^2 (poor quality, see photos)
- Saltro from Sweden in GP (about 4 x 30 units) => 8573-**8622** x 5975 – 6075 μm^2 (see photo GP1 to 6)
- Saltro from Sweden in Waffle pack (about 480 units) => **8502** x 5989 μm^2 (good quality)

From measuring the dimension of a selected number of dies, the company found a fairly big variation in size.

This may be explained in case the wafer was cut at different times and maybe by different suppliers.

The size variation may cause problems for a successful packaging in our small capsules. Discussions are going on with the company how to circumvent this.

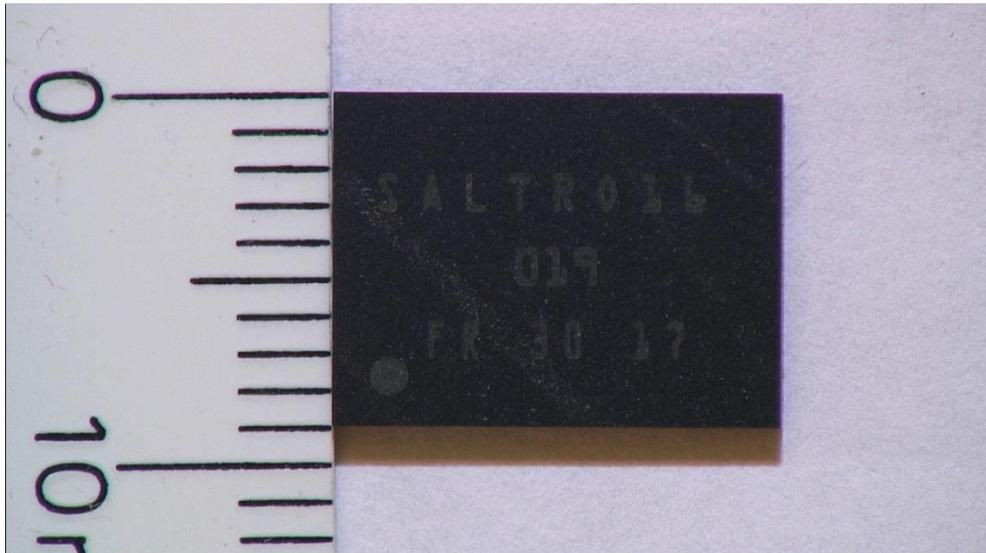
Examples of bad quality dies



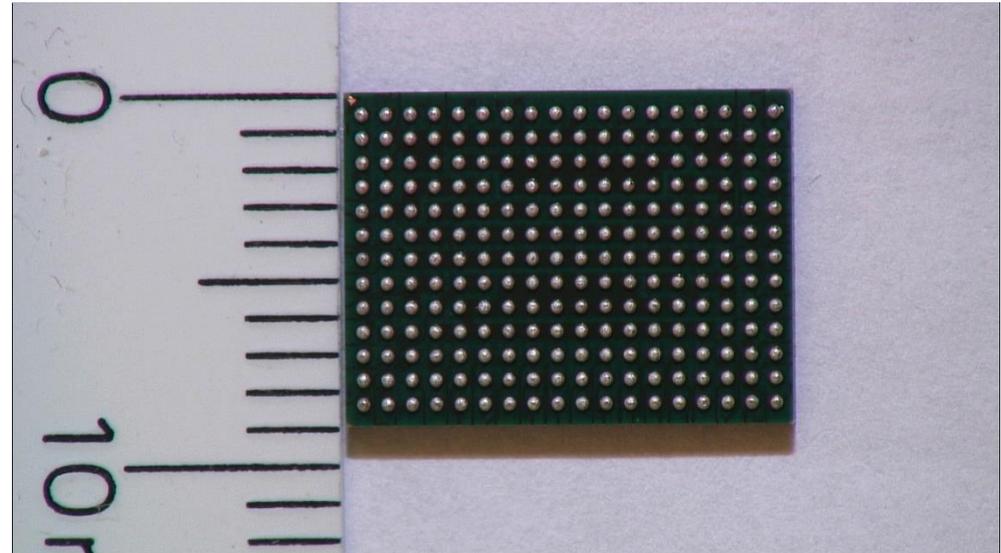
The packaged SALTRO-16 chip

- We have obtained a pre-series of 34 packaged substrates, from the French company, for testing their functionality. The dimensions of the chip are 12x9 mm².
- In addition we have got 40 empty capsules, which will be used for soldering tests onto the MCM-board.
- The substrates for all 840 dies have been ordered

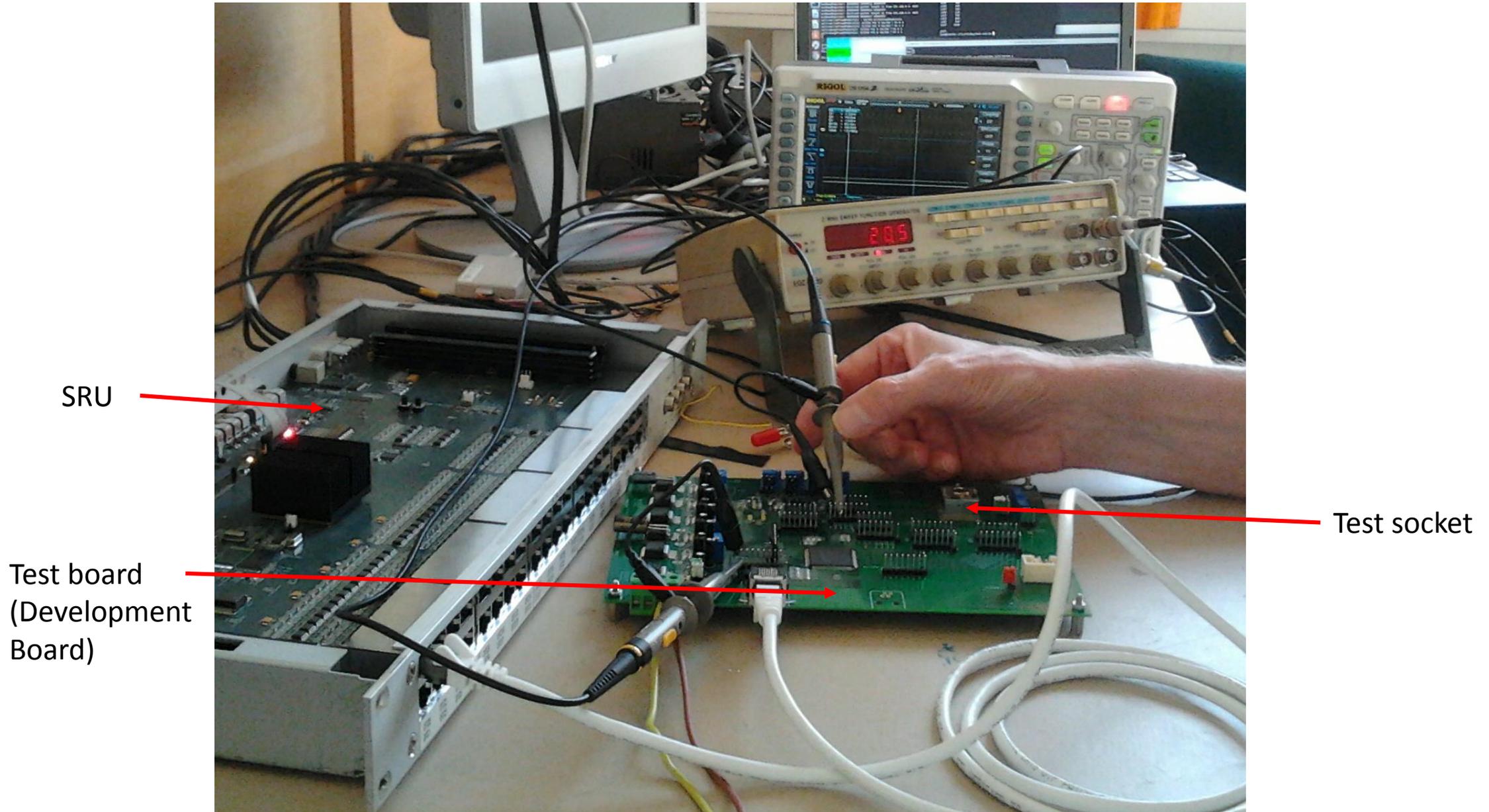
Top side



Bottom side

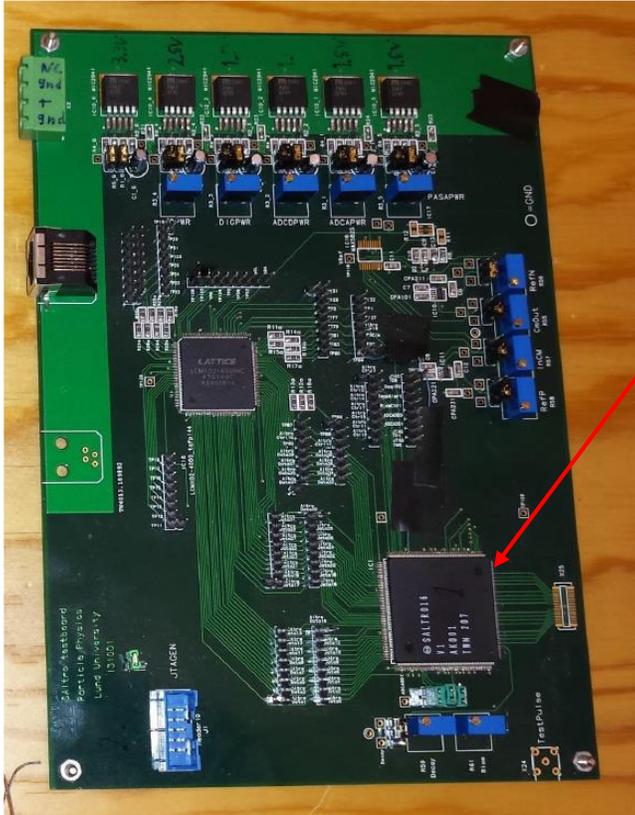


The Lund test set-up



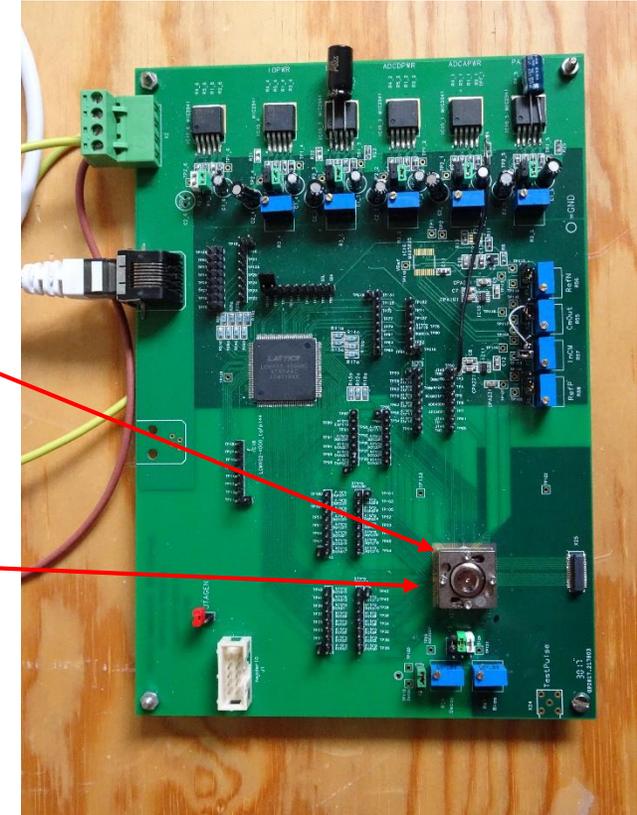
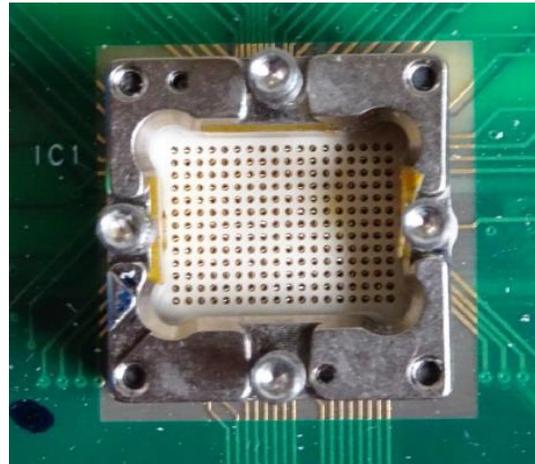
Testing the Lund test board (Development Board)

- In order to test the functionality of the Lund test board, it was equipped with a QFP-packaged chip, as used for tests at CERN.
- The chip that was mounted passed the CERN-tests.
- The tests in Lund gave results consistent with those from CERN \Rightarrow Indication that the test board is ok.
- On an identical board a test socket was mounted for tests of the BGA-packaged chips.



Chip in QFP-package

Test socket for BGA-packaged chips



Status of the SALTRO DAQ system

The CPLD: The firmware is done for the development board and has been used when testing chips.

The SRU: The firmware is partly done for the Development Board, what exist have been used when testing chips.

- We can read/write SALTRO and CPLD registers.
- We can send software triggers to the SALTRO.
- We can only read partial event data.

Still to do:

- Some intermittent problems on the SRU still have to be solved.
- Firmware on the SRU:s to read full events for up to 32 MCMs per SRU still has to be implemented.
- The trigger system to the SRU:s has to be implemented.
- Test of the full readout of the Development Board; the max data rate and the trigger rate.
- The CPLD firmware needs to be modified for the final MCM.

The PC DAQ:

- The modification of the ALTRO DAQ is done (use of ethernet UDP instead of ALICE DDL).
- The detector control between the SRU/CPLD and PC is done.
- New data format with respect to ALTRO DAQ.

Readout of the Development Board:

- The SALTRO DAQ has been used to test chips.

Detector control:

- Low Voltage control, temperature monitoring, reference voltage settings ... to be done.

Trigger handling:

- The trigger handling has to be implemented.

Monitor and run control:

- This is the same as in the ALTRO DAQ, modified for change of data format.

The prototype MCM-development board

The re-designed prototype MCM-development board is ready and the PCB is going to be ordered.

- Single Saltro16 readout in a BGA ZIF (zero insertion force) test-socket
- New reprogrammable CPLD, with a smaller footprint. This helps in the deployment of the component on the final MCM-board. Connections as in the final circuit.
- Same power distribution
- Test-points on all signals
- 8-layer board 210x145 mm² (The final MCM-board is 25 x 32.5 mm²)
- No impedance control, no signal timing/length matching
- HDI design because of BGA footprint (buried 0.1mm vias)
- 3 signal layers, 5 power layers

This board will be used for:

- debugging the MCM-board itself
- characterizing single SALTRO16 chips
- test the FPGA firmware and to establish the communication between the SALTRO16-chip and the SRU.
- further develop the DAQ system for the final system

Test results

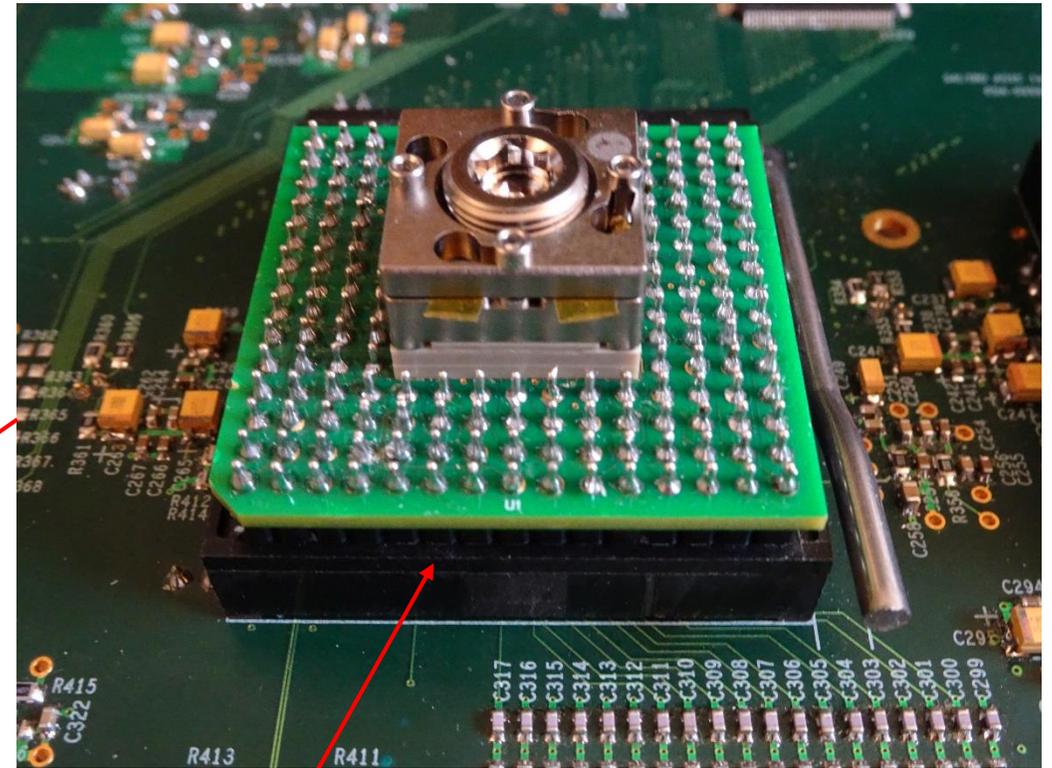
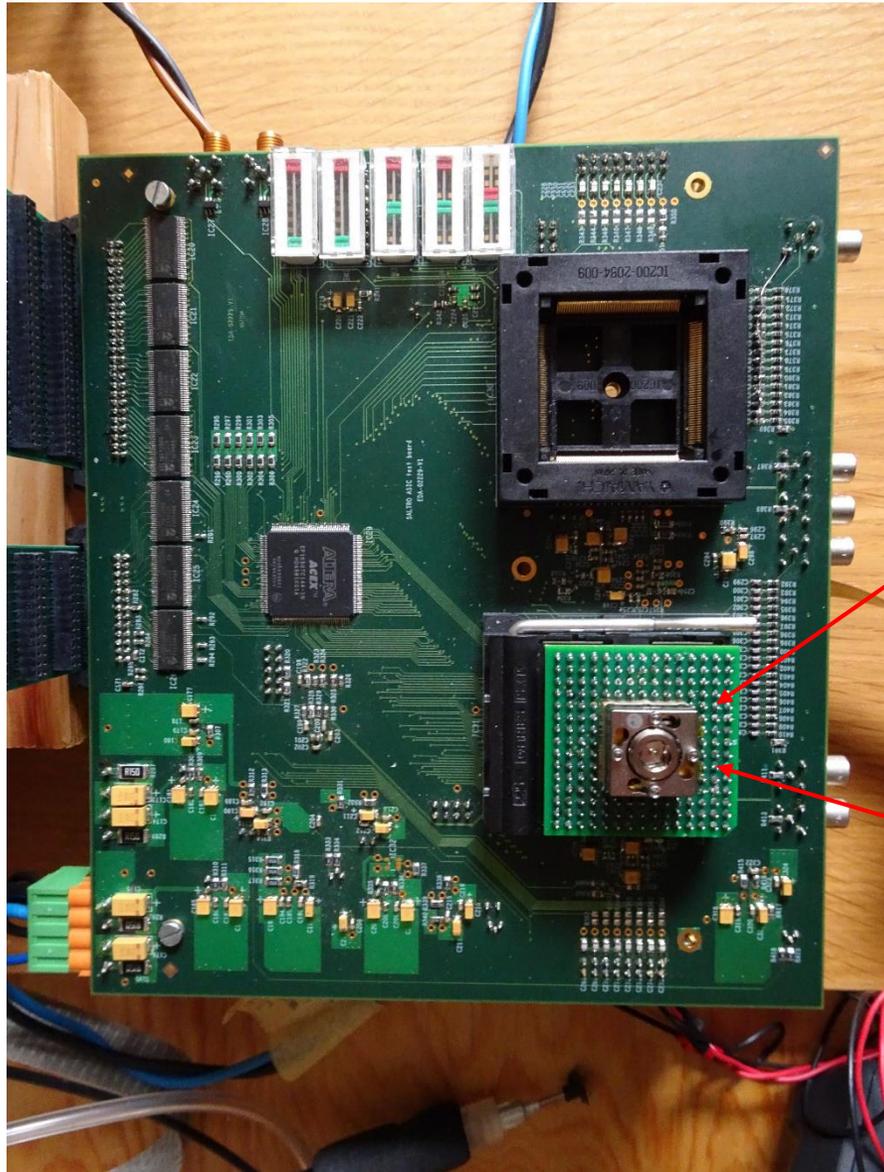
The first test of all 34 chips with the Lund test board gave the following results:

type	Number of chips	comment
1	20	Passed the test
2	6	Oscillating ADC values, one channel per chip
3	3	Bit problem, one channel per chip
4	1	Short between power and ground
5	4	No connection to die.

The number of fully working chips corresponds to about 60% of all chips.

We wanted to make sure that the strange behaviour of the nine chips of type 2 and 3 was not caused by some bug in our test system.

To do so we designed an adaptor board which could be mounted in the PGA-socket of the CERN test board and onto which a test socket for the BGA-packaged chips was mounted.



Adaptor board with a test socket for BGA-packaged chips. The adaptor board is mounted on a PGA-socket sitting on the CERN test board

The same results were obtained which convinced us that the Lund test board is ok.

Our conclusion is that the problems are either due to errors in the chip design/fabrication or in the packaging.

ACTION:

Inspection and size measurement of the chips has been required before selection for packaging.
Another 55 chips is being ordered

Summary

The first 34 SALTRO16 chips have been tested for their functionality using two independent and quite different readout systems, giving essentially the same results.

The fraction of usable chips is as low as 60%, which has led us not to order packaging of the remaining lot but have decided to limit the order to 55 units.

The DAQ system is working for testing the chips but for the final readout system there are still a number of things to do.

The MCM Development Board has been redesigned and the PCB is going to be ordered.