Measurements on +/-12.5 kV Inductive Adders with +/-200 ppm Pulse Flatness over 900 ns for CLIC Damping Ring Kickers at CERN

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Outline

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  - Specifications for CLIC DR Extraction Kicker Modulator
- Inductive Adder
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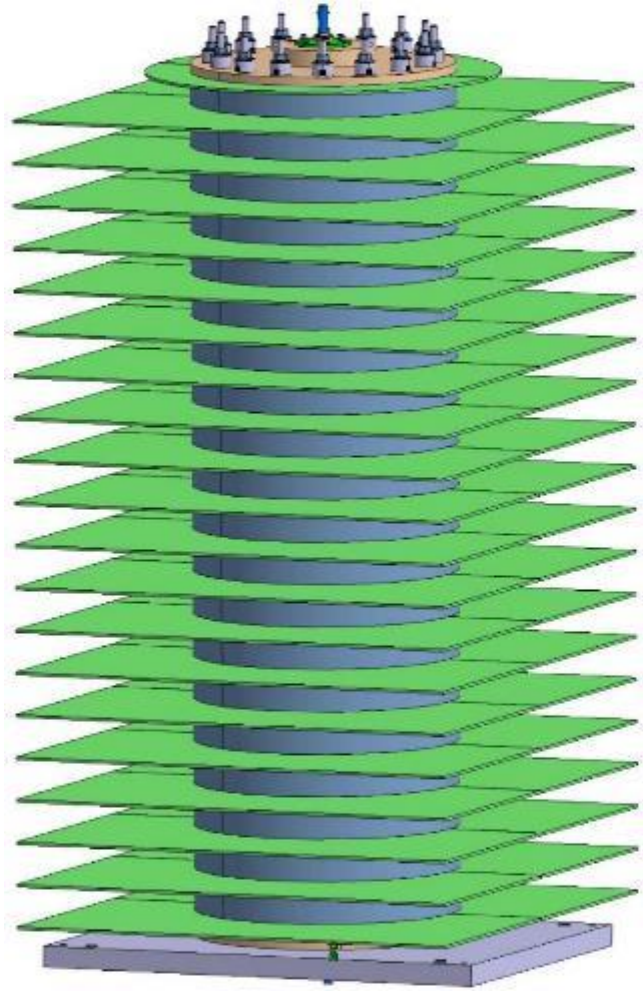
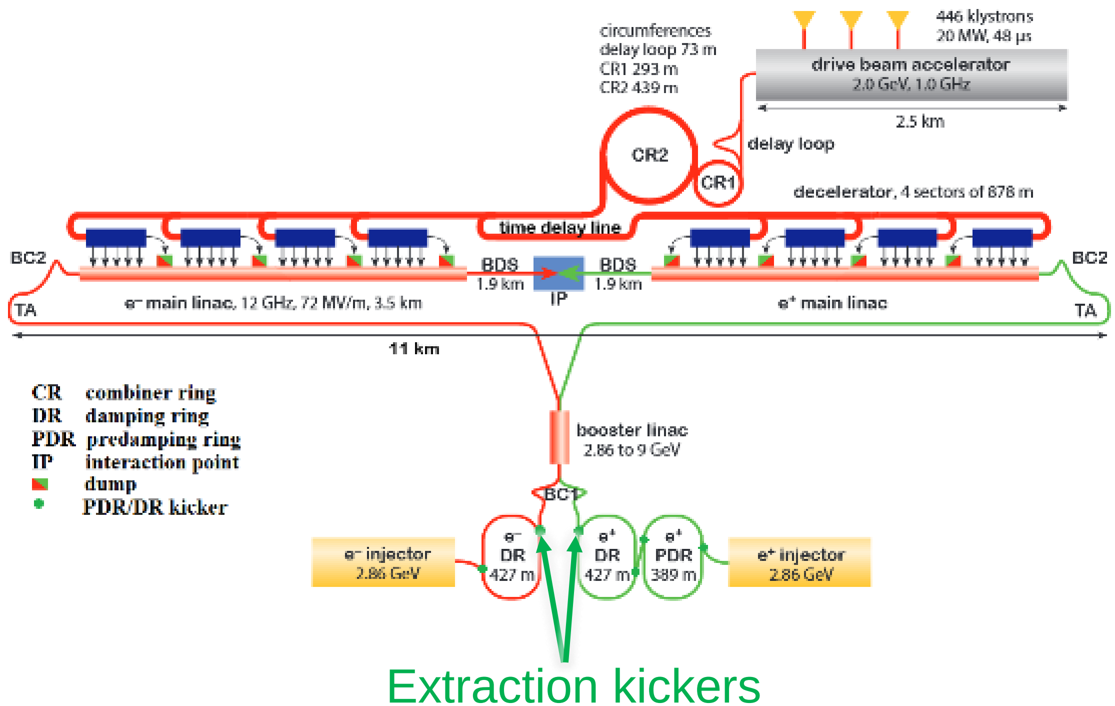
  - Measurements on Flat-top Pulse
  - Measurements on Controlled Decay Waveform for the CLIC DR Stripline Kicker.
- Summary and Future Work



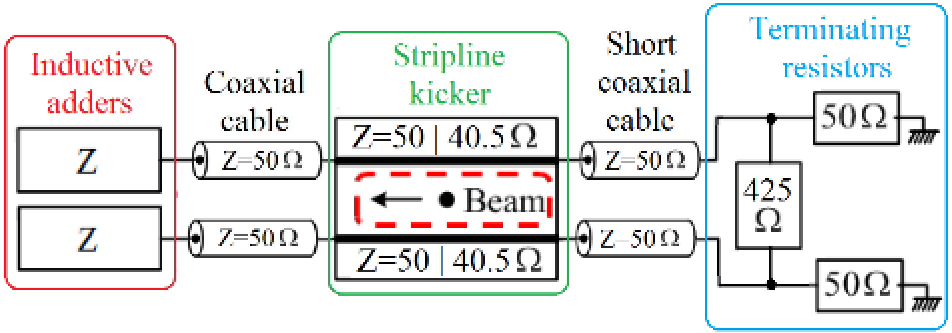
Compact Linear Collider (CLIC)

- Electron-positron collider, up to 48 km (3 TeV) long linear accelerator.
- Several stages: Injectors, Pre-Damping (**PDR**) and Damping Rings (**DR**) and main linear accelerators.
- A crucial parameter to be minimized is the beam emittance (”cross-sectional area of the beam”).
- The emittance of the beam is reduced by PDRs and DRs (synchrotrons): wiggler magnets cause particles to emit synchrotron radiation (photons) and lose energy of both transversal and longitudinal momentum components. The momentum loss is compensated by accelerating the particles (by RF cavities), which increases the longitudinal momentum. As result, the energy of the particle beam is preserved, but the emittance of the beam is decreased.
- Each bunch passes through the linear accelerator only once: any variation of the electric and/or magnetic field of the **DR extraction kicker** would cause the emittance to increase.

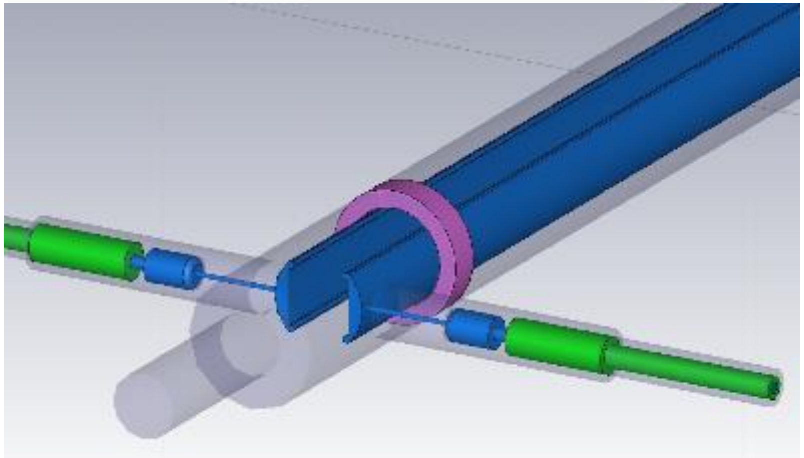


CLIC layout for 380 GeV baseline

Specifications for the CLIC DR Extraction Kicker Modulators: *Waveform* Stability & Repeatability



Simplified schematic of a CLIC DR stripline kicker system

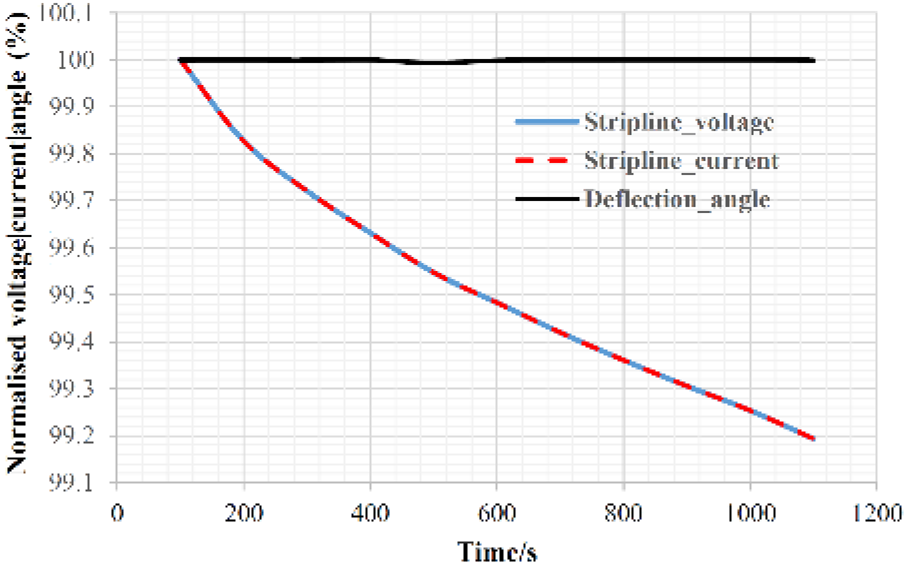


3D model of the CLIC DR stripline electrodes

- **Stripline kicker: two electrodes, powered with opposite polarities**
- **Both electric and magnetic fields deflect the beam.**
- **Impedances of the striplines are 50 *Ω* when ”off” and 40.5 *Ω* when ”on”: both modes are matched with a terminating resistor network.**
- **The total deflecting angle for particles in each bunch during a single kick should be the same.**
- **According to optimization studies of the CLIC DR prototype stripline kicker (by C. Belver-Aguilar), the impedance of the kicker does not remain unchanged during the pulse: in order to generate the same deflection for each bunch, the voltage and current need to be modulated.**
- **The optimum waveforms for two stripline electrodes are identical ”controlled decays”: these generate a constant ”flat-top” for total deflecting field.**

Specifications for the CLIC DR Extraction Kicker Modulators: *Waveform* stability & repeatability

	CLIC DR (1 GHz | 2 GHz)
Pulse voltage (per Stripline)	±12.5 kV
Stripline pulse current [40.5 Ω load]	±309 A
Repetition rate	50 Hz
Pulse waveform duration *900 ns = 160 ns + 580 ns gap + 160 ns	~160 ns | ~900* ns
Waveform repeatability	**±1x10^{-4} (±0.01 %)**
Waveform stability	**±2x10^{-4} (±0.02 %)**
Voltage rise/fall time	< 1000 ns



- The required waveform is a controlled decay.
- Definitions for waveform parameters
  - Repeatability: difference of amplitudes of any two waveforms during the pulse (160 | 900 ns)
  - Stability: difference between the optimum, simulated, waveform and a generated waveform at any time point during the pulse
- **Extremely tight requirements for waveform stability and repeatability!**
- For rise/fall times, ≤ 100 ns desired

Inductive Adder

- Many primary “layers”, each with solid-state switches
- The output voltage is approximately the sum of the voltages of the primary constant voltage layers

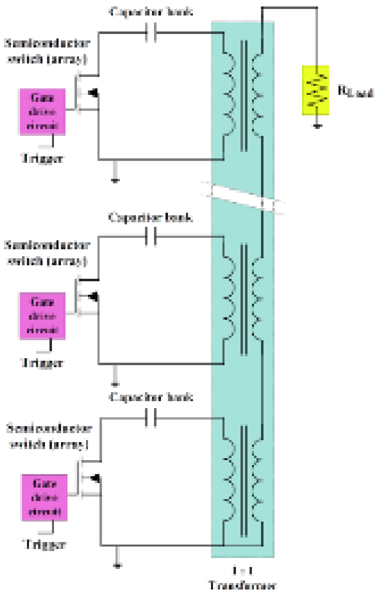
+ The output voltage can be modulated during the pulse by passive/active analogue modulation.

+ Possibility to generate positive or negative output pulses with the same adder: the polarity of the ouput pulses can be easily changed by grounding the other end of the output of the adder

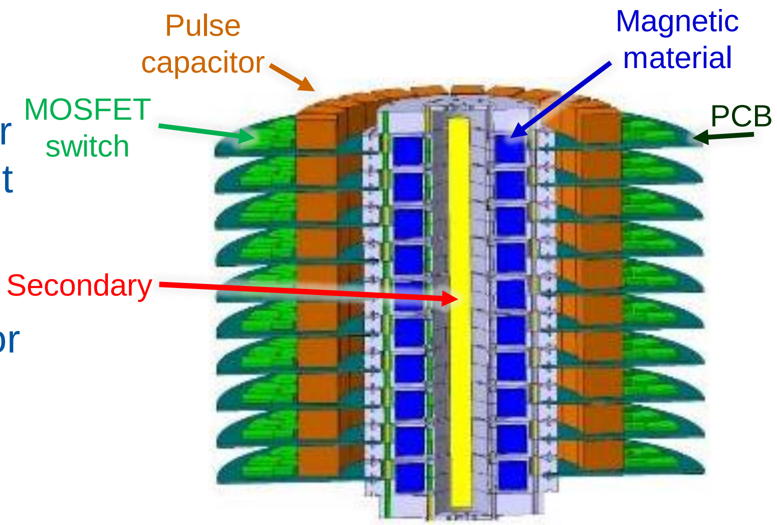
+ All control electronics referenced to ground potential.

+ Built-in fault tolerancy and redundancy: if one switch or layer fails, the adder still gives full voltage or a significant portion of the required output pulse (good for the machine safety).

+ Modularity: the same design can potentially be used for kickers with different specifications (CLIC PDR & DR kicker modulators, extraction + dump kicker

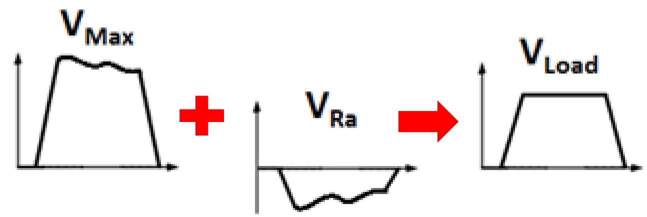


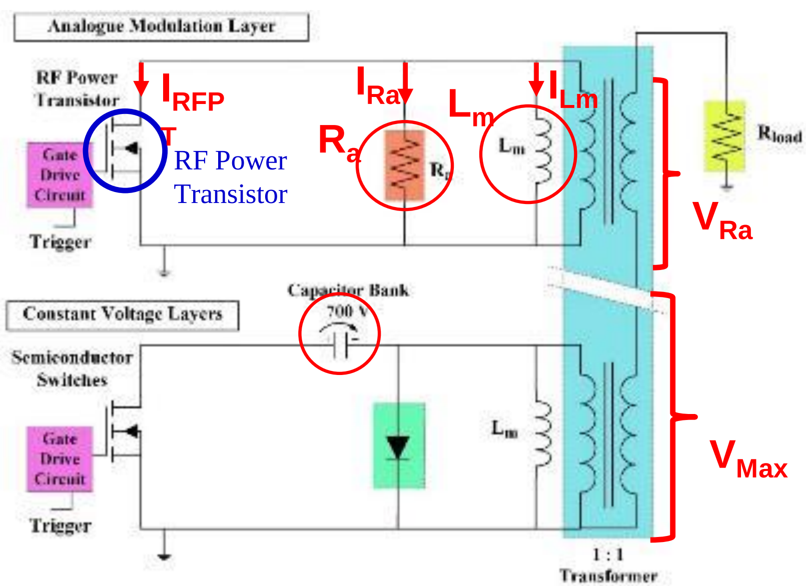
Inductive adder



Improving the Waveform Stability: Active Analogue Modulation

- Droop and ripple of the output pulse can be compensated with an active analogue modulation layer
- Operation principle: the primary of the analogue modulation layer is effectively in series with the load. The primary consists of resistor R_a in parallel with magnetizing inductance L_m and an **RF power transistor.**
- The load voltage is the sum of the voltages across all of the layers ($V_{Max} + V_{Ra}$)
- **Active mode:** The voltage across R_a, i.e. across the analogue modulation layer, can be controlled by modulating the current through the RF power transistor.
- Passive mode (RF power transistor is off): During the pulse, current through L_m increases, which causes current through R_a to decrease. Therefore, voltage over R_a decreases, which can compensate for a reduction in the primary voltage (i.e. droop) of the other layers.



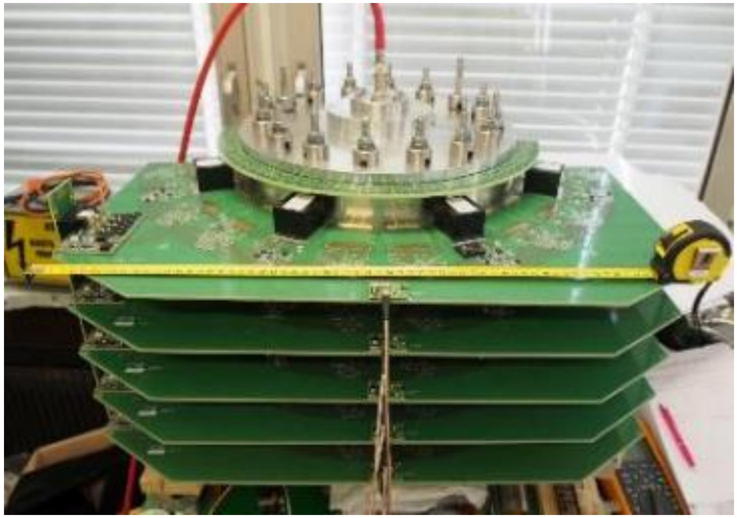


Prototypes 4&5: Full-Scale, +/-12.5 kV, 20-layer, Inductive Adders for CLIC DR Extraction Kicker System

- Specifications according to requirements for CLIC DR extraction kicker:
  - Target waveform stability ±0.02 % for 900 ns at 12.5 kV
  - Target waveform repeatability ±0.01 % for 900 ns at 12.5 kV
- Status: under testing, measurements carried out with up to 19 constant voltage layers + 1 analogue modulation layer, up to 10.5 kV

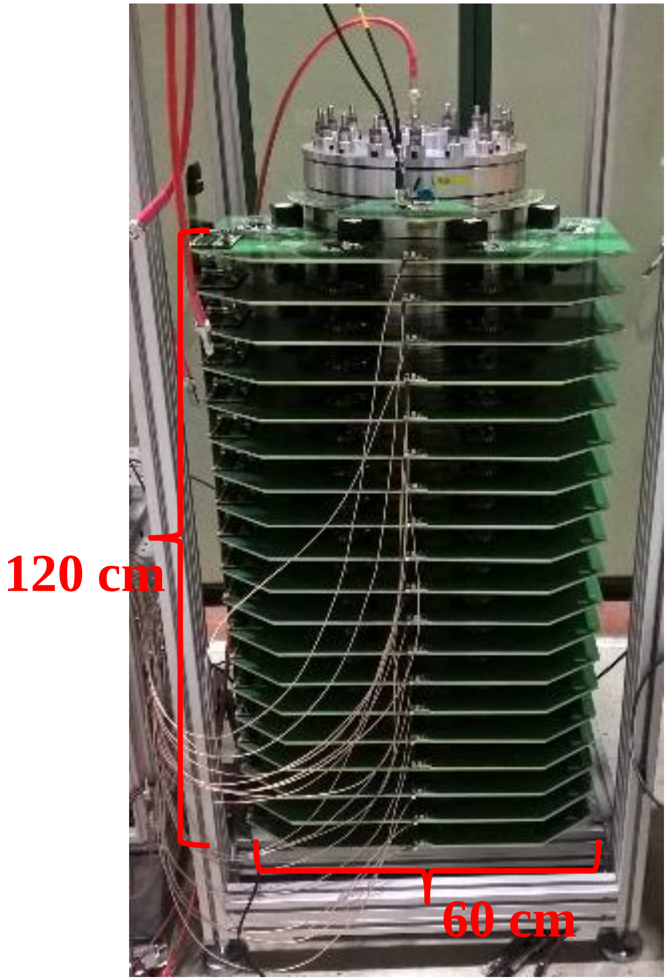
Design Parameter	20-Layer Full-Scale Prototype	CLIC DR Extraction Kicker Modulator
Output Voltage (kV)	**12.5**	12.5
Output Current	**309***	250
Voltage per layer	**700**	700
Number of layers	**20**	20
Pulse flat-top duration (ns)	**1100**	160 – 900
Pulse rise time [0.1-99.9 %] (ns)	**100**	< 1000
Pulse fall time [0.1-99.9 %] (ns)	**100**	< 1000
Flat-top stability (for 900* ns)	**≤ ±0.02 %**	±0.02 %
Flat-top repeatability (for 900* ns)	**≤ ±0.01 %**	±0.01 %

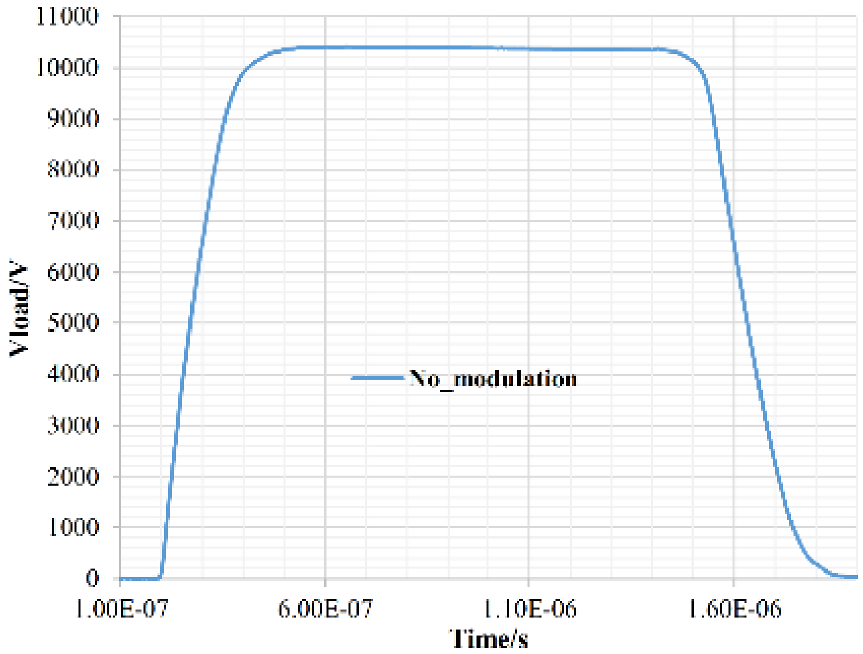
*Stripline off-mode impedance 40.5 *Ω*



First 5 layers of the 12.5 kV inductive adder assembled at CERN

Measurement without Modulation

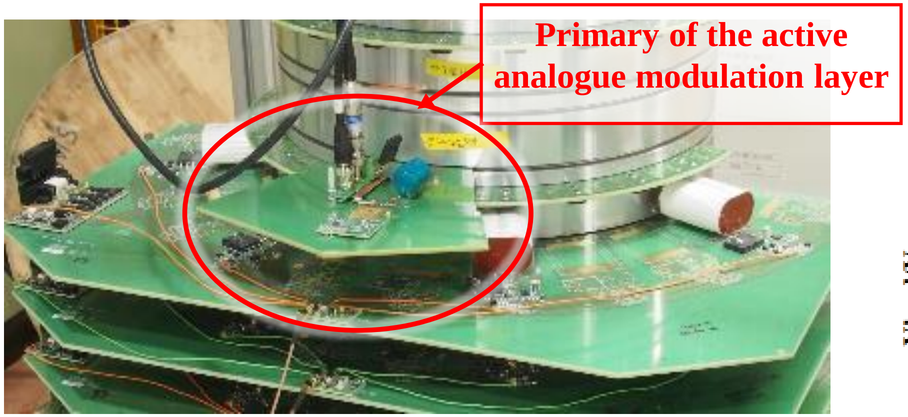




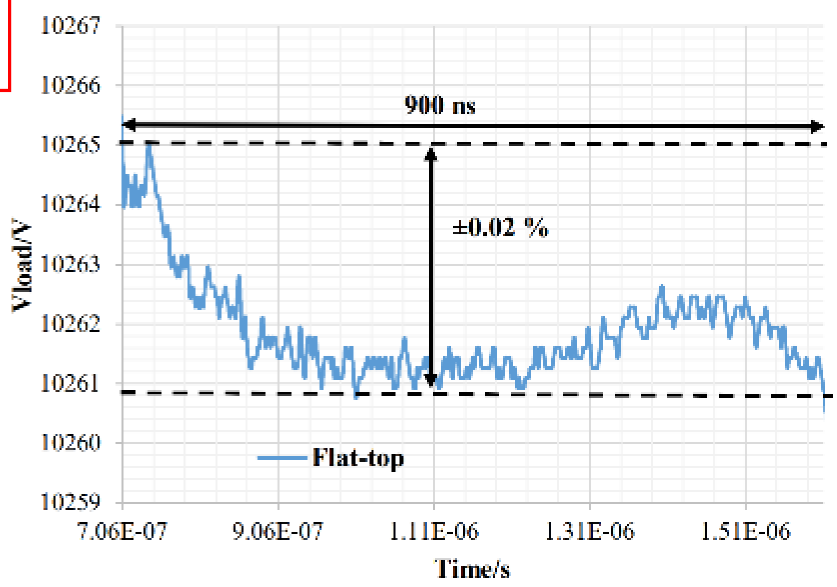
- **Setup for the measurement:**
  - 20-layer prototype inductive adder
  - 18 constant voltage layers, with half-layer PCBs
  - 4 branches powered per layer, capacitors (48 µF/layer) initially charged to 590 V.
  - **No modulation applied**
  - **Output voltage 10.4 kV, droop 60 V for 700 ns.**

⇨ Flat-top stability w/o compensation: ±0.3 % (±30 V) over 900 ns, at 10.4 kV

Measurement on a Flat-top Pulse



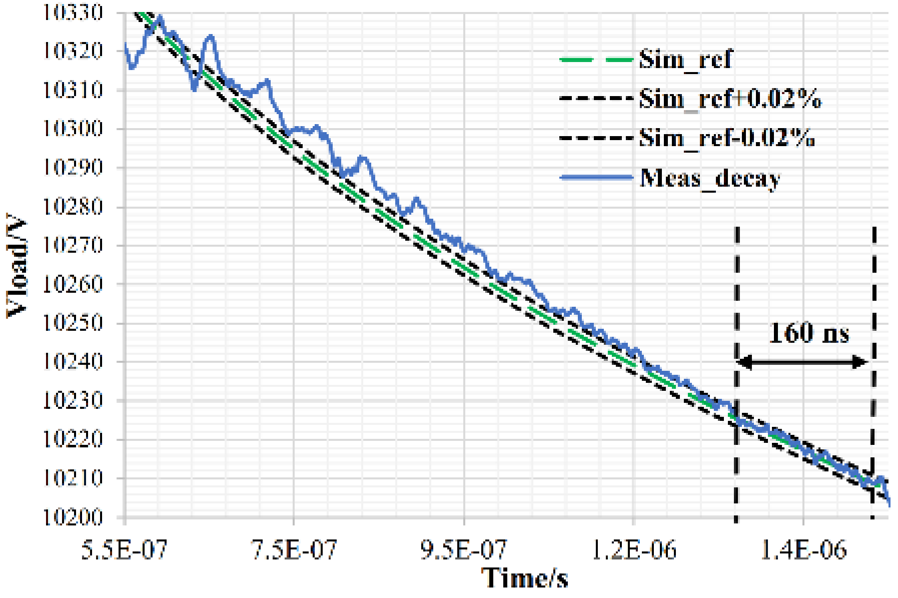
- **Setup for the measurement:**
  - 20-layer prototype inductive adder
  - 19 constant voltage layers, with half-layer PCBs
  - 4 branches powered per layer, capacitors (48 µF/layer) initially charged to 605 V.
  - **1 active analogue modulation layer**
  - **Active compensation of droop**
  - **Output voltage ~10.3 kV**



- ⇨ **Until recently, the specifications called a "flat-top" pulse.**
- ⇨ **Manually tuned compensation, not yet fully optimised: could be improved e.g. by applying frequency domain compensation, with Fast Fourier Transform analysis.**
- ⇨ **Flat-top stability: ±0.02 % (±2.2 V) over the 900 ns flat-top at 10.2 kV (for an average of 1k measured pulses).**

Measurement on an Optimum Controlled Decay Waveform

- **Setup for the measurement:**
  - 20-layer prototype inductive adder
  - 18 constant voltage layers, with half-layer PCBs
  - 4 branches powered per layer, capacitors (48 µF/layer) initially charged to 605 V.
  - **1 active analogue modulation layer**
  - **Active modulation applied to ajdust the flat-top to a controlled decay**
  - **Output voltage ~10.3 kV (decay)**

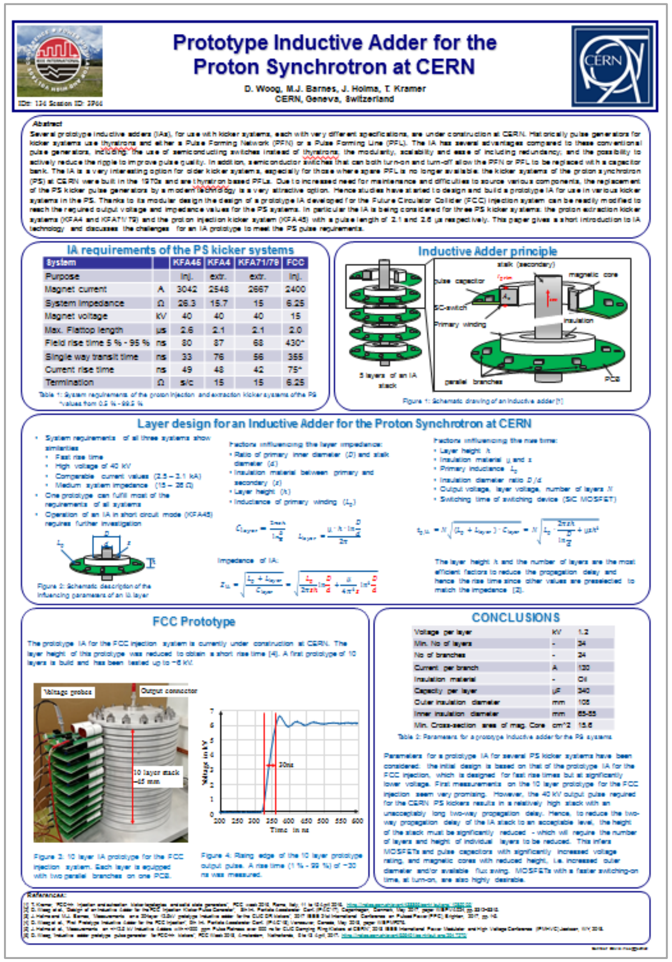


- **Waveform stability ±0.02 % over 160 ns wrt. the optimum decay waveform (according to CLIC DR kicker stability requirement) at ~10.3 kV (for an average of 100 waveforms)**
- **Manually tuned compensation, not optimised: can be improved e.g. applying frequency domain compensation, with Fast Fourier Transform analysis.**
- **Target for next measurements: stability ±0.02 % over the first and last 160 ns of a 900 ns (or over 900 ns) decay wrt. the optimum decay waveform.**

Summary & Future Work

- Two full-scale, 20-layer, +/-12.5 kV CLIC DR extraction kicker inductive adders have been built at CERN and testing is on-going.
- Active analogue modulation methods applied to a) improve the flat-top stability of the waveforms and b) to adjust the output waveform for a controlled decay waveform.
- The best measured flat-top stabilities, with active droop compensation (not fully optimised) :
  - ±0.02 % over 900 ns for a flat-top pulse at 10.3 kV.
  - ±0.02 % over the best 320 ns for a decay waveform at 10.3 kV
- Next steps
  - Measurements at 12.5 kV (nominal voltage)
  - Decay waveform measurements with ±0.02 % stability over 900 ns.
  - Measurements with two indutive adders by measuring the difference of two pulses with oppostive polarities, for stability and repeatability.
  - Design of automated control system for the waveform corrections.
  - Measurements of two 12.5 kV inductive adders with a prototype stripline kicker installed in a beamline at Alba Synchrotron Light Source in Spain (September 2018).
- Much interest for inductive adder technology at CERN, regarding e.g. FCC project and replacement of ageing systems in existing accelerators at CERN:

see poster "Prototype Inductive Adder for the Proton Synchrotron at CERN" ID: 3P44 on Wednesday



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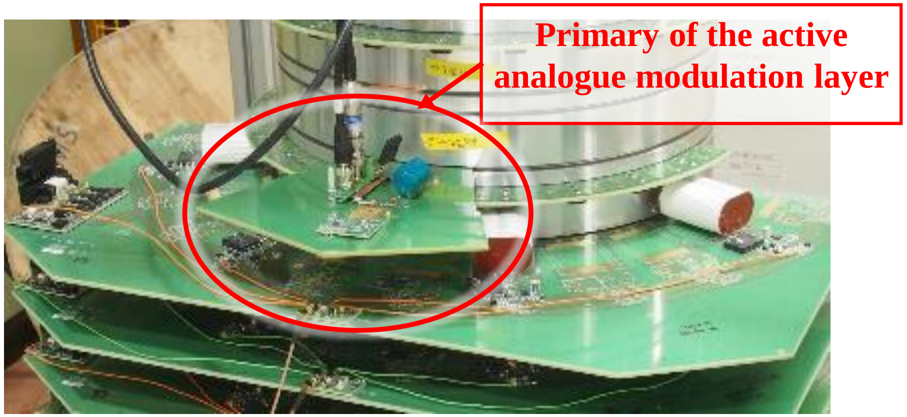
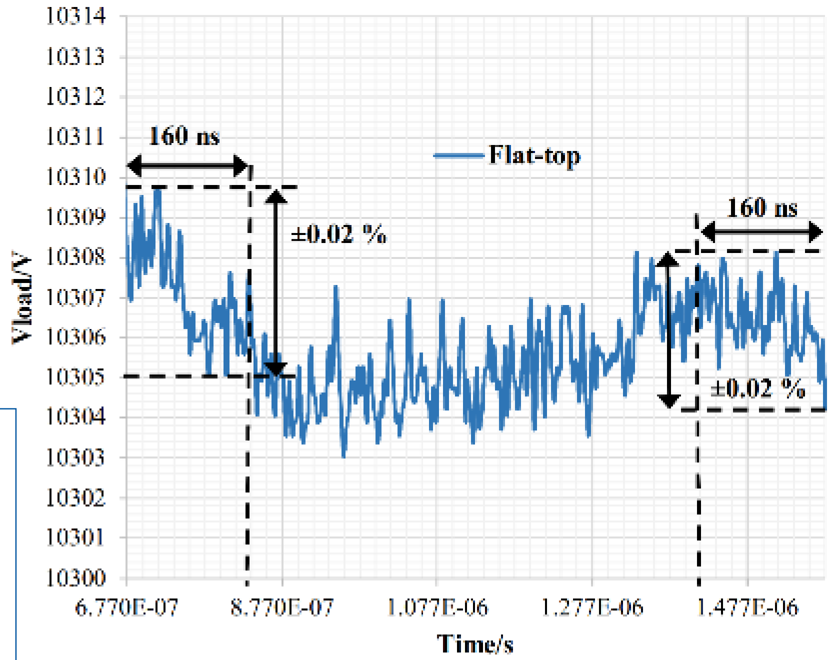
Prototype 4&5: Flat-top Pulse, with Modulation





- **Setup for the measurement:**
  - 20-layer prototype inductive adder
  - 19 constant voltage layers, with half-layer PCBs
  - 4 branches powered per layer, capacitors (48 μF/layer) initially charged to 605 V.
  - **1 active analogue modulation layer**
  - **Active compensation of droop**
  - **Output voltage 10.3 kV**

⇨ **Until recently, the specifications called a "flat-top" pulse.**

⇨ **Manually tuned compensation, not yet fully optimised: could be improved e.g. by applying frequency domain compensation, with Fast Fourier Transform analysis.**

⇨ **Flat-top stability: ±0.02 % (±2.3 V) over the first and last 160 ns of the 900 ns flat-top and ±0.03 % (±3.3 V) over 900 ns, at 10.2 kV (for an average of 100 measured pulses).**