# A Series Arc Fault Location Method for DC Distribution System Using Time Lag of Parallel Capacitor Current Pulses

Xiaojun Liu, Qing Xiong, Shengchang Ji, Lingyu Zhu, Lu Gao, Zhitong Jiang

State Key Laboratory of Electrical Insulation and Power Equipment, Xi'an Jiaotong University, Xi'an 710049, China

## I. INTRODUCTION

- With DC series arc fault detection method developing, arc fault can be detected and switched at the initial arcing time. The way by artificial patrol to locate arc fault is more difficult with no obvious arcing trace. So it's necessary to propose an accurate location method avoiding high service cost.
- Although there are lots of studies about DC arc location method, most of these location method concentrate on determining the arcing circuit branch and fail in determining the accurate arc location.
- Based on time lag of parallel capacitive current, a series arc fault location method is proposed. And series arc fault can be accurately located and the largest location error is less than 10m.

## II. DC ARC TEST PLATFORM

- The structure of arc generator is shown in Fig. 1. Controlled by step motor, arc is generated between the movable electrode and the fixed electrode. DC series arc generator is series in the circuit at different location indicating different arc fault location.
- The supply is a DC source and output is from 0V to 360V.
- Rogowski coils(100Hz-1000kHz) are utilized to measure the high frequency current through capactor.
- The DC arc fault test platform diagram with two test scenarios is shown in Fig. 2.
  - In single line test scenario, two capacitors(C1 and C2)with 100nF are paralleled at both two ends of the single line, as shown in Fig. 2.a.
  - In double lines test scenario, C1 is paralleled with the supply, C2 and C3 are respectively paralleled at different lines end, as shown in Fig. 2.b.
- The two-cores cable is 300 meters long.
- A 41Ω resistor (R1 and R2) is set as the load.

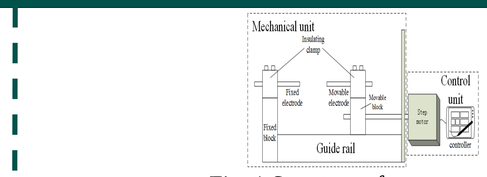
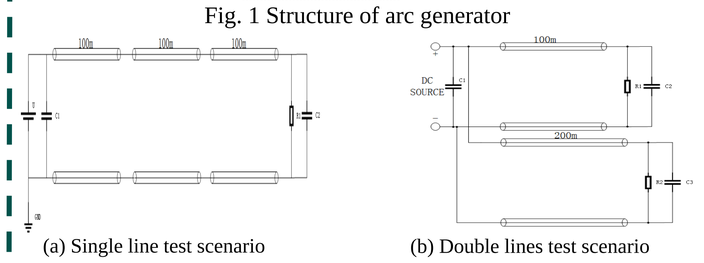



Fig. 1 Structure of arc generator




(a) Single line test scenario (b) Double lines test scenario

Fig. 2 DC arc test platform diagram

## III. ARC FAULT LOCATION METHOD

- A. Arc Fault Location Method
  - When series DC arc fault occurs in circuit, high frequency characteristic current flows through the two capacitors with a time lag.
  - Arc fault location method by use of time lag(between t1 and t2) is shown in Fig. 3.

$$\begin{cases} s=t_1\cdot v+t_2\cdot v \\ l=t_1\cdot v \end{cases} \qquad l=\frac{s-(t_2-t_1)\cdot v}{2}$$

$s$: length of the whole line (m)；$l$: distance from arc fault to the line beginning (m)；$t_1$: time from arc fault to the line beginning (s)；$t_2$: time from arc fault to the line end (s)；$v$: wave velocity (m/s)

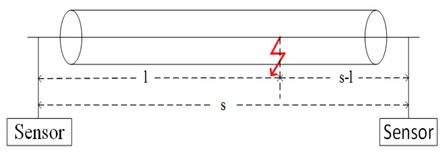



Fig.3 Principle of double-ended traveling wave

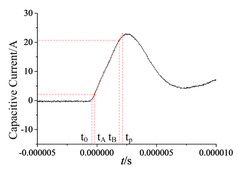


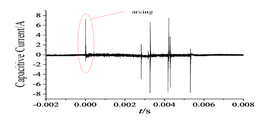

Fig. 4 Arriving time of capacitive current

- B. Arriving Time Estimation
  - The arriving high frequency pulse has a short width and a high amplitude as shown in Fig. 4.
  - Low change rate at pulse beginning and ending has an interference to compute the arriving time.
  - Apparent zero-point t0 and apparent peak-point tp is proposed to compute the arriving time of pulse and time lag to locate arc fault.

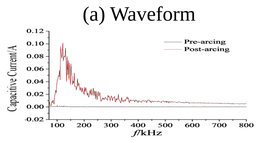
$$t_0=1.125t_A-0.125t_B$$
$$t_p=1.125t_B-0.125t_A$$
$$t=t_p-t_0$$

## IV. TEST RESULT

- A. time-frequency characteristics of series arc in cable line
  - Waveform and spectrum of capacitive current with arcing are shown in Fig. 5.
  - The amplitude of capacitive current has an obvious change when arc occurs.
  - In frequency domain, the amplitude of 100-300 kHz high frequency capacitive current between pre-arcing and post-arcing change a lot.




(a) Waveform




(b) Spectrums of Pre- and Post-arcing

Fig. 5 Waveform and spectrums of capacitive current

- B. Wave velocity
  - Travelling wave would reflect at the impendence-changing joint, as shown in Fig. 6.
  - A 5V square wave is injected into a 300m cable with no load at cable end.
  - Time lag from the square wave injected into cable beginning to the injected wave arriving at the same location is measured as 4.76 ms. And wave velocity in cable is $1.26\cdot10^8$ m/s.

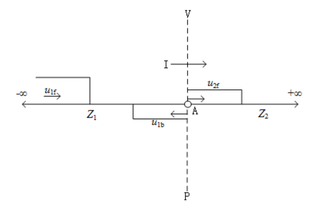



Fig. 6 Reflection of travelling wave

- C. single-line test scenario
  - In this scenario, series DC arc fault is set at five locations, as shown in Fig. 7.
  - When series arc fault occurs at different five locations, the current through two capacitors is shown in Fig. 8.By measuring the arriving time, time of an apparent zero point can be computed. In addition, time lag between two different arriving apparent zero point and location of arc fault by this method are computed, as showed in Table 1.
  - the fault can be accurately located, and the largest positioning error does not exceed 4% and is less than 10m.

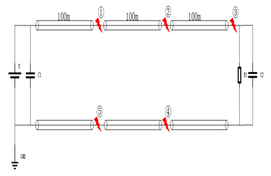
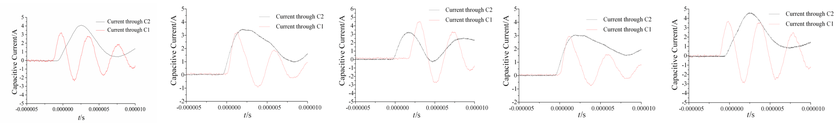



Fig. 7 Arc locations in single line




(a)C1&C2 current at location 1 (b)C1&C2 current at location 2 (c)C1&C2 current at location 3 (d)C1&C2 current at location 4 (e)C1&C2 current at location 5

Fig. 8 Capacitive current at different arc locations in single line test scenario

Table.1 Test result at different arc locations in single line

| | $t_1$/μs | $t_2$/μs | $(t_2-t_1)$/μs | l/m | Δl/l |
|---|---|---|---|---|---|
| Location 1 | -1.3438 | -0.5715 | 0.7723 | 97.48 | 2.52% |
| Location 2 | 0.2113 | -0.4346 | -0.6459 | 193.92 | 3.04% |
| Location 3 | 1.7775 | -0.3771 | -2.1546 | 296.51 | 1.16% |
| Location 4 | 0.1368 | -0.4888 | -0.6256 | 192.54 | 3.73% |
| Location 5 | -1.1650 | -0.3988 | 0.7663 | 97.89 | 2.11% |

- D. double lines test scenario
  - In this scenario, series DC arc fault is set at four locations, as shown in Fig. 9.
  - When series arc fault occurs at different four locations, the current through capacitors is shown in Fig. 10, the time lag between two different arriving apparent zero points and the computed location are shown in Table 2.
  - One line have no interference to the location at the other. Using the arriving time lag between the apparent time of current pulse through C1 and C2, the arc fault at line 1 can be located. And the arc fault at line 2 can be located by the arriving time lag between the apparent time of current pulse through C1 and C3. By this location method, the largest location error is less than 10m.

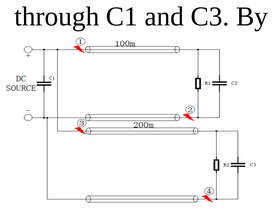
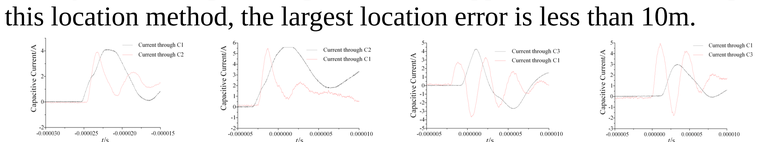



Fig. 9 Arc locations in double lines




(a)C1&C2 current at location 1 (b)C1&C2 current at location 2 (c)C1&C3 current at location 3 (d)C1&C3 current at location 4

Fig. 10 Capacitive current at different arc fault locations in double line test scenario

Table.1 Test result at different arc locations in single line

| | Δt/μs | l/m | Δl/l |
|---|---|---|---|
| Location 1 | 0.7480 | 2.88 | 2.88% |
| Location 2 | -0.7500 | 97.25 | 2.75% |
| Location 3 | 1.5137 | 4.64 | 2.32% |
| Location 4 | 1.4562 | 191.74 | 4.13% |

## V. CONCLUSION

- Capacitors paralleled to couple the high frequency arc current can obviously avoid the reference from normal DC current.
- The frequency band of capacitor current with arcing in cable line is from 100 – 300 kHz.
- Both in single line system and multiline system, the largest location occur is less than 10m and arc fault occurring at line 1 won't be interfered by another line, indicating that arc fault can be accurately located by use of this method.

Author email: Lxj951011@163.com

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