Development, Implementation and Final Performance of the New PS Booster Distributor Generators

(PFN, 6.3kV/1kA) with Fast Protection System

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LHC Injectors Upgrade

Abstract

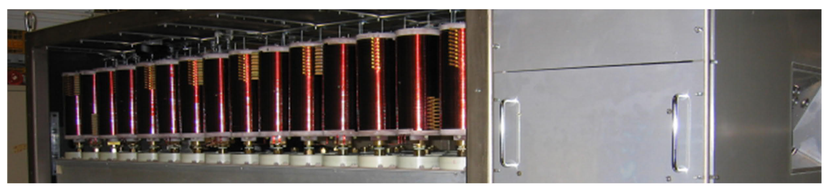
The LHC Injector Upgrade project aims at increasing the performance of the LHC injectors and includes the replacement of Linac2 by Linac4 as injector to the Proton Synchrotron Booster (PSB). In order to distribute the 160 MeV beam from Linac4 to the four rings of the PSB, a new distributor system has been built. The required five pulse generators have a pulse length ranging from 20 µs to 620 µs with a rise time of less than 2 µs and a maximum flattop ripple of ±1 %. Four generators distribute the beam to the four vertically stacked PSB rings whilst the fifth generator dumps the beam tail. The basic generator hardware consists of a Pulse Forming Network (PFN), two series connected IGBT switches, an optical trigger interface and a Fast Interlocks System (FIS) for hardware protection. During the iterative development phase, solutions to fulfil the required performance relating to rise time, jitter, long-term stability and reliability have been implemented and will be presented. The different failure modes of the generator have been studied, identified and mitigated, mostly by means of the FIS. The FIS is integrated into a larger control system infrastructure via an Ethernet backbone and industrial bus (Profinet). The industrial bus manages all PLC controllers for slow supervision of ancillary systems and remote control systems from the operating room. The process of the final tuning and the reached performance are outlined. This paper presents the development phases of the generator, the hardware protection system, the final design choices and its performance.

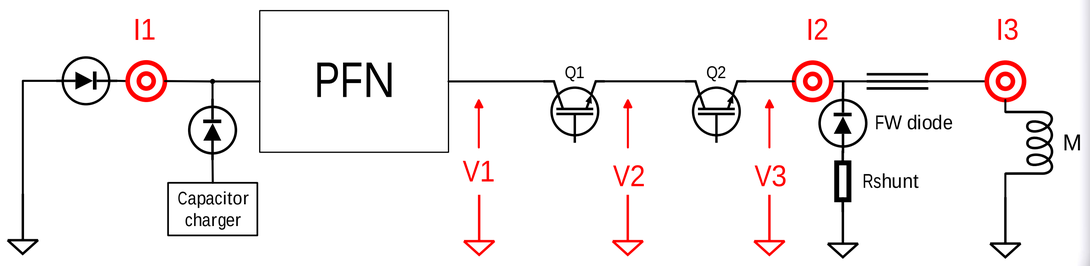
Introduction

Each of the five distributor subsystems consist of the generator, the magnet, the capacitor charger, the Fast Interlocks System (FIS) and the slow controls.

Nominal current	1 kA
Nominal voltage	6.3 kV
Charateristic impedance	~6.25 Ω
Pulse length (max.)	630 µs
Flattop ripple (max.)	± 0.5 %
Repetition rate (max.)	1.1 Hz
Number of cells (max.)	60
Cell capacitance	1 µF
Cell inductance (max.)	38 µH
Rise time (1-99% max.)	2 µs
Integrated field	9.5 mT·m
Cabinet dimensions in mm	2516 x 890 x 2060

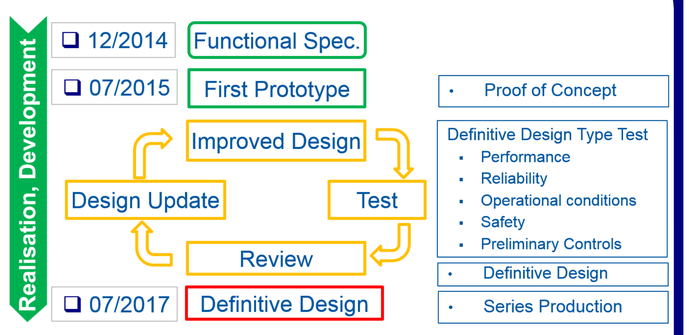
Distributor Generator





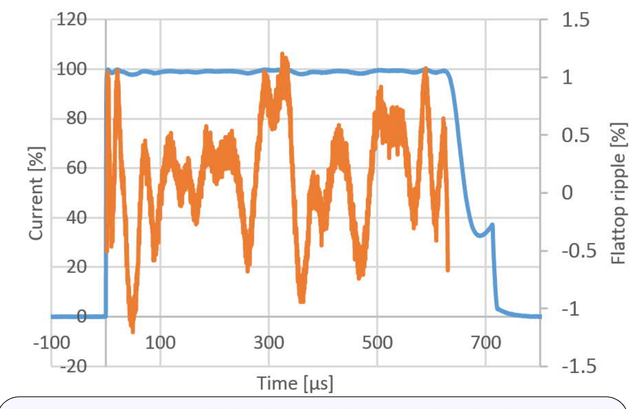
PFN system with magnet M, IGBTs Q, current transformers I, HV dividers V.

Development Phases



A simple test setup was used with old inductors from an operational PFN to verify the IGBT switching speed and proof the concept. After initial tests the first prototype was built and operated by simple pulse generators and an old PS protection system. The design was improved during the iterative testing phase until a robust one was found. After the successful long-term type test with all the changes in place the series production was started with this definitive design. Each generator was checked, tuned and tested.

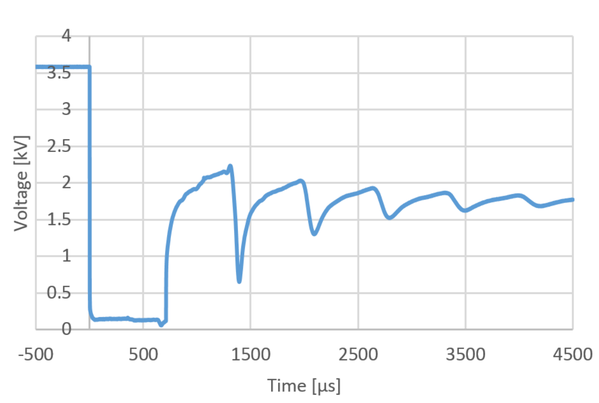
Generator

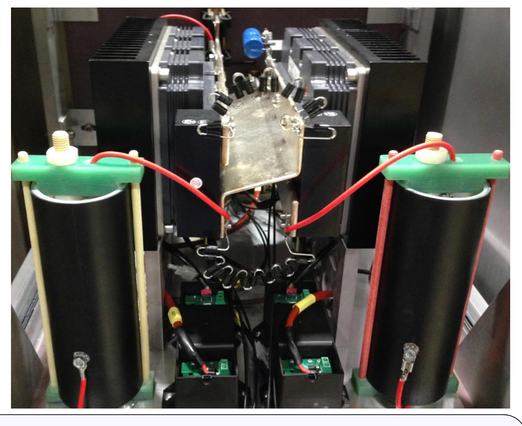


Magnet current (blue) and flattop ripple (orange).

- Maximum pulse length: 630 µs
- 60 cells of 1 µF adj. max 38 µH.
- Front cell: ~76 µH, 2 µF, 6 Ω.
- Nominal: 1 kA, 6.3 kV, max. 1.1 Hz.
- Adjusted to a flattop ripple of± 1 %
- During long shut down 2, fine tuning to ± 0.5 %.

The inductors can be roughly adjusted by taps and fine-tuned by means of two movable inner eddy current screens.
An energy recuperation diode recuperates approximately 50 % of the PFN initial voltage. The main switch of the generator consists of two series connected IGBTs. A specific trigger sequence of two trigger signals is needed for this switch assembly to optimize the voltage balance between both transistors. The voltage balance is monitored and, in case of problem, is actively controlled by the hardware protection system.





High side IGBT voltage measured with internal HV divider in the front.

Improvements during Iterative Testing

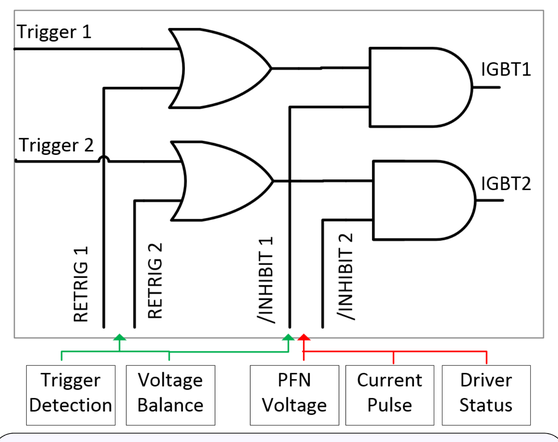
Change	Improvement
Increased copper cross-section of inductors and interconnections	Reduced heating, stable current flattop
Insertion losses of the optic fibers reduced by 3 dB	Reduced jitter on IGBTs
Parallel branches of filter resistors increased from 4 to 8	Reduced heating, reduced resistance drift, stable overshoot
Operational amplifiers and optic fiber trigger cards moved into PFN cabinet	Reduced losses, jitter and improved signal quality
Improved internal PFN auxiliary cable rooting	Reduced EMC issues
Change of auxiliary Power Supply for IGBT driver	Reliability
Increased accuracy and stability of V1, V2, V3	Reliability, IGBT protection

PFN Tuning

With the experience of the prototype, the approximate cell inductance and the corresponding tap connection was already known and pre-set for the series. The first rough inductance readjustments have been done by changing the tap position. For the fine-tuning the generator was continuously pulsed at 1 kV. The inductance was changed by repositioning the inner inductor eddy current screens during pulsing. This allowed a direct feedback on the oscilloscope and a precise and time efficient tuning.

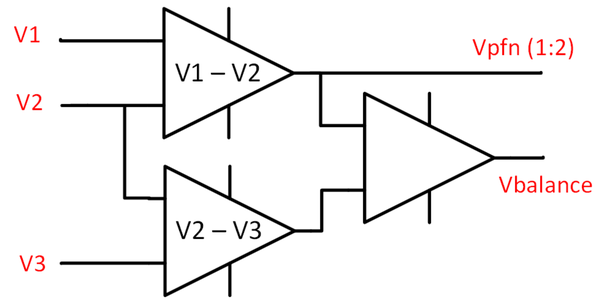
Failure Modes of the Generator

The different failure modes of the generator have been studied, most importantly: short circuit, open circuit, IGBT fault, wrong triggering, and wrong pulse parameters. Mitigation measures have been implemented mostly by means of the FIS and by hardware design.



Trigger module with fault detection modules

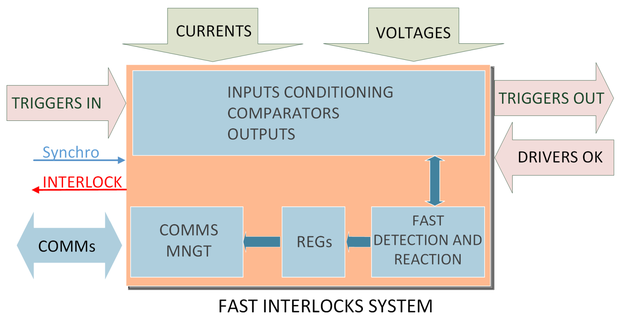
The FIS does not only passively protect by monitoring the voltage imbalances across the IGBTs but also checks for the correct trigger sequence and blocks or regenerates triggers.



Voltage tracking and imbalance detection

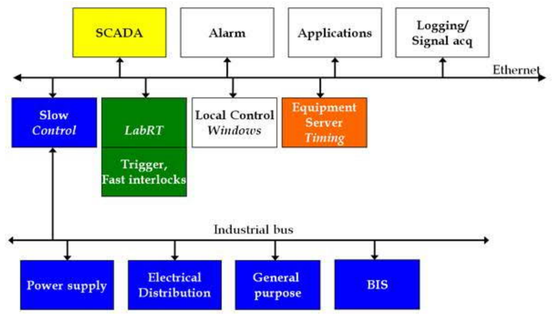
For fast reaction time the voltage across each IGBT is determined by analogue subtraction of the measured voltages. A comparator evaluates the imbalance. In case of too high imbalance, the FIS will take the required actions depending on the actual state of the generator (switch on, during the pulse, switch off, before the pulse).

Hardware Protection System



- Protect generator hardware from damage: degradation, failure, wrong operation.
- Detection and correction of failures.
- Fast reaction times.
- Signals: conditioned by operational amplifiers, evaluated by comparators.
- FPGA with cycle time of 10 ns

System General Controls



- Housed into 9 racks
- Local power distribution unit
- User interface (SCADA)
- Slow control management
- Finite state machine
- Alarms for critical sub-systems
- Beam Interlock System

Conclusion

The development phases of the system has been described. The advantages of a prototype together with an intensive testing phase has been shown by pointing out some of the major changes and improvements applied before the series production. The failure modes and their mitigation measures by combinational and low level implementation has been shown. The final system parameters reached in the laboratory have been stated.