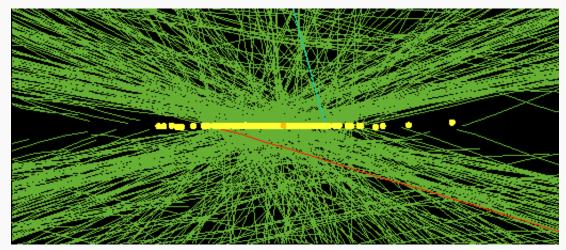
Calorimeter trigger for CMS phase-2

Cécile Caillol University of Wisconsin-Madison

Triggering on new physics at the HL-LHC, workshop at Princeton University

Physics motivation

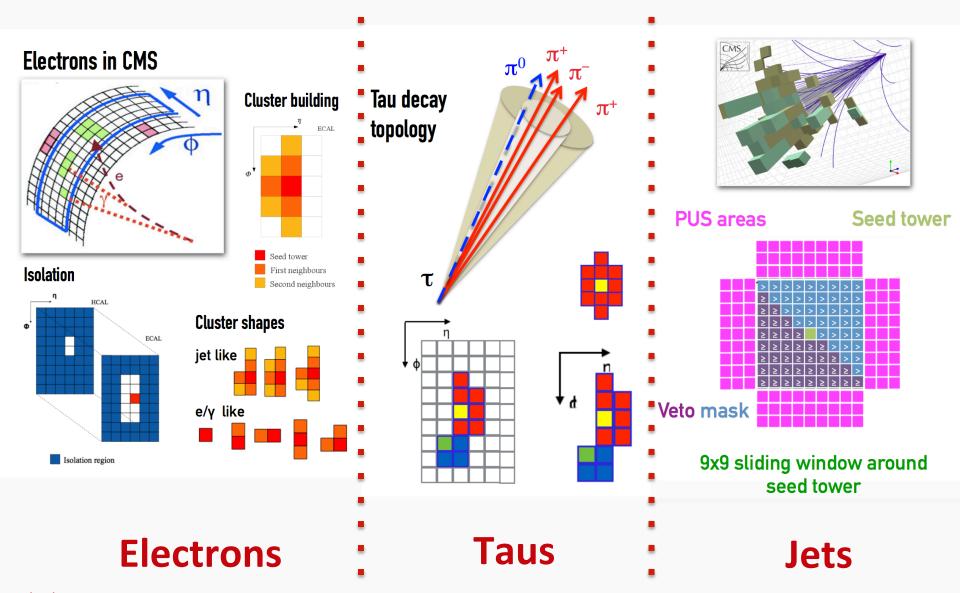
- Events with low p_T objects should be recorded to keep sensitivity to electroweak physics:
 - − Higgs sector: $H \rightarrow \tau \tau$, $H \rightarrow ZZ \rightarrow 4I$, $H \rightarrow BSM \rightarrow SM$, ...
 - W and Z physics: precision measurements
 - **–** ...
- But major challenges in phase-2:
 - High luminosity
 - High pileup (140-200)



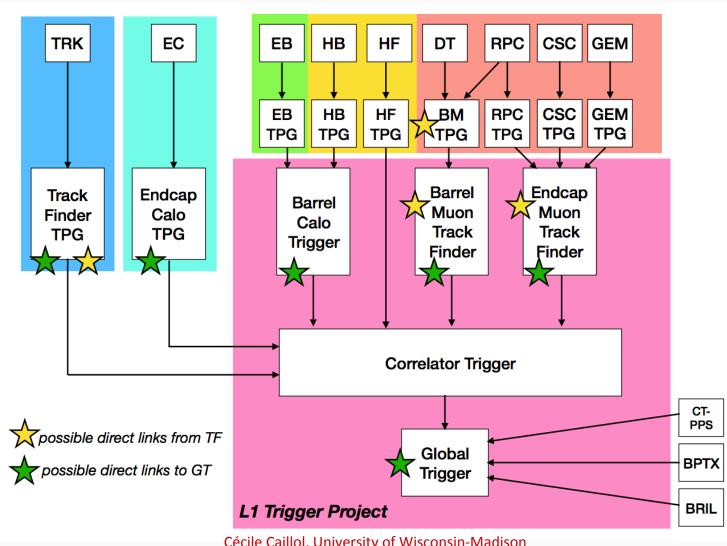
Trigger upgrades

- Significant upgrades are needed to keep similar trigger thresholds as in phase-1
- Upgrades should aim at reaching offline reconstruction performance at the L1 trigger level. This would lead to:
 - Increase of the reconstruction efficiency
 - Sharpening of the trigger efficiency turn-on
 - Decrease of the background rates
- Reaching offline reconstruction performance involves:
 - Using track information from track trigger
 - Increasing calorimeter trigger granularity

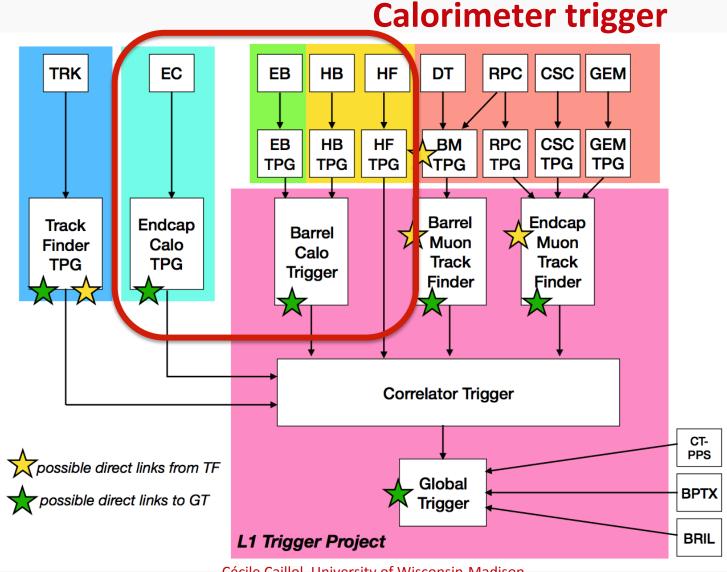
Object signature – Phase-1 algorithms



Phase-2 L1 overview

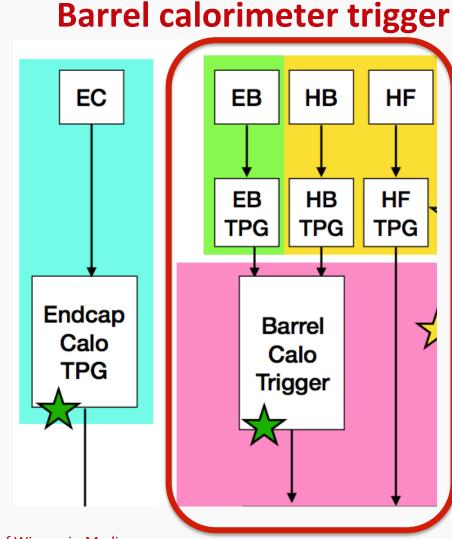


L1 overview



Calorimeter trigger - Barrel

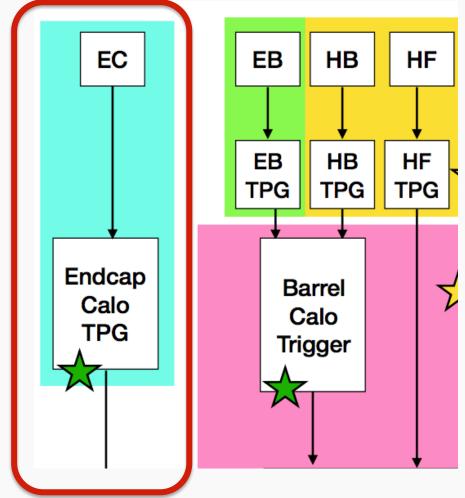
- Essentially same structure as for phase-1 upgrade
- ECAL barrel (EB): increase of transverse granularity (unit size 25 times smaller than in phase-1)
- HCAL barrel (HB)
- HCAL forward (HF)



Calorimeter trigger - Endcap

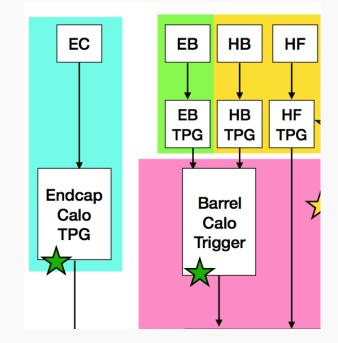
- Completely new 3D structure
- High granularity sampling calorimeter
- Time-multiplexed architecture

Endcap calorimeter trigger



Phase-2 calorimeter trigger

- Tiled multilayer architecture:
 - Layer-1 (regional): Crates assigned to particular regions receive information from different subdetectors
 - Layer-2 (global): The information from the different regions is combined
- Xilinx FPGA package C2104 (max 104 optical links)

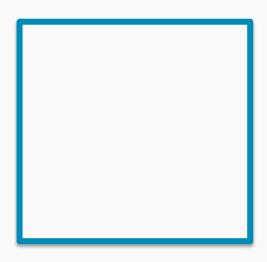


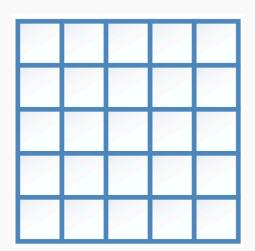
 Calorimeter objects can then be matched to tracks from the track trigger

EB - ECAL barrel

• **Phase-1**: 1 trigger tower with dimension 0.085 x 0.085

- **Phase-2**: the ECAL units are crystals (crystal dimension: 0.0175 x 0.0175), and 5x5 crystals are covered by a front-end card
- Increase of granularity → better position and energy resolution, better shape distinction between signal and backgrounds, better matching to tracks





EB – Trigger primitives

- Two possibilities:
 - Send single crystal information
 - Cluster crystals and send information about clusters

•	Crystal	primitive	(baseline)):
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- 16 bits: E_T (10), time (5), spike flag (1)

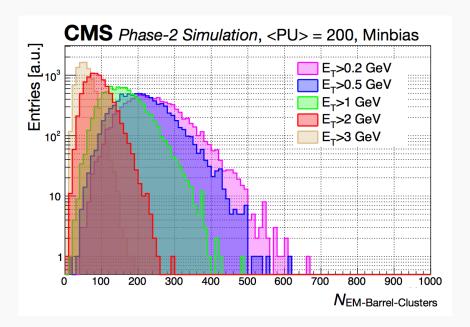
Quantity	N bits
$E_{ m T}$	10
Time	5
Spike flag	1
Total	16

- Cluster primitive:
 - Example with 40 bits: Also includes the position of the cluster and the number of crystals in the cluster
- Primitives sent to correlator of global trigger
- Trigger primitive generator entirely located in back-end electronics (for phase-1: on-detector electronics)

Quantity	N bits
$E_{ m T}$	10
Time	5
η	8
$ \phi$	8
$N_{ m crystal}$	8
Spike flag	1
Total	40

EB – Cluster primitive

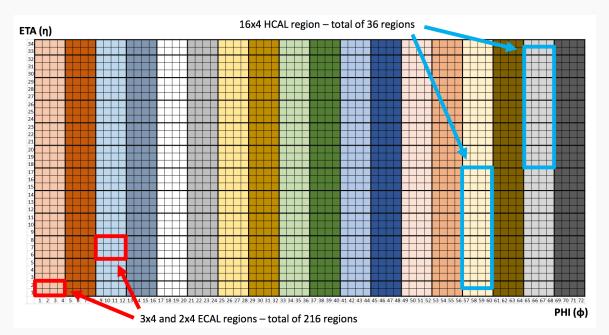
- Not the preferred solution, only if processing or bandwidth becomes constrained
- Capacity to transmit of order 1000 clusters per bunch to limit truncation effects to 10^{-4} (for PU = 200)



• A 16-bit word that sums the crystal energy within a region of 25×25 crystals should be sent to account for unclustered energy.

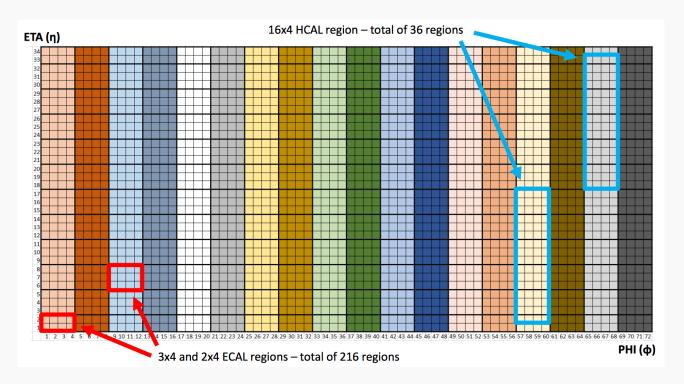
EB – Region definition

- Each front-end card collects data from a 5 × 5 array of crystals at 160 MHz
- 12 such cards send data to a single back end-card, via 48 upstream links and 12 downstream links
- Each back-end card covers 300 crystals ($\eta \times \varphi = 0.26 \times 0.35$)
- 216 back-end cards (in 18 crates) cover the ECAL barrel



Hadron Barrel (HB)

- Back-end divided in $16\eta \times 4\varphi$ regions and tower level energies are sent out with 16Gbps links at 16bit/tower.
- Total of 36 regions, each processed by a single FPGA.



Hadron Barrel (HB)

- Back-end divided in $16\eta \times 4\varphi$ regions and tower level energies are sent out with 16Gbps links at 16bit/tower.
- Total of 36 regions, each processed by a single FPGA.

- Same hardware as developed for EB
- The Phase-2 upgrade of the HB calorimeter replaces the back-end electronics, and partially replaces a few front layer scintillator tiles

Hadron forward (HF)

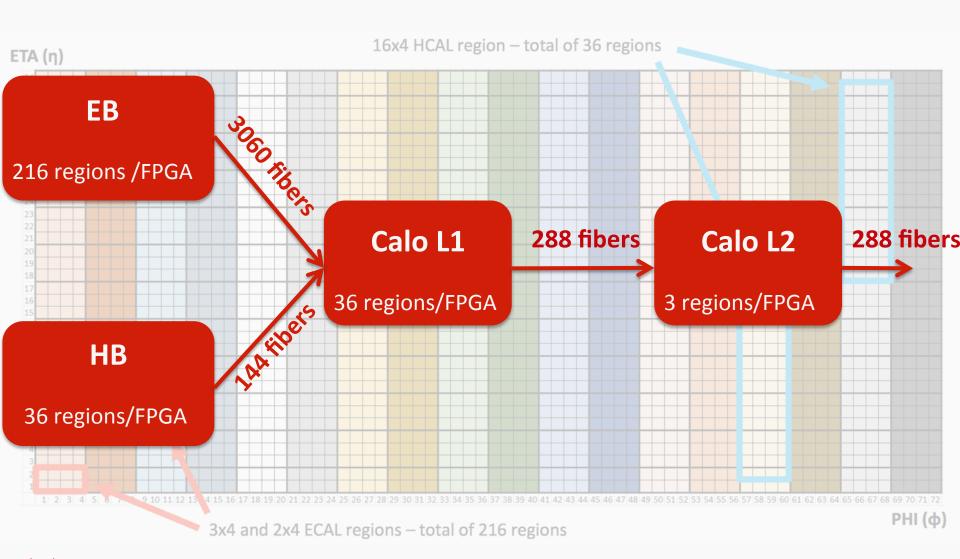
- The HF detector will continue to operate with the Phase-1 front-end and back-end electronics.
- Phase-1 HB and HE back-end cards will be reused to increase HF back-end to sustain the rates expected in phase-2

HB and HF – Trigger primitive

- HB units are trigger towers of 0.0875 x 0.0875 (25 times bigger than the EB units)
- HB trigger primitives correspond to these trigger towers, with 16 bits

Quantity	N bits (HB)	N bits (HF)
$E_{ m T}$	10	8
Feature bits	6	2
Total	16	10

Recap - Barrel calorimeter layout



High-granularity endcap calorimeter (EC)

- Completely new high granularity sampling calorimeter, using silicon and scintillators as sensitive elements
- 52 sensitive layers (28 in ECAL and 24 in HCAL)
- Trigger cells correspond to 4 cm² in the silicon regions
- 3D high granularity makes PF algorithm possible at L1
- Dimensions of the trigger towers: 0.0875 x 0.0875, same as in the barrel

EC – Trigger primitives

- 1. Form 2D clusters from trigger cells in a single layer, and sum tower data into a single η , φ grid
- 2. Combine the 2D clusters in depth to form 3D clusters, and combine all the single-layer tower map data with an appropriate weighting into the complete transverse energy tower map.
- The completed tower maps and 3D clusters form the ECT primitives that are transmitted to the L1 trigger.
- Time-multiplexing to transfer all the 2D clusters and tower maps for a single bunch crossing into one FPGA, feasible in 4µs

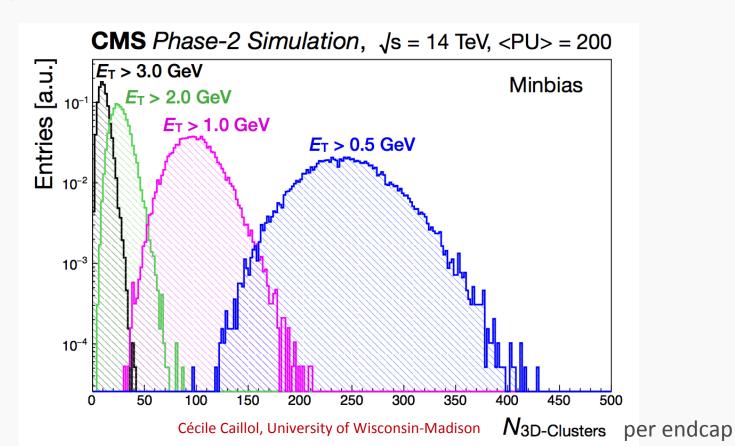
EC – Trigger pimitives

 Typical size of a 3D cluster should be around 200 bits (minimum 128 bits)

Quantity	N bits	Comment
$E_{ m T}$	2 × 16	with and without PU subtraction
Endcap	1	
$\mid f_{ ext{EE}} \mid$	13	E_{T} fraction in EE
f_{BH}	12	$E_{\rm T}$ fraction in BH
L_{max}	6	Max energy layer
$\mid \eta \mid$	11	Shower start
ϕ	11	Shower start
z	10	Shower start
$N_{ m cells}$	8	
Quality	12	
Extra flags	12	
Minimum total	128	

EC – Trigger primitives

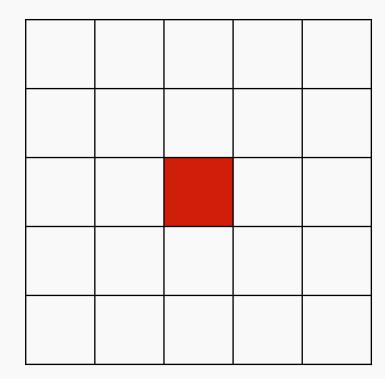
- E_⊤ threshold needed to reduce bandwidth
- Threshold such that clusters can be matched to tracks (2-3 GeV) \rightarrow ~1 GeV
- Bandwidth of 80 kb per bunch crossing, corresponding to 200 clusters per endcap, needed for this threshold



Trigger algorithm – Electron example

- Algorithm developed for EB
- Electron identification at L1 strongly based on calorimeter trigger
- Rate reduced by matching calo objects to tracks

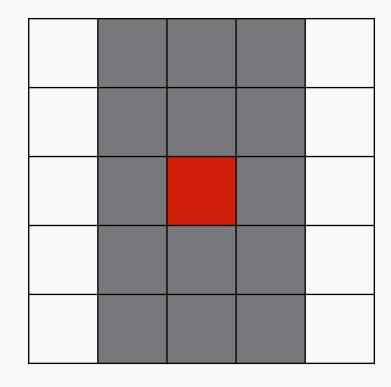
Seed crystal with E_T > 1 GeV



Trigger algorithm – Electron example

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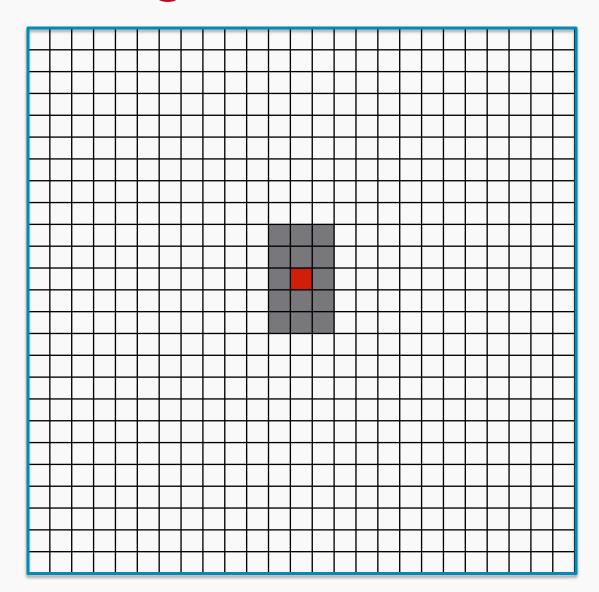
Seed crystal with E_T > 1 GeV



Cluster energy in 3x5 crystals around the seed

Position of the cluster determined from energy-weighted crystals

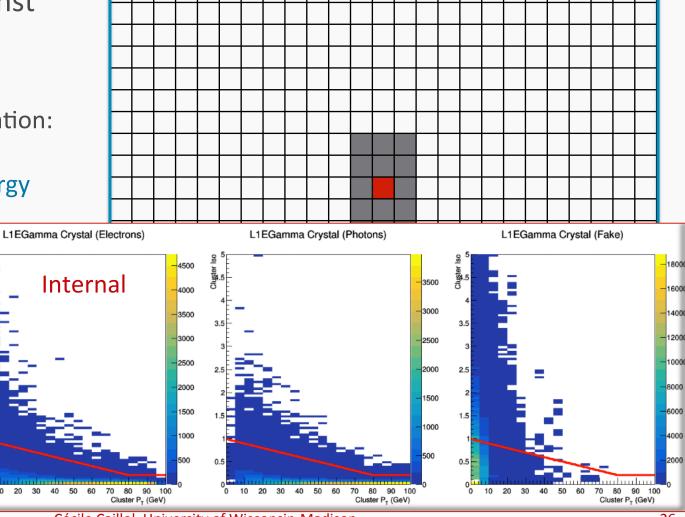
- Discriminating variables against jets:
 - Relative isolation:
 Energy in
 cluster / energy
 in 27 x 27



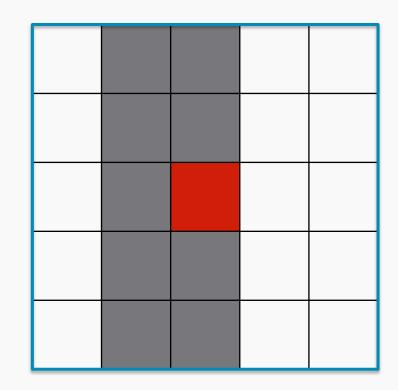
Discriminating variables against jets:

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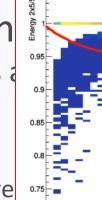
- Discriminating variables against jets:
 - Relative isolation
 - Shower shape:Max energy in2x5 / Energy in 5x5

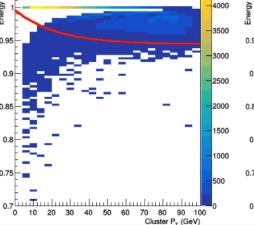


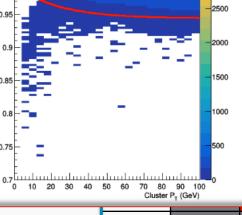
Internal

L1EGamma Crystal (Electrons)

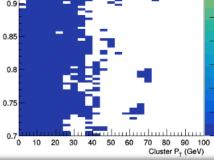
 Discrim variables a jets:







L1EGamma Crystal (Photons)



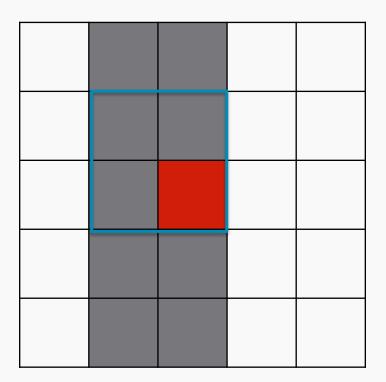
Relative

– Shower shape: Max energy in 2x5 / Energy in 5x5



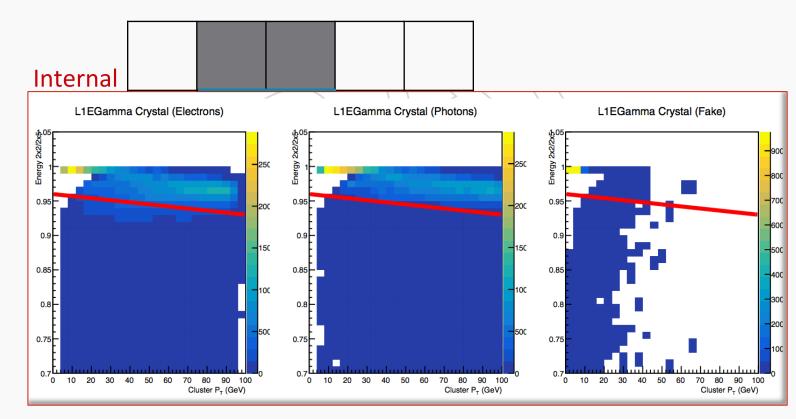
Photon algorithm

- Additional shape variable:
 - Photon shower shape (max energy in 2x2 / max energy in 2x5)

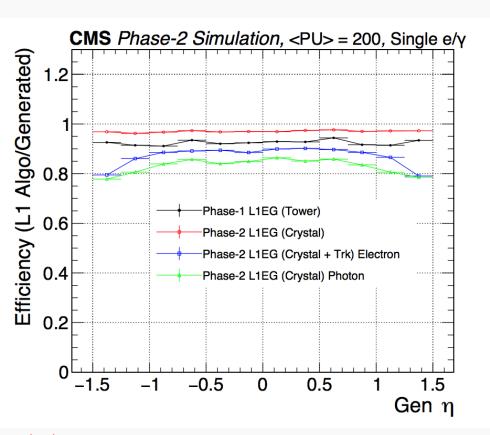


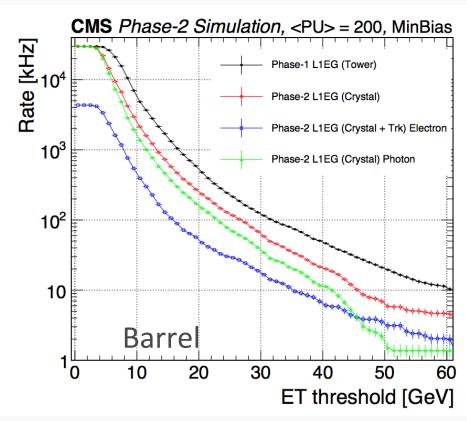
Photon algorithm

- Additional shape variable:
 - Photon shower shape (max energy in 2x2 / max energy in 2x5)



- Phase-2 calo-based only algorithm performs better than phase-1 because of higher granularity
- Matching the objects to tracks can further reduce the rate by an order of magnitude





Conclusion and prospects

- Geometry and trigger primitives defined for phase-2 calorimeter trigger
- Algorithms for specific objects developed to check performance
- Hardware R&D on the way:
 - Virtex-7 μTCA and ATCA cards
 - Embedded Linux
 - High level synthesis (HLS) coding



