Trigger Upgrades Introduction

- **First Day: Review the status of the R&D effort.**
  - Progress on algorithms
  - Impact of the HCAL upgrades to trigger (TPGs)
  - Demonstrator R&D effort and results
  - We will be seeing significant progress in all aspects which will enable us to conclude that things have matured enough to start planning our Trigger Upgrades TDR.
- **Second Day: Need to organise and plan the Phase-I trigger**
  - Need to keep ahead of the detector upgrades and dictate the physics/trigger needs to them.
  - We have several successful demonstrators at hand but this is only a good start and does not guarantee the success of the progress. For this we need a plan that includes.
    - **Firmware plan**
    - **Software plan**
    - **Road map for producing and commissioning the new trigger.**
  - These are the subject s to be discussed in the second day.

First Day: 18.10.09

10:00	Introduction and Goals	FOUNTAS, Costas
10:10	HCAL Trigger Primitives	MANS, Jeremiah MANS, Jeremiah
10:25	ECAL TPG Hardware - Opto-SLB	DA SILVA, Jose
10:40	uTCA Matrix Card Status	JONES, John
10:55	uTCA Aux Card Status - TTC+S-LINK64	GORSKI, Thomas Andrew SMITH, Wesley
11:10	Muon Trigger Upgrades - CSC	FURIC, Ivan Kresimir
11:35	Global Trigger Upgrades	TAUROK, anton
12:00	Future Trigger Designs	JONES, John
12:25	Future Trigger Designs	GORSKI, Thomas Andrew
12:50	break	
14:00	Track Trigger Designs for Phase - II	HEINTZ, Ulrich
14:25	Simulation Studies for Track Triggers	FRAZIER, Robert
14:50	HCAL TPG Simulation Studies	NACHTMAN, Jane
15:15	Calorimeter Trigger Simulation Studies	DASU, Sridhara
15:40	Firmware Studies and Performance	SCHULTE, Michael

Second Day: 29.10.09

time	title	presenter
10:00	Introduction and Goals	FOUNTAS, Costas
10:15	Firmware Organisation - Validation - Commissioning	SCHULTE, Michael
10:45	Hardware Demonstrators Goals and Plans	ILES, Gregory Michiel
11:15	Online Software Needs and Roadmap	FRAZIER, Robert
11:45	Infrastructure	HANSEN, Magnus
12:15	Manpower commitments - A summary	
12:35	Closing	FOUNTAS, Costas

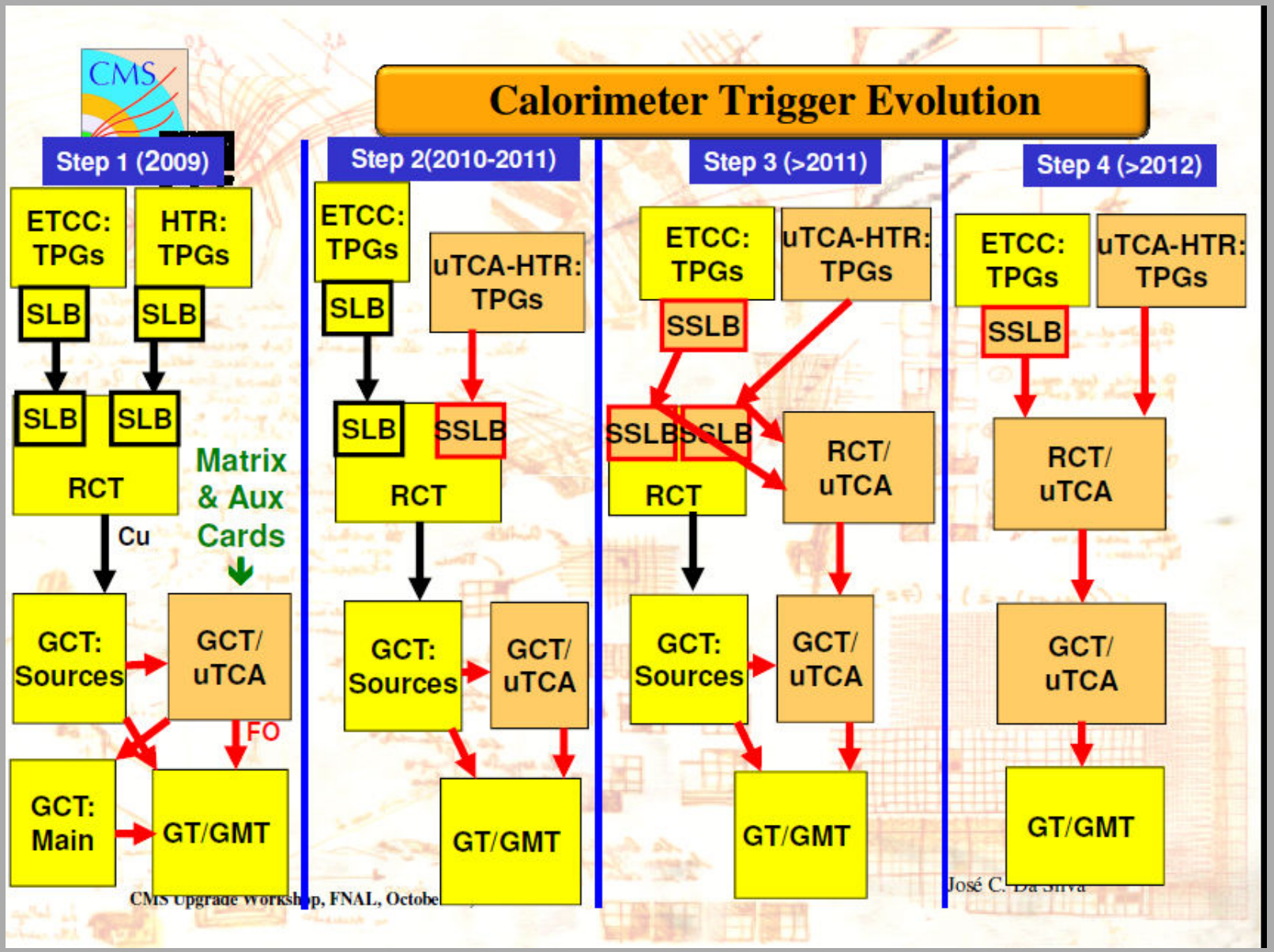
Goal: **We need to conclude our design by April 2010**

Otherwise there is a danger that the various efforts will either reproduce each other or they may de-focus and become incoherent.

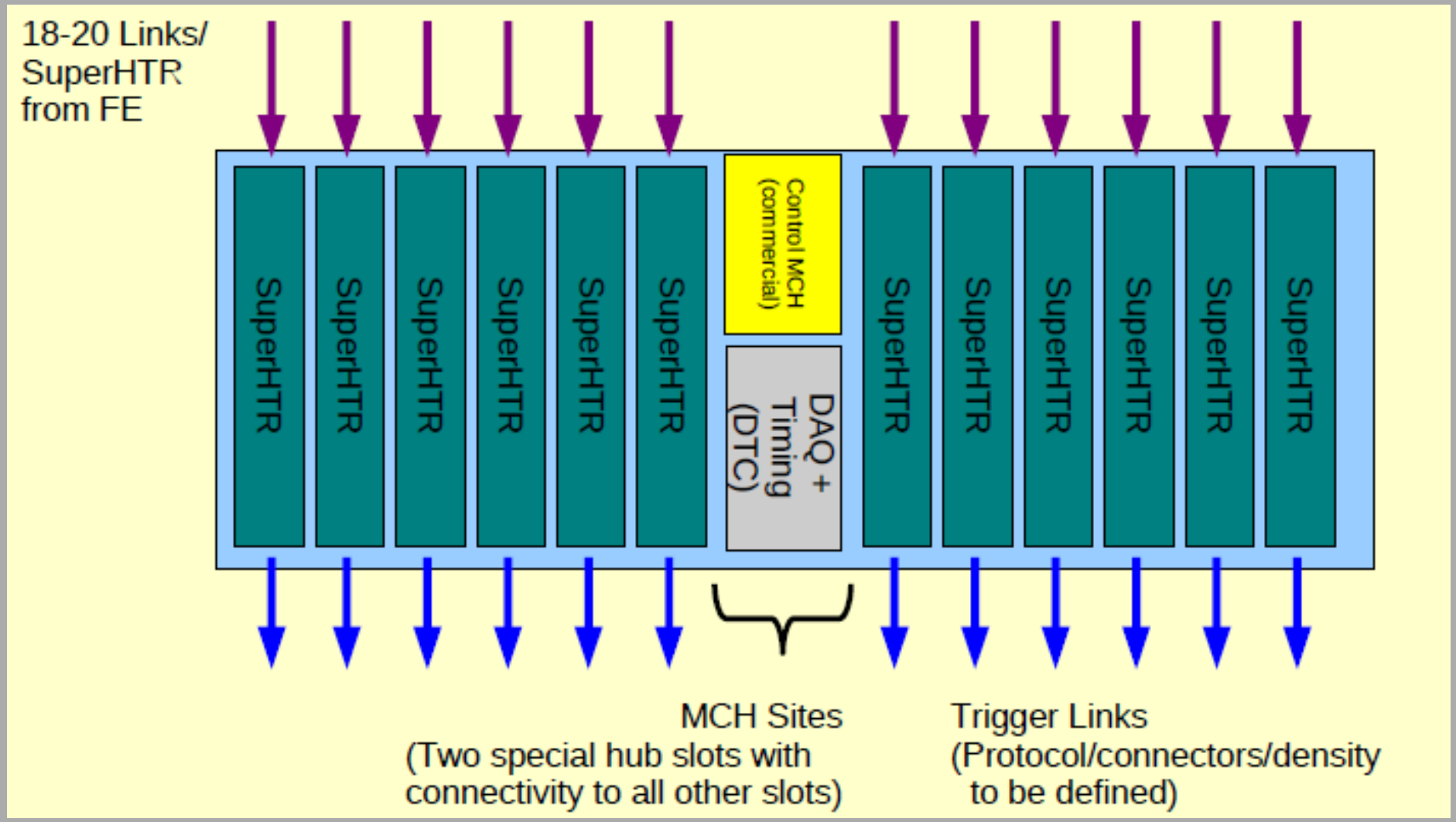
Goals of the Trigger upgrade

- **The Current Trigger system had had its TDR in 2000 and it was designed in the 90s. It will work for 10^34 as demonstrated be a large number of studies (MC).**
- **There may be surprises after the first data come up and we need to have the capability of replacing this system rapidly to enhance the CMS physics reach.**
- **We should be also be able to do this upgrade without disturbing the CMS data taking capability (some people use the word 'adiabatic').**

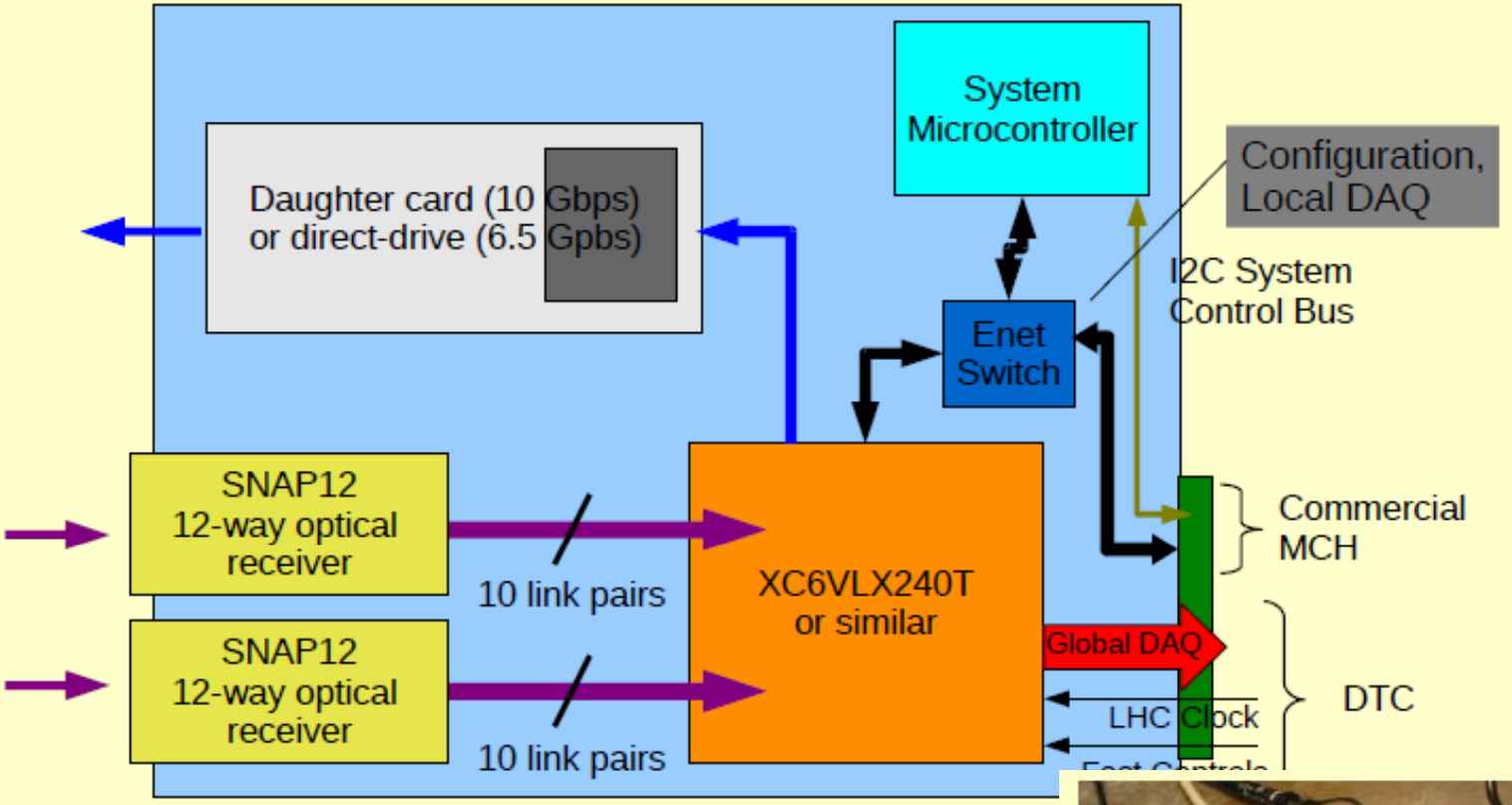
Calorimeter Trigger Upgrade: FNAL-WS-08



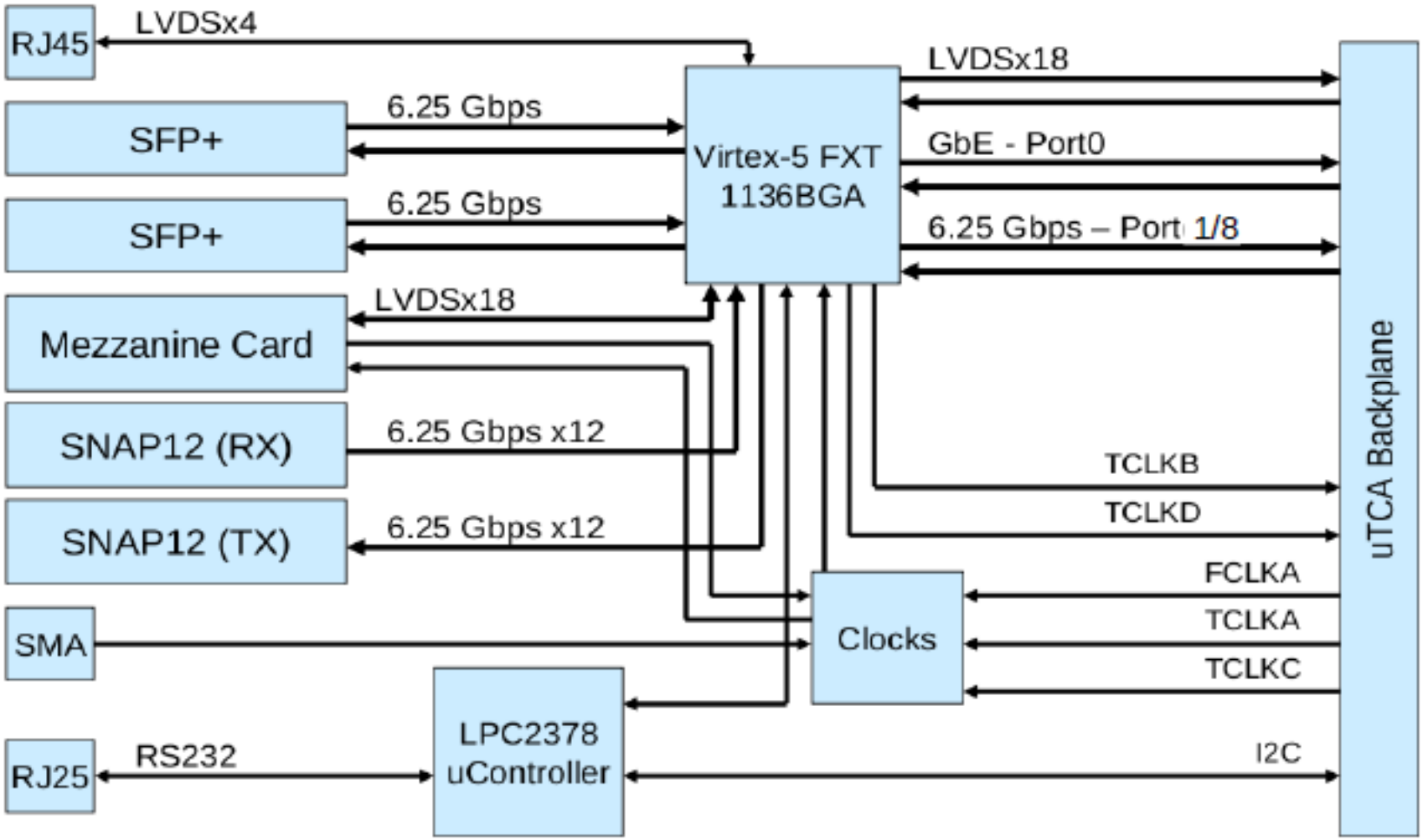
HCAL Trigger Primitives



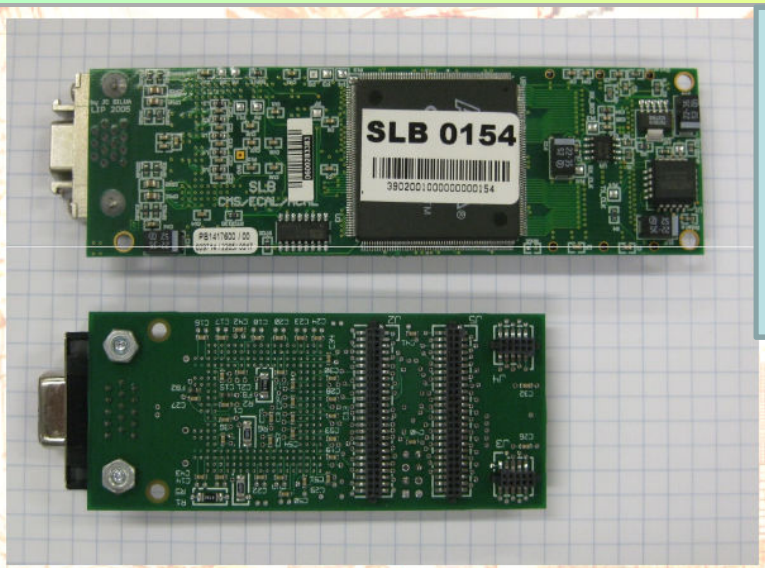
SuperHTR


System Microcontroller
Configuration, Local DAQ
Daughter card (10 Gbps) or direct-drive (6.5 Gpbs)
I2C System Control Bus
Enet Switch
SNAP12 12-way optical receiver
SNAP12 12-way optical receiver
10 link pairs
10 link pairs
XC6VLX240T or similar
Commercial MCH
Global DAQ
LHC Clock
DTC

SuperHTR

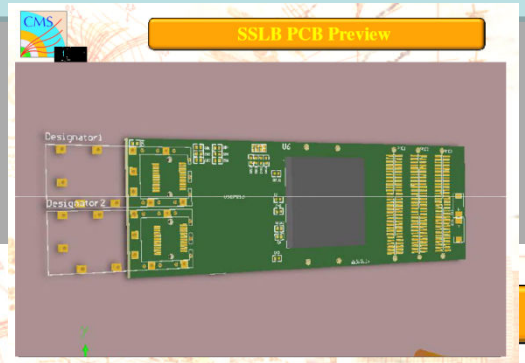

RJ45
LVDSx4
SFP+
6.25 Gbps
SFP+
6.25 Gbps
Mezzanine Card
LVDSx18
SNAP12 (RX)
6.25 Gbps x12
SNAP12 (TX)
6.25 Gbps x12
SMA
RJ25
RS232
LPC2378
uController
Virtex-5 FXT
1136BGA
LVDSx18
GbE - Port0
6.25 Gbps – Port 1/8
TCLKB
TCLKD
FCLKA
TCLKA
TCLKC
Clocks
I2C
uTCA Backplane

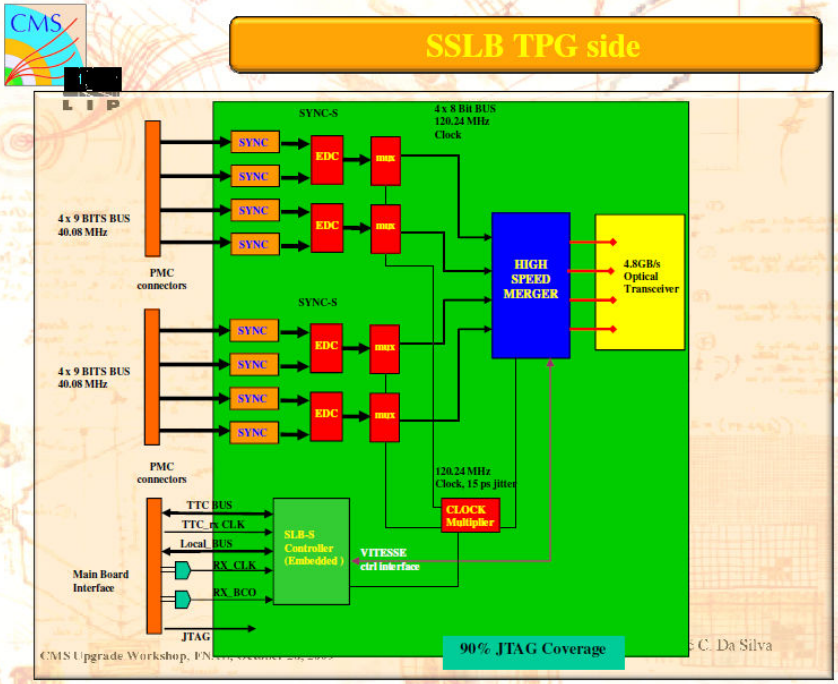
Replacing the ECAL Links SLB with Opto-SLB

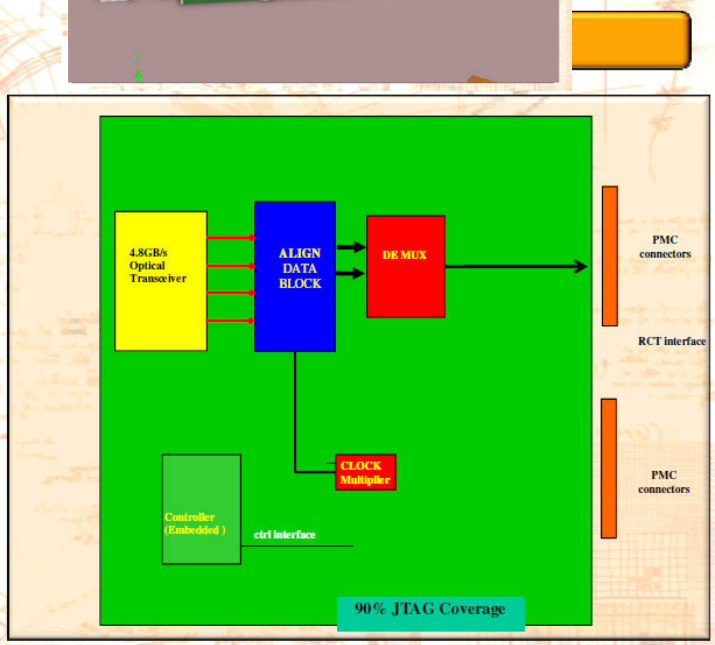


1026 Copper Links from ECAL TPGs need to be converted to Optical Links.

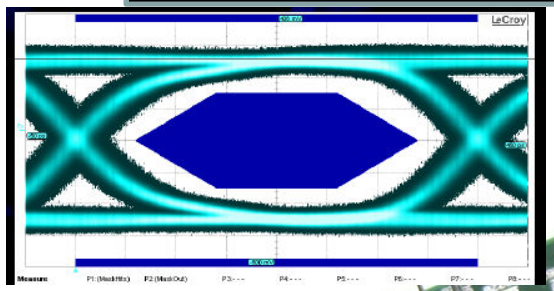
The new design (see below) is called the Opto-SLB

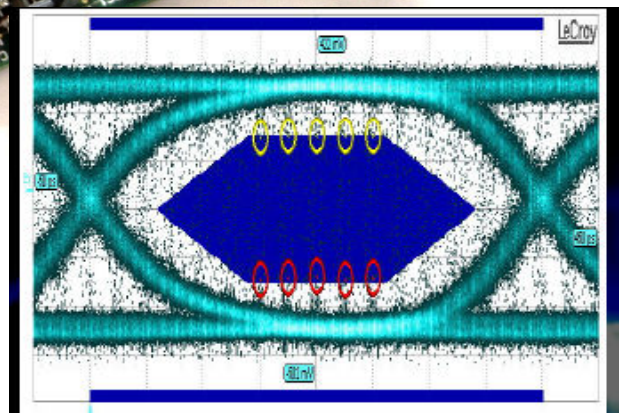






The Matrix Card





Matrix Rev-A: Works !

Matrix Card Status

The original Matrix Card design had a number of (mostly minor) faults:

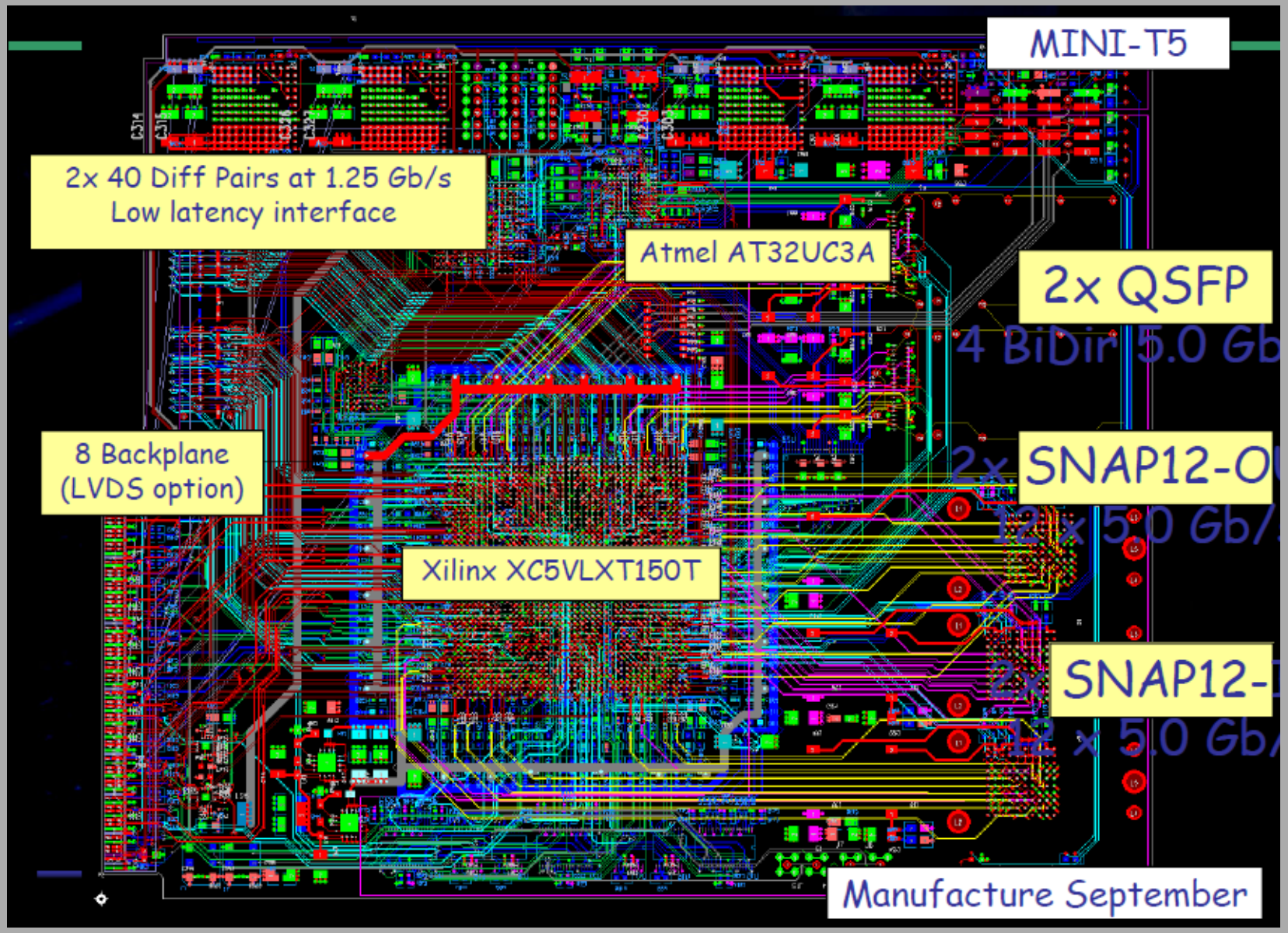
- Microcontroller was too small for firmware
- Some TX serial links showed signal degradation (plane structure issue?)
- Missing pull-up / series-termination resistors

Tests included:

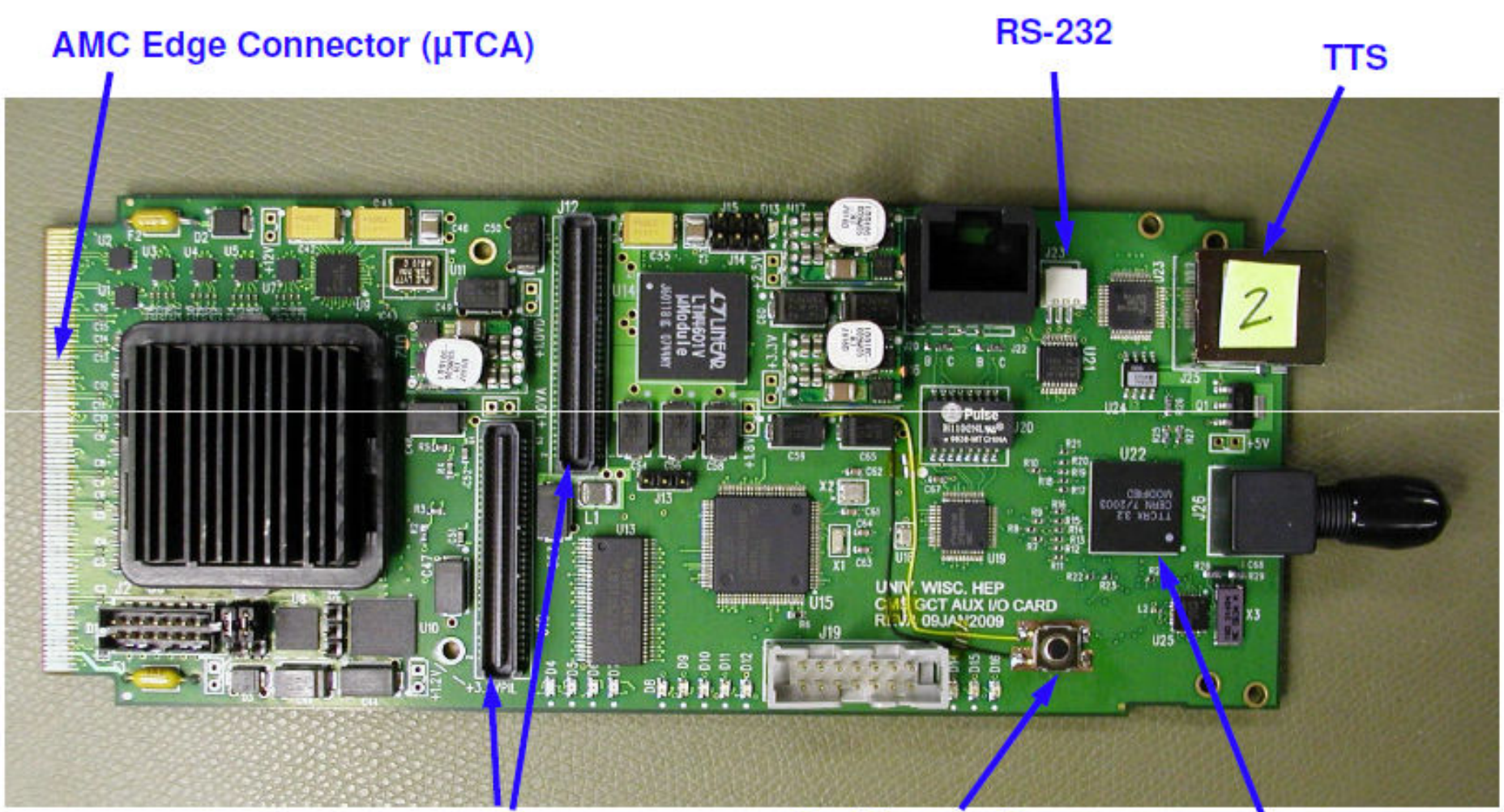
- All serial links (internal loopback, fiber loopback – 16 links)
- GbE over backplane (1 link)
- GbE over fiber (1 link)
- uC control & programming
- CPLD JTAG switching
- DDR2 RAM
- Inter-Matrix card testing (16 links)

The Matrix Design is now Available

- The Matrix Card was intended to be a common hardware platform
- For that to happen, the design must be made readily available
- The Open Hardware Repository (OHR, Javier Serrano, CERN) was conceived to create common hardware platforms that could be shared for future development
- Design is made available in full (reference schematics, gerbers, etc…)
- As part of the process, the design is reviewed and tested by many groups
  - → Increased reliability
  - → Shared knowledge
- The Matrix card design will soon (if not already) be available IN FULL on the OHR (www.ohwr.org)

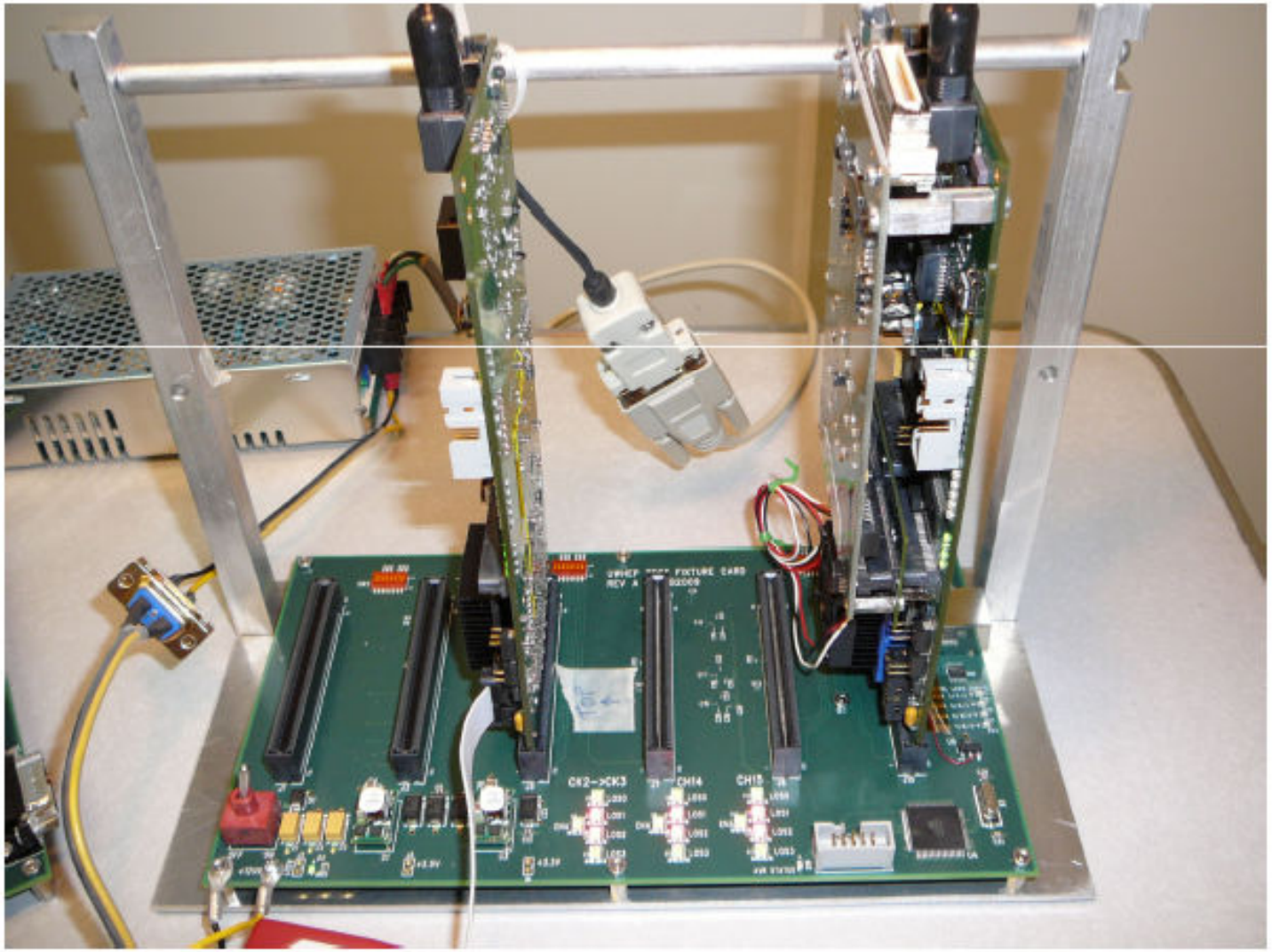

MINI-T5
2x 40 Diff Pairs at 1.25 Gb/s
Low latency interface
Atmel AT32UC3A
2x QSFP
4 BiDir 5.0 Gb
8 Backplane
(LVDS option)
2x SNAP12-O
12x 5.0 Gb/
Xilinx XC5VLXT150T
2x SNAP12-
12 x 5.0 Gb/
Manufacture September

Slink64 and TTC: Aux Card



Test Setup for Aux Card:UW

Two Aux Cards in Test Fixture Running a GTP Link Test
(6 connections—4 passive, 2 through switches)

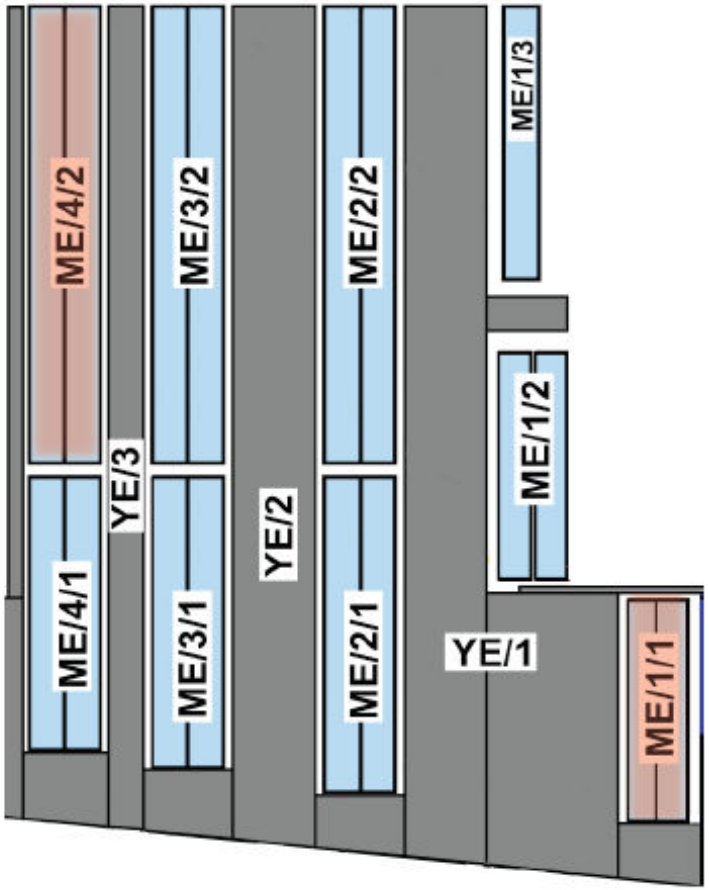


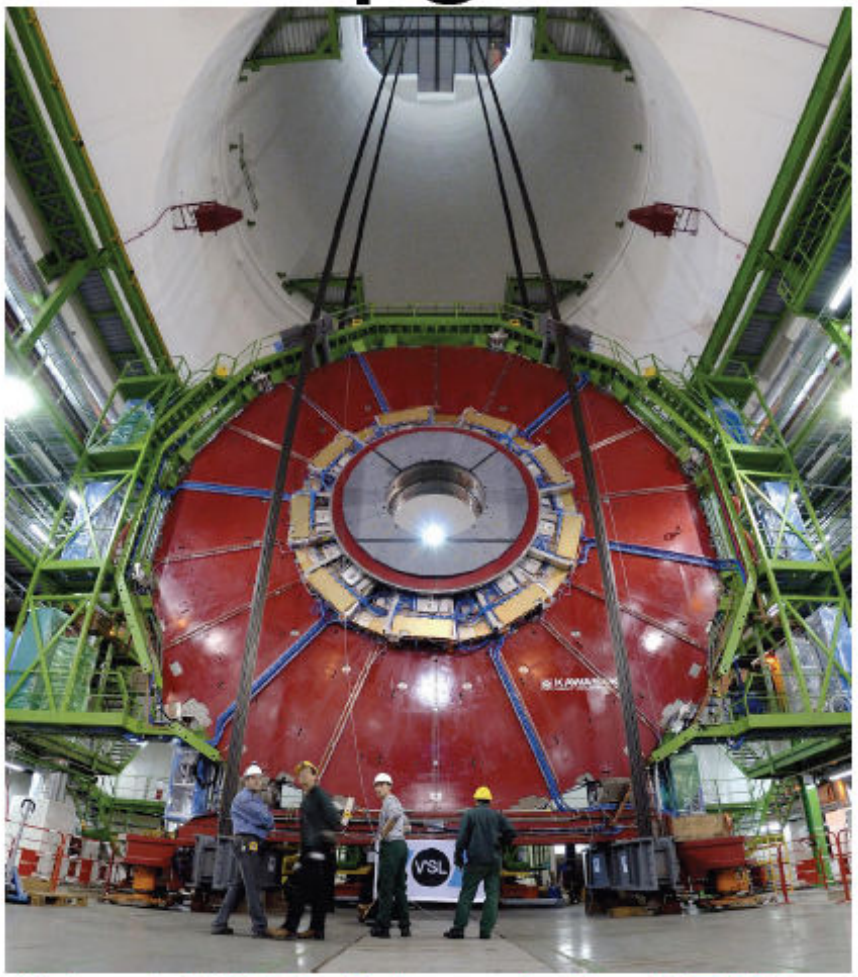
Status of Calorimeter Demonstrators

- We have Matrix and Aux Card working prototypes and this means:
  - We could replace GCT if the first LHC data shows that more complicated algorithms are required to enhance the CMS physics capabilities.
  - This system or modified designs of it is expandable and can provide the basic design for all calorimeter triggers.
  - We are well in our way to stay ahead of HCAL upgrades and provide triggers as needed.
- However, GCT experience shows that from working prototypes one needs 3 years + considerable amount of expertise resources.
- We need now to get organised and produce a roadmap for the final system

CSC Trigger Upgrades

ME4/2 and ME1/1 upgrades





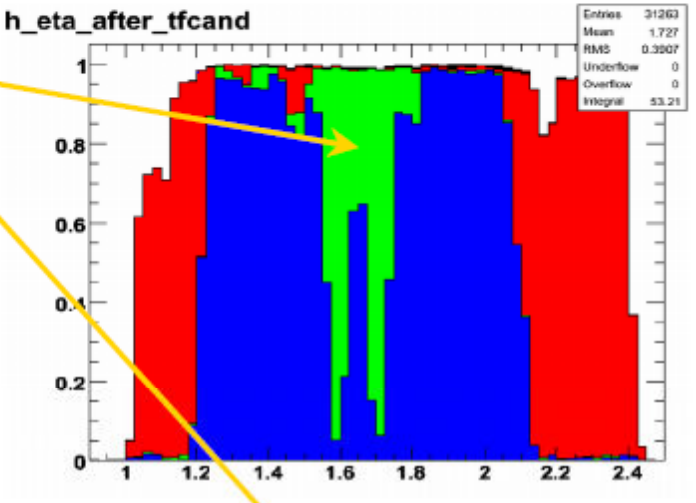
"Empty" YE3 disk ready for ME4/2

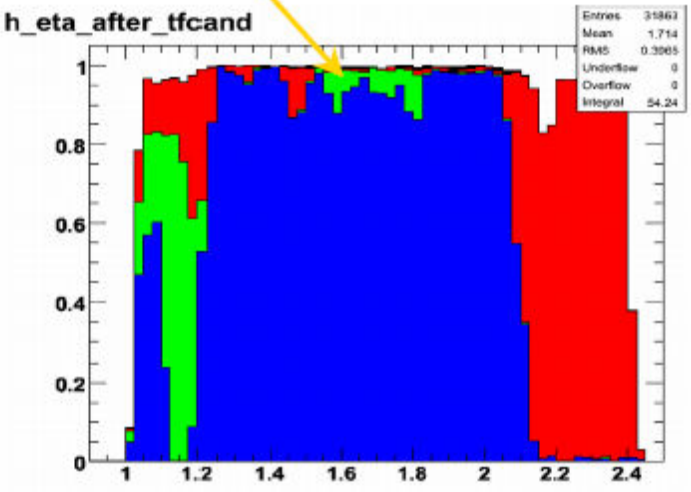
CSC-Trigger Efficiencies

Simulation result (May '09)

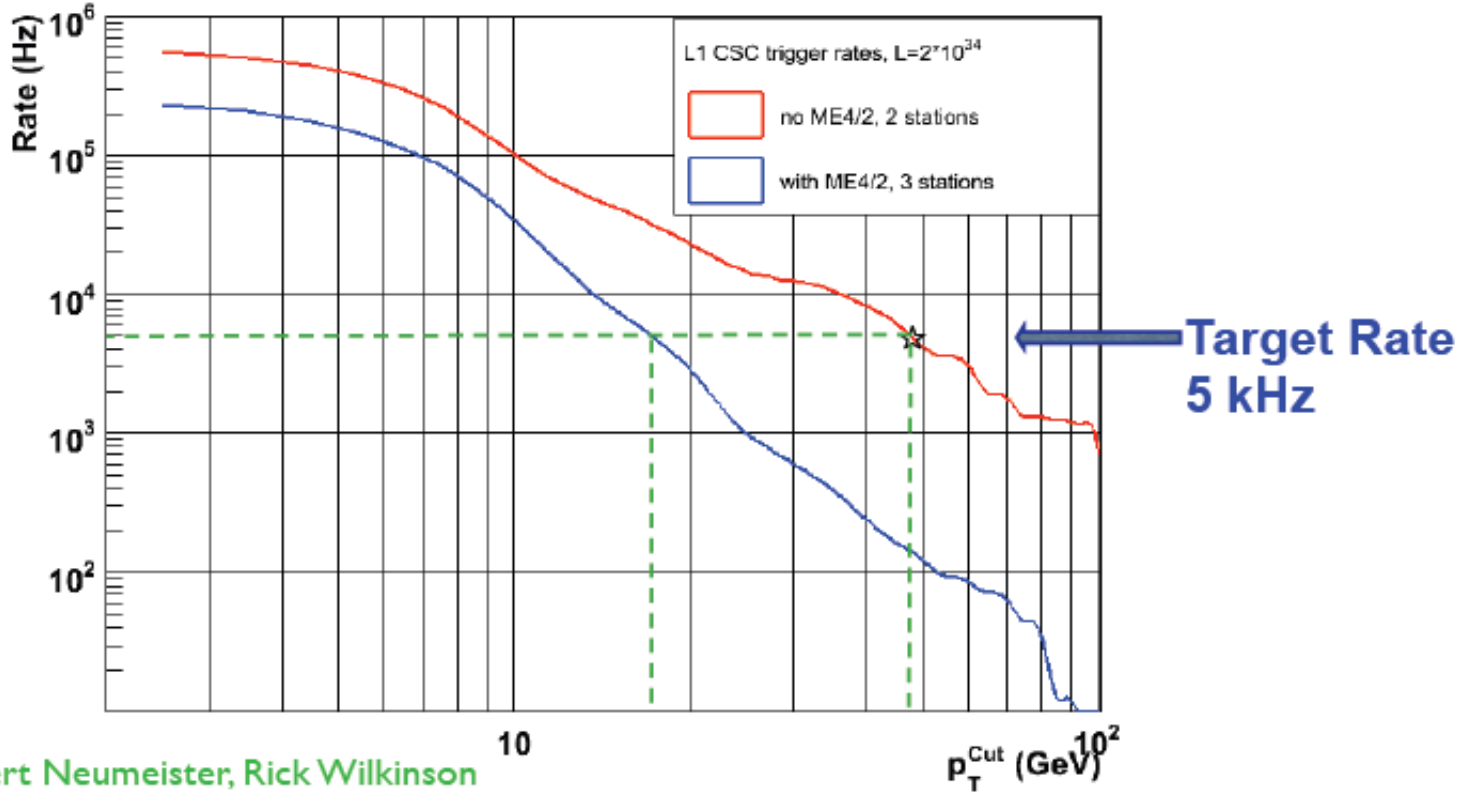
(Vadim Khotilovich, Alexei Safonov)

- Efficiency gaps for good quality TF tracks disappear with addition of ME4/2
- ME4/2 will be included by default in 31X
- Back-porting to 22X took a considerable amount of effort
  - Thanks to the experts: Rick Wilkinson, Tim Cox, Oana Boeriu and Slava Valuev!





CSC Trigger Rates



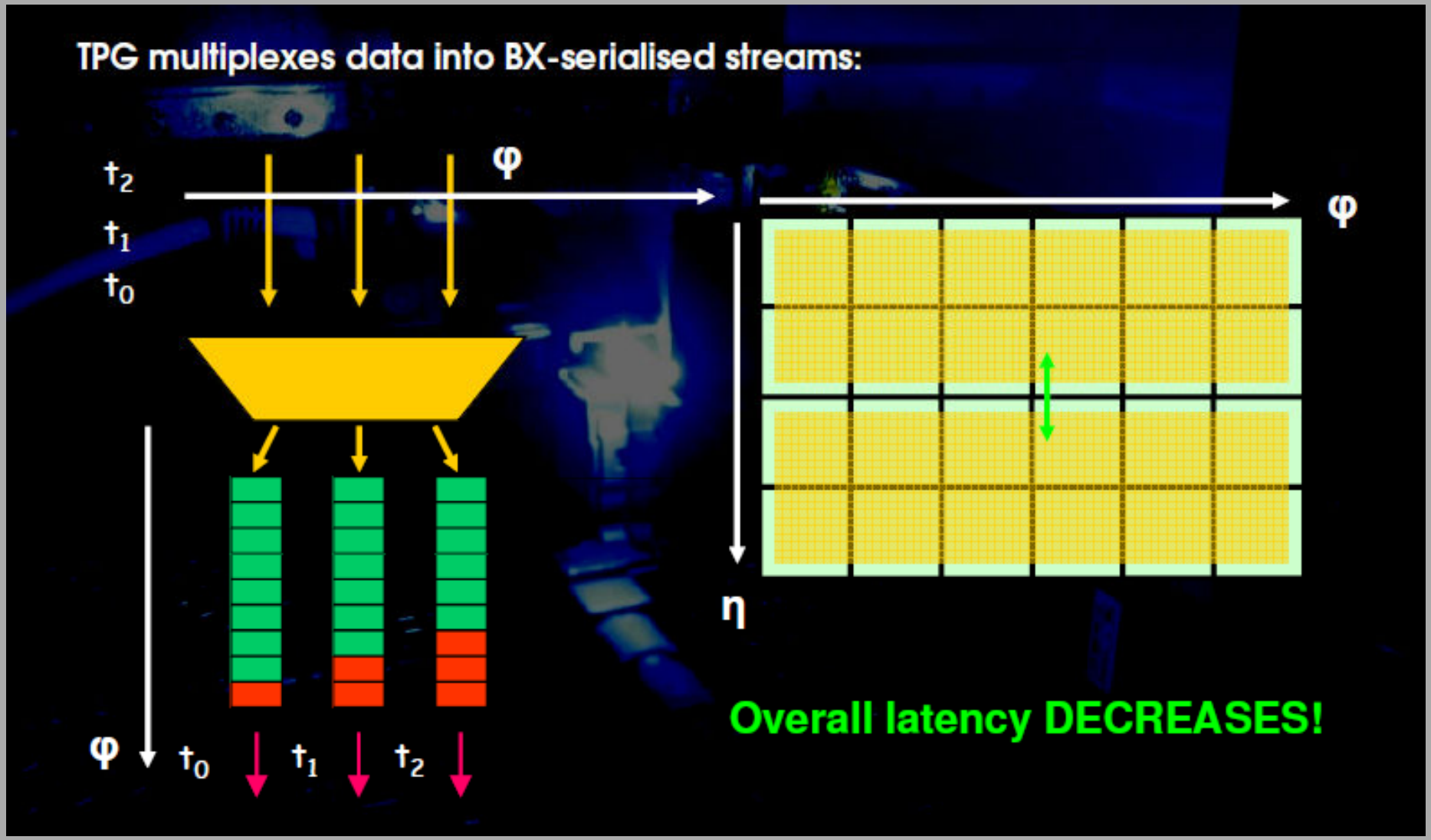
Ingo Bloch, Norbert Neumeister, Rick Wilkinson

Port Cards

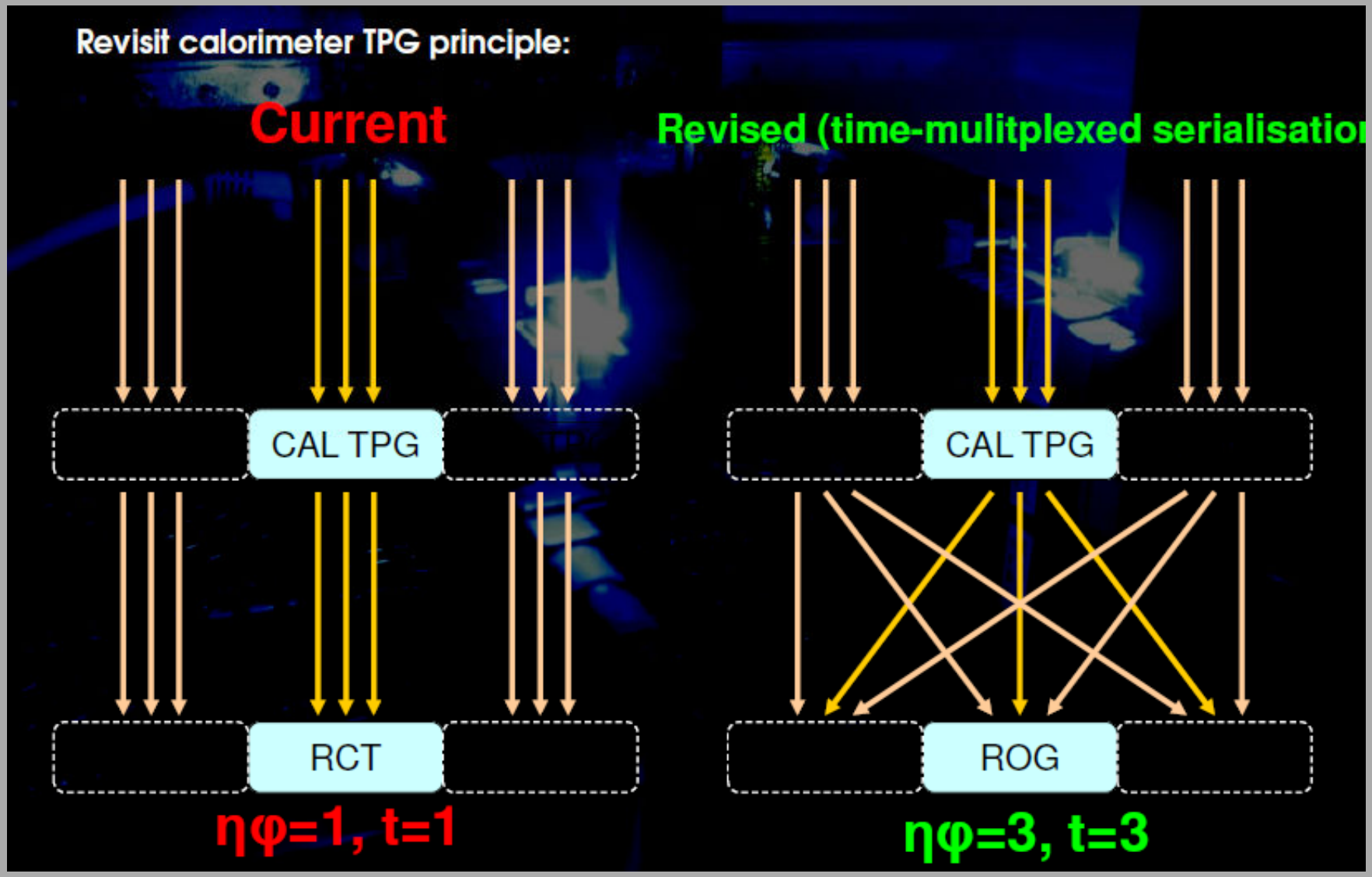
- Current design is adequate for LHC luminosity
  - 2 LCTs (di-muon signal) + 1 (background) = 3 LCTs per Port Card per BX
- With luminosity upgrade, we expect ~7 LCTs per Port Card per BX.
  - Preliminary simulated data, no measurements so far
  - Reality could be **worse**
- Port Card becomes a **bottleneck**
- Solution:
  - Keep 2 Trigger Primitives per chamber
  - Bring all LCTs to SP (18 per Port Card per BX), no filtering
    - May keep the filtering option in Port Cards, in case it's needed
- Port Cards have to be redesigned and replaced system-wide
  - Faster data links evaluated.

All off detector Electronics (Sector Proc.) must change too

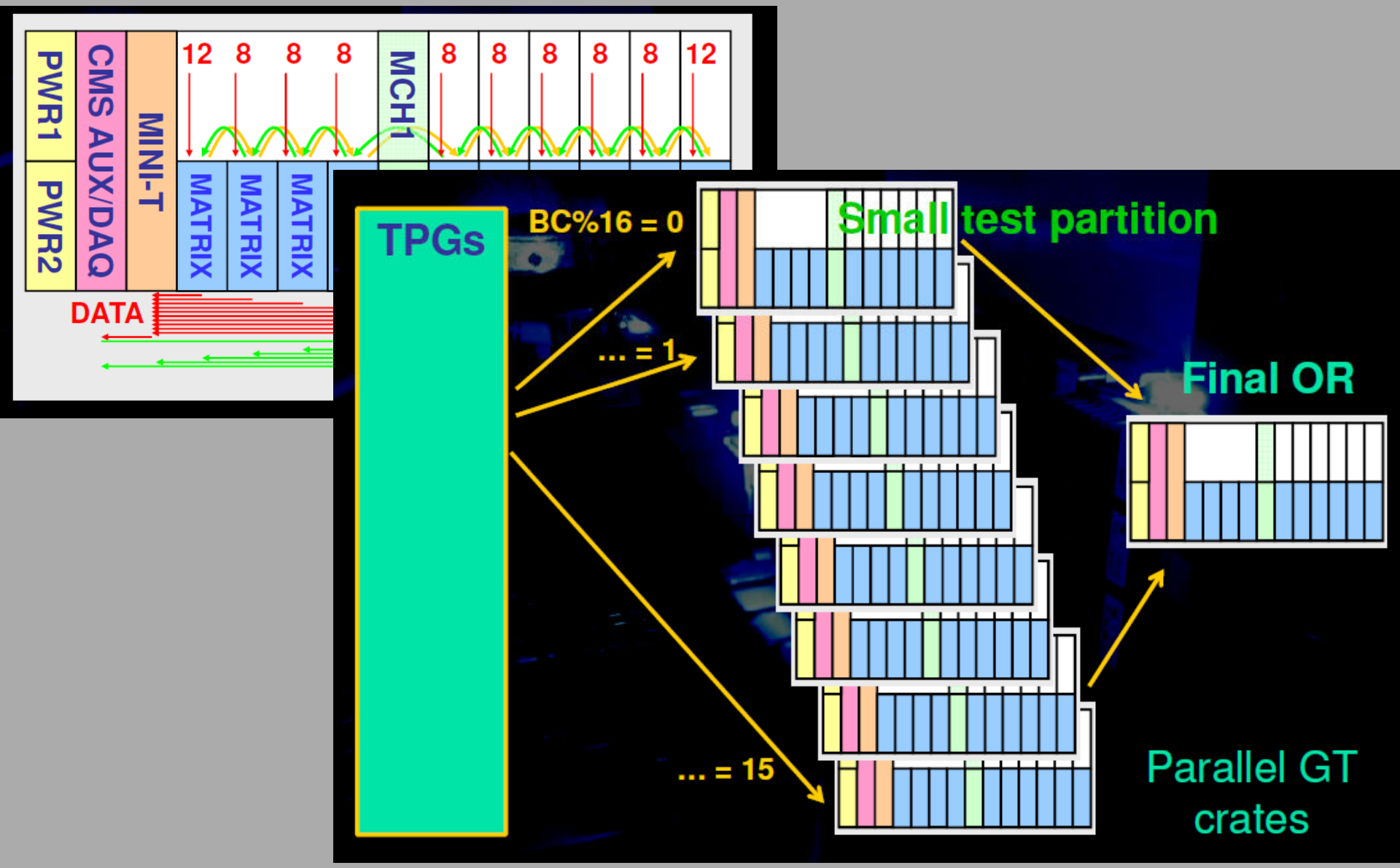
Designs for the next trigger - I



Designs for the next trigger - I



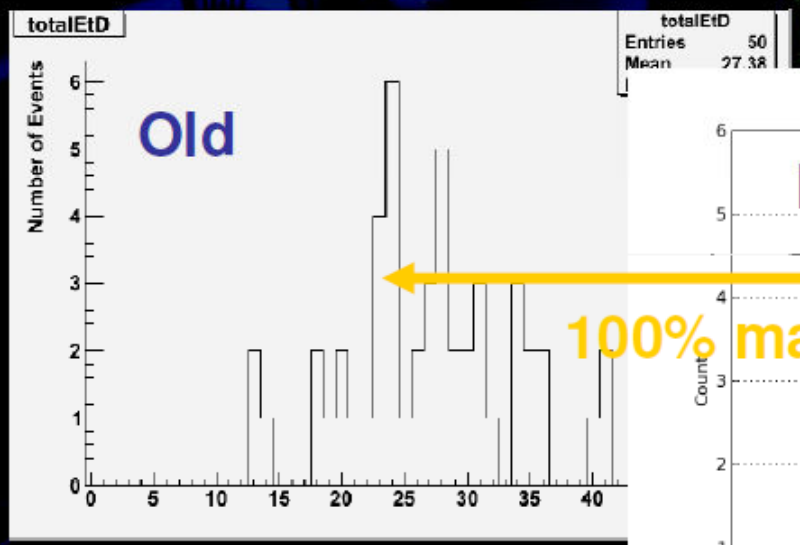
Designs for the next trigger - I

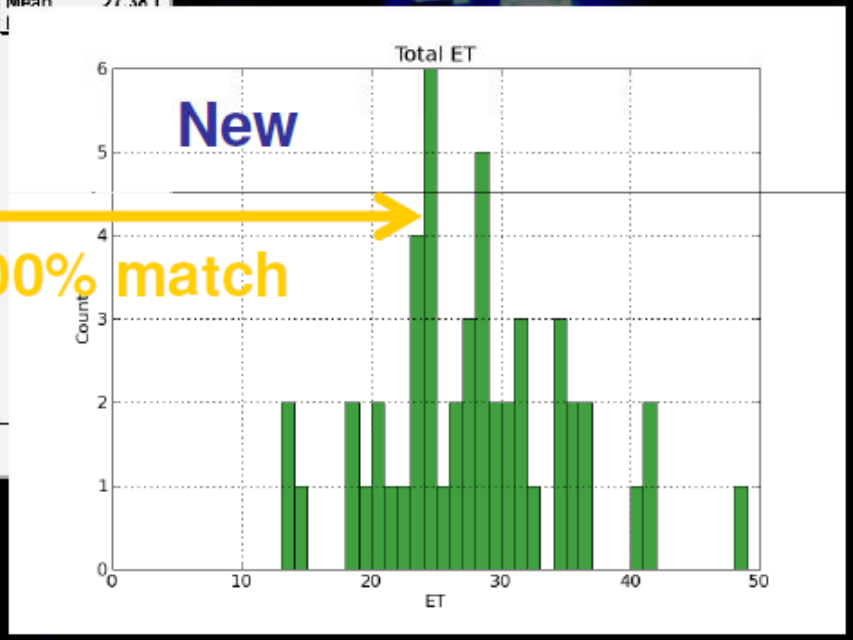


Compare current GCT emulator with new algorithms

Results are identical (except for binning, etc…) in ET sum case

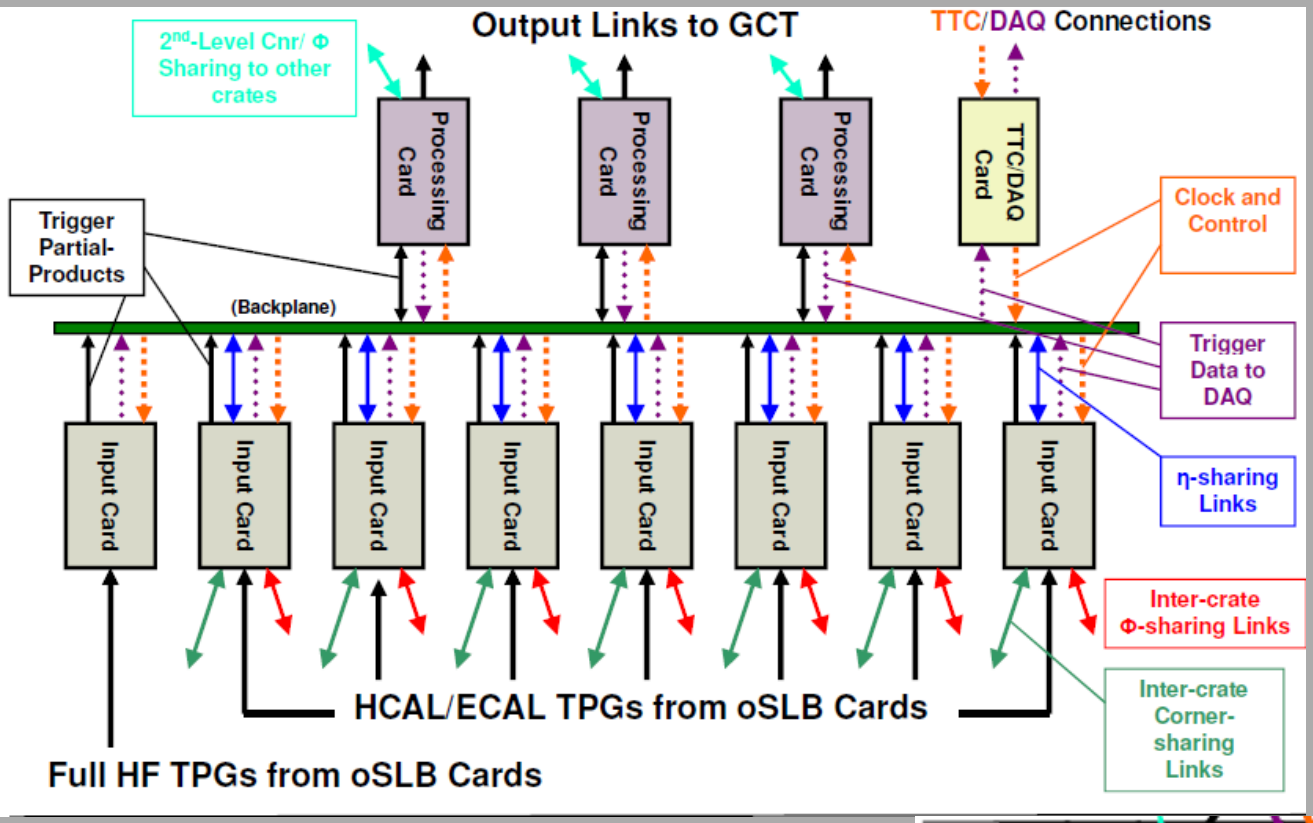
Data shown in slide from CRAFT

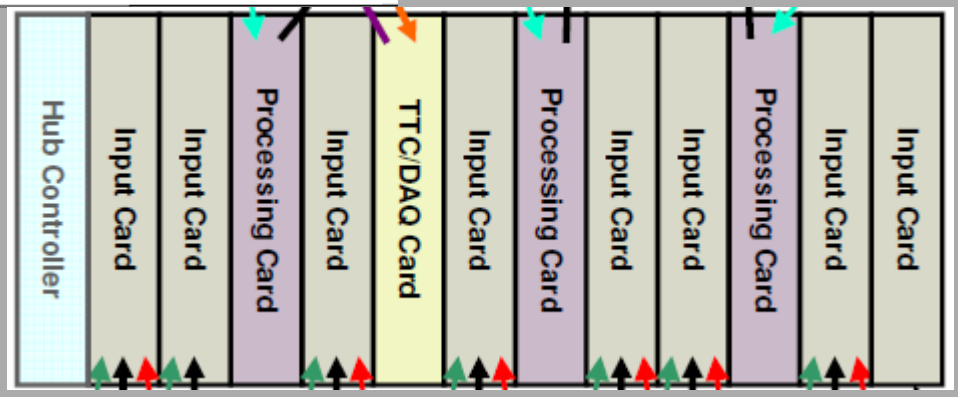




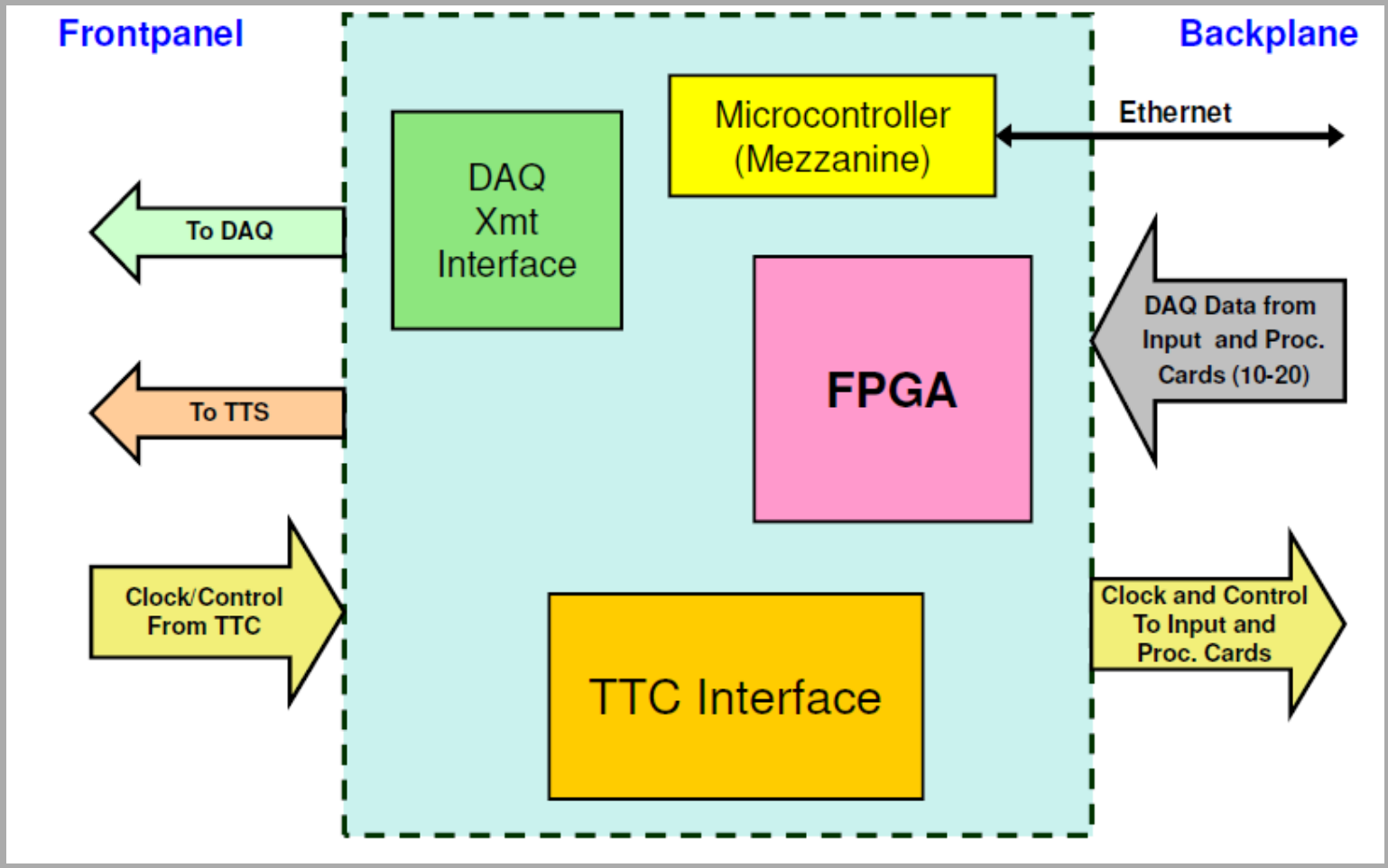
100% match

Designs for the next trigger - II

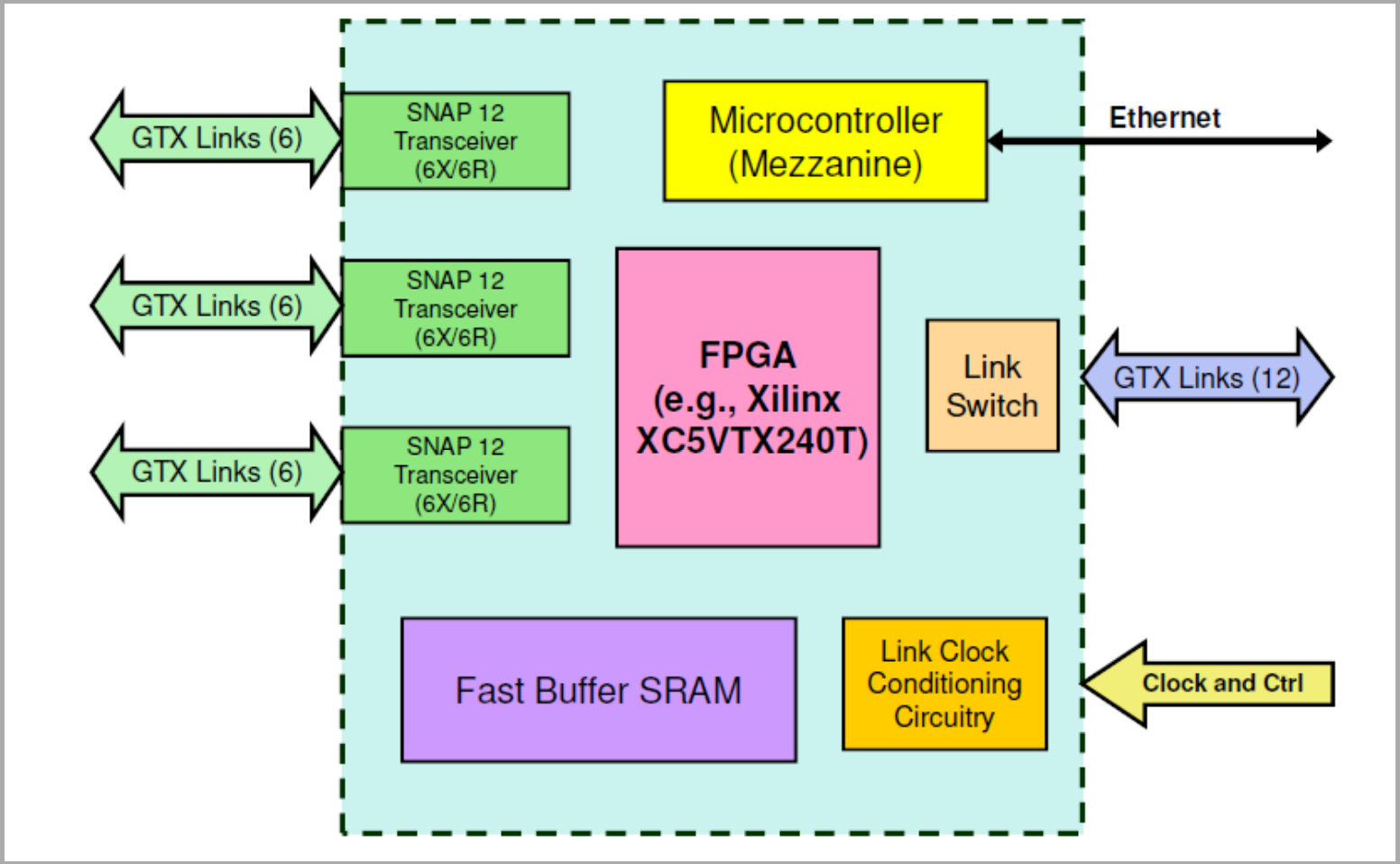




Designs for the next trigger - II

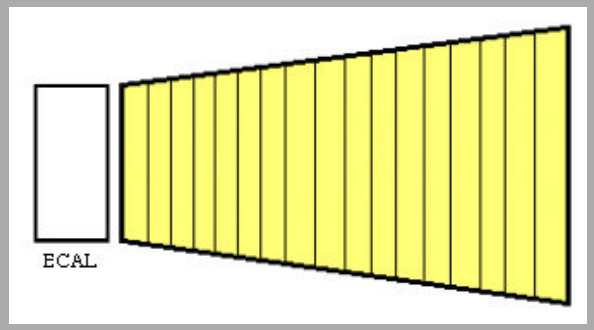


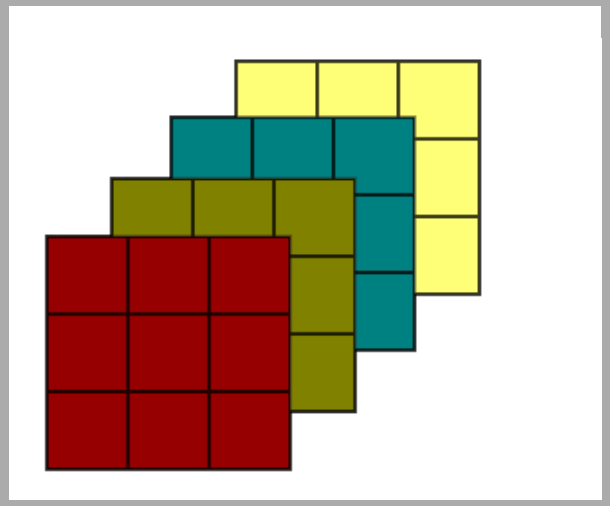
Designs for the next trigger - II



HCAL Trigger Primitives

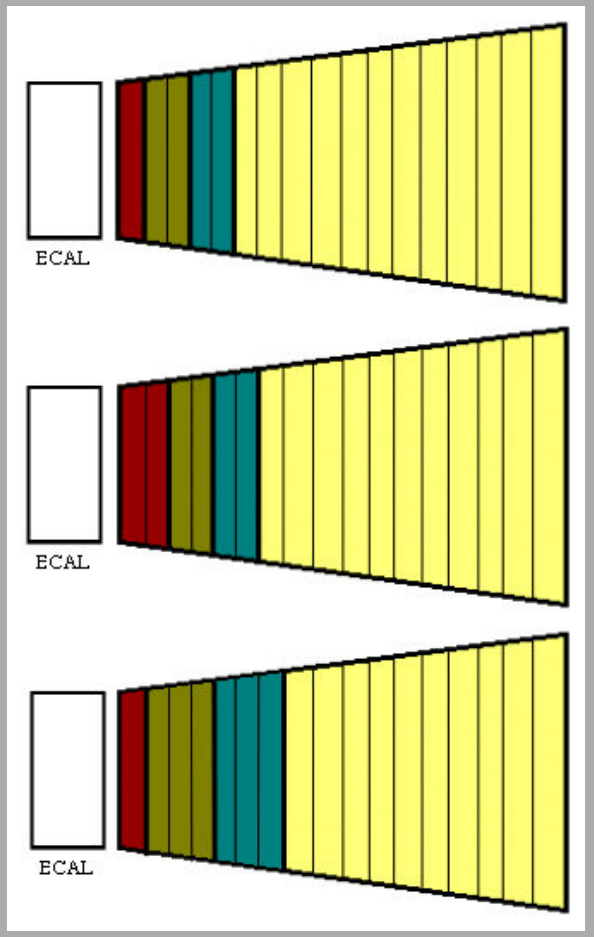
Current:





4 depths of HCAL

With SLHC upgrade, we can split HCAL into 4 depths:



HCAL TPG CODE

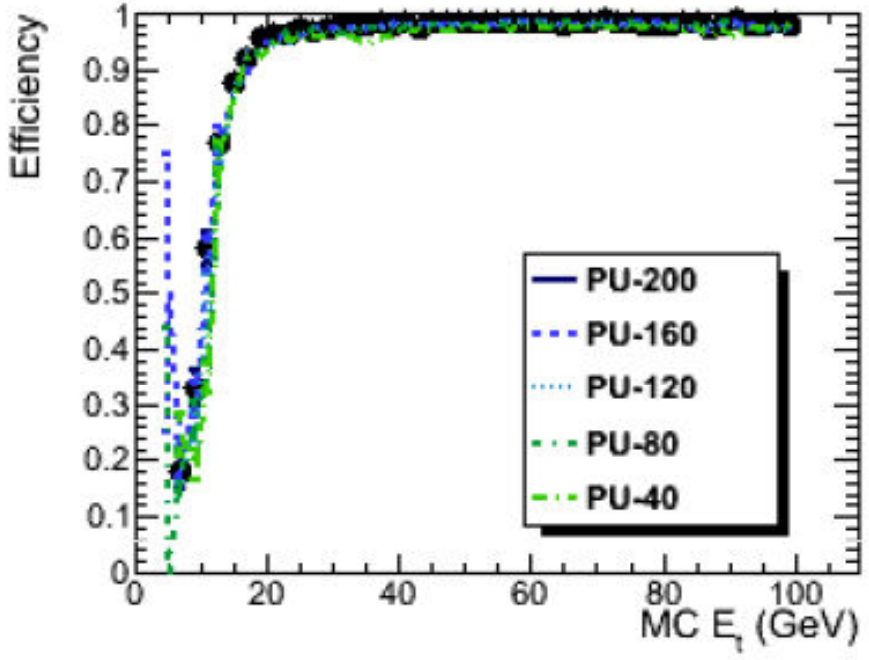
- HcalTriggerPrimitiveDigi
  - Identified by an HcalTrigTowerDetId
  - Contains multiple HcalTriggerPrimitiveSamples with bit-wise information
  - An HcalTriggerPrimitiveSamples has:
    - 8 bits of “compressed et”
    - 1 bit of “fine grain” energy information
- HcalSLHCTriggerPrimitiveDigi
  - Identified by an HcalTrigTowerDetId
  - Contains multiple HcalSLHCTriggerPrimitiveSamples with bit-wise information
  - An HcalSLHCTriggerPrimitiveSample has:
    - **8 bits** of “compressed et”
    - **8 bits** of “fine grain” – precise usage to be defined
    - **8 bits** of “isolated compressed et”

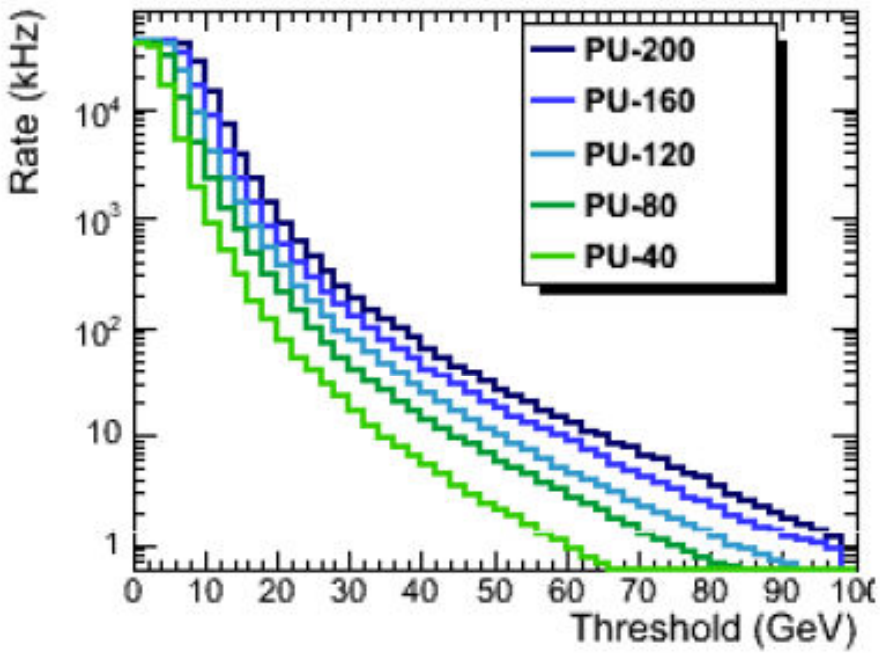
HCAL TPG Code

- Edmund's code is on the UserCode CVS. Documentation is forthcoming.
  - UserCode/eberry/Producers/HcalSLHCTrigPrimDigiProducer/
- Using the code
  - cvs co -d Producers/HcalSLHCTrigPrimDigiProducer UserCode/eberry/Producers/HcalSLHCTrigPrimDigiProducer/
- Use on samples produced using Jeremy Mans multi-depth simulation by adding to your cfg.py file:
  - process.load("Producers.HcalSLHCTrigPrimDigiProducer.hcalSLhcTpDigi_cfi")
  - process.TPG = cms.Path(process.simHcalSLHCTriggerPrimitiveDigis)
- Note: this is all very recent progress!

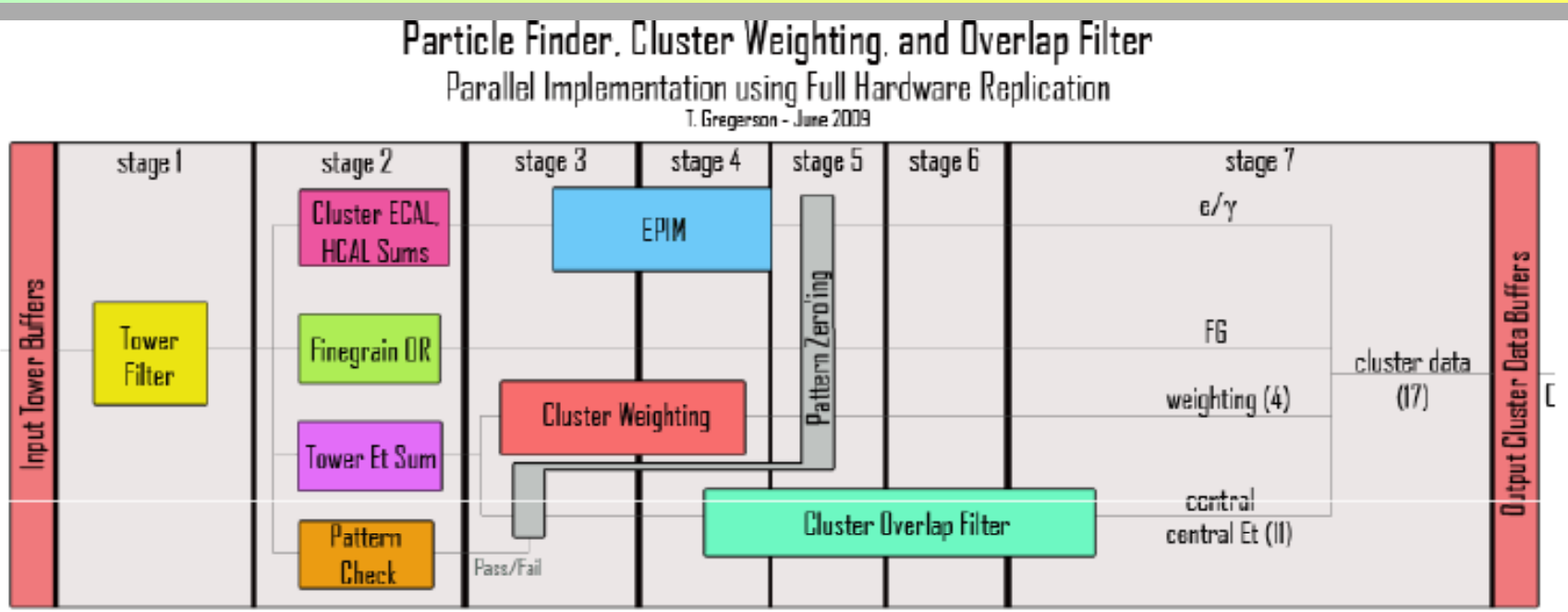
Significant Progress

Lvl-1 Trigger Simulations





Algorithm Firmware



- **Cluster finder, overlap filter and weighting logic can be processed in 7 pipeline stages (without buffering I/O)**
  - **Latency of just 35 ns**
  - **Lots of hardware is shared**
  - **Parallel computations decrease delay**
- **All designs tested with physics patterns from emulator**

Conclusions

- We have enough hardware devices at a good state and we need now to consolidate and focus (tomorrow's session)=> Road-Map
- **We need to finalise the final design by April 2010** (Workshop ?)
- First Version of the HCAL TPG Simulation code is ready (congratulations to the HCAL Colleagues)→ **By April 2010 debugged + working Code**
- Tomorrow's summary should have a draft plan to go forward…

Apologies for this summary