ASIC Building Blocks for Tracker Upgrade

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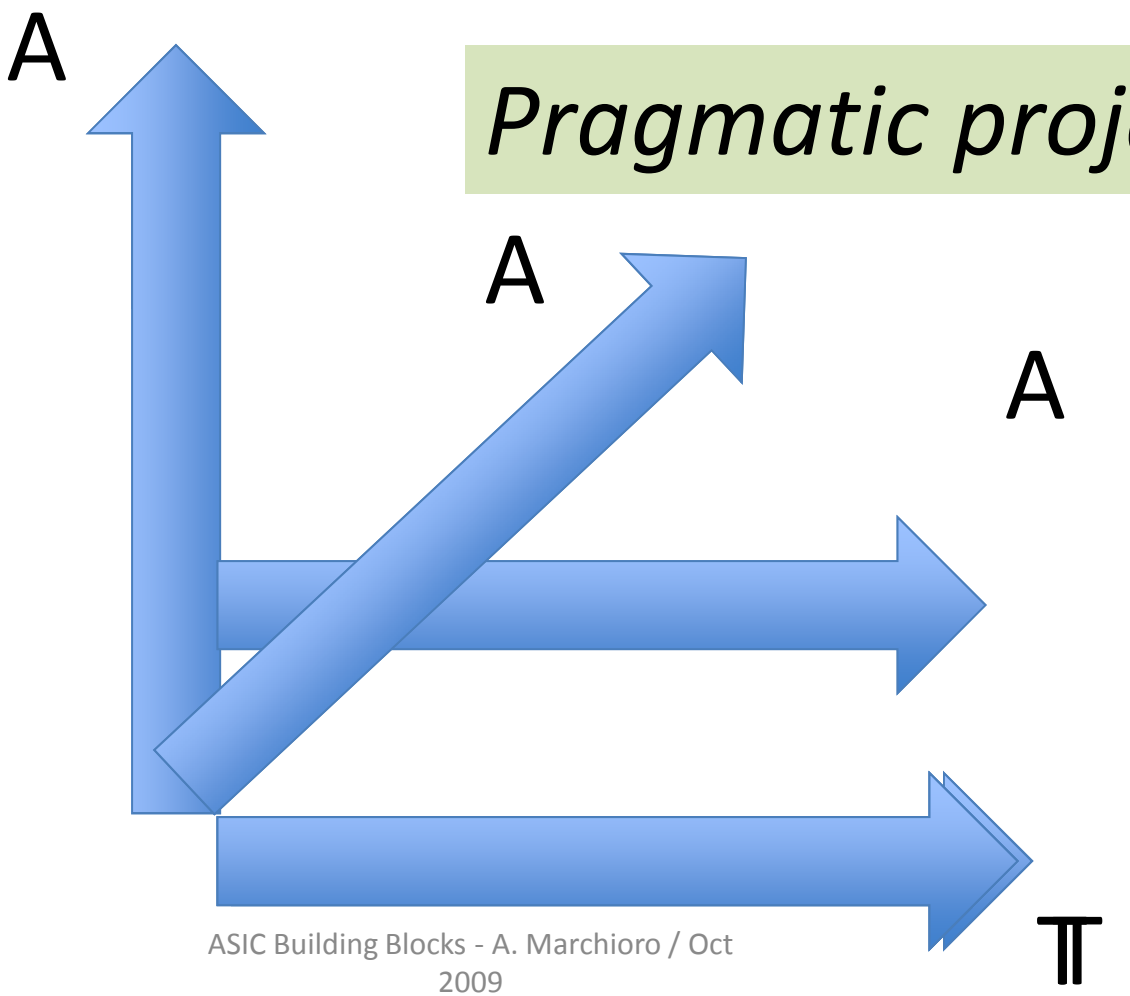
Idea behind

- As discussions on final architectures (requirements driven, i.e. top-down) apparently needs still time and discussions to converge, it appears to me as useful to allow some critical bottom-up work to make progress in parallel without further delays.

Objective: Instead of going for a "final" design immediately, a set of critical building blocks that would be part (even if approximately) of any final architecture should be defined, designed, manufactured and evaluated in a shorter time frame.

Idea behind



Pragmatic project

Benefit of this strategy

- Organizes progress along an “evolutionary” path, instead of a risky “revolutionary” one
- Allows engineers who will have to implement the final architecture to gain experience in technologies that are largely new and where a long and painful learning curve may be necessary
  - More learning now, less mistakes later
  - Don’t postpone learning because of architectural uncertainties
- Does not freeze system architecture too soon
- Does not freeze technology choice too soon, allows for adaptation to rapidly changing technology panorama
- But will help the decision process on the final architecture with the know-how gained during the design of these blocks

Building Blocks

- Front-End circuits:
  - Preamp-Shaper
  - Leakage compensation
  - Discriminator
  - Discriminator Reference and control
  - Bias DAC
  - Bandgap voltage reference
- Timing
  - PLL
    - Programmable delay clock source
- Digital Blocks
  - Event Storage memory
  - Slow Control Interface
  - GBT (e-Link) adapter
  - Various Low Power Techniques
- Interfaces
  - Slow control interface
  - Low Power digital link
- Low cost interconnection technology
  - Macro cells for C4 bump bonding (@150-225 μ pitch)

Why 90nm

- Pixel area in trigger layer is ~(100 x 1800 μ)
  - Complexity of trigger channel is much higher than present tracker or pixels, FE chip should be “edge-less” to allow no dead-detector area
    - Analog FE, biasing, discriminator, memory, coincidence etc.
- 90 nm offers 10-20% power saving
  - Power is critical for new tracker!
- Metalization in 90 nm is low-K, i.e. less parasitic cap
  - Metal density is critical for Z-shift logic
- 90 nm is also essential for low digital power
- 90/65 nm is essential for future GBT

Costs: new facts

- As an example, for a 15m2 dual-layer triggering tracker one needs (at 100% yield):
  - 6,000 5x5 cm2 dual-layer modules
    - 12,000 sensors, i.e. 3,000 6” wafers
      - ~~~@750 $/wafer -> 2.25 M$
    - 216,000 (8x16mm2) 90nm ASICs, i.e. ~~~ 1000 8” wafers
      - ~~~ @2K $/wafer -> 2.0 M$
      - It may well be more convenient to move to 300 mm wafers for this volume! The cost/cm2 is lower in 300mm.
- Bottom line: pixelized architecture changes relative cost importance between electronics and sensors

Plans

1. Specify the functionality of the building blocks and the rough characteristics of the test-chips
2. Allocate work among design groups
3. Synchronize design tools and methodologies
    1. Designers to follow scheduled methodology courses based on new Cadence methodology tools
4. Organize 90nm MPW submissions to prototype some of these blocks
    1. New MLM option are making this more affordable

CERN organized
5 Days Training Course on 130/90 nm Design Methodology

Day 1 => Lead by Ahmed Noeman
- Concept Validation
- Constraint Driven Analog Block Creation

Day 2 => Lead by Ahmed Noeman
- Electrical Parameters Optimization Over Process Variations
- Block IP Characterization Front End
- Functional Verification

Day 3 => Lead by Vincent Cao Van Phu
- CDB IP Import to OA database for IC61 Methodology
- Hierarchical Floorplaning (Virtuoso based)

Day 4 => Lead by Vincent Cao Van Phu
- Block IP Characterization Back End
- DRC (Calibre + Assura workflows)
- LVS (Callibre + Assura workflows)
- Extraction

Day 5 => Lead by Vincent Cao Van Phu
- Digital Block Implementation
- Digital IP Characterization

If interested, email: Kostas.Kloukinas@cern.ch

Other critical technologies

- Packaging = Hybrid = MCM technology is also likely to be on the critical (technical) path
- Candidates are:
  - 3D + ? (even 3D doesn't fly!)
  - C4 based technologies
  - Wire bonded based technologies
  - Various substrates technologies
- One common problem:
  - How to build economically modules of large area
  - *Reminder for non-expert when embarking in new technologies: "Wafer-scale integration" has been a buzzword in the semiconductor industry for at least 20 years, it never worked!*
- Evaluation of different options should be left open until we better understand the real requirements

Conclusion

- Factorize architectural complexity from technological complexity as early as possible
  - Understand basic analog feature of technology
  - Allow optimization in a second phase of circuit parameter
- Teaming (scarce) engineering resources is important
- Allow architects to experiment with different options while engineers are not stuck (and frustrated) with continuous ECOs