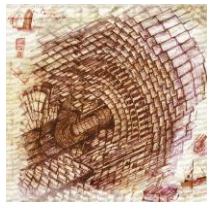


Power Provision for the Tracker Upgrade - Overview, Status, Open Questions

Katja Klein

1. Physikalisches Institut B

RWTH Aachen University

CMS Upgrade Workshop, Fermilab
October 30th, 2009

TWiki: https://twiki.cern.ch/twiki/bin/view/CMS/SLHCTrackerPower
HyperNews: hn-cms-slhc-tracker-power@cern.ch

DC-DC Conversion for the Tracker

A novel powering scheme will be needed ⇒ review process to narrow down options.

Power task force recommended **DC-DC conversion as baseline solution** (Jan. 09).

Serial Powering is the back-up. Reverting to the back-up must remain possible, until feasibility of DC-DC conversion powering scheme is proven.

V_{in} (e.g. 10V)
Power loss in supply cables ~ I^2, reduced by $1/r^2$

→

DC-DC Converter
Conversion ratio r = 2 - 10
$r = V_{in}/V_{out} = I_{out}/I_{in}$

→ **V_{out}** (e.g. 1.2V)

DC-DC converters are currently foreseen for:

1.) Pixel detector at phase-1

2.) Outer tracker at phase-2

DC-DC Conversion for the Tracker

1.) Pixel detector at phase-1 (for details, see talks in pixel meeting)

- Conversion ratio of ~ 2
- Converters installed on supply tube ($\eta \approx 4$)
- Relaxed requirements in terms of size, material, conductive & radiative noise
- Radiation level: fluence $\approx 6 \times 10^{14} cm^{-2} s^{-1}$; dose $\approx$ 200kGy (TDR, 700fb^{-1}, x2)
- Final production version needed in 2011 (?)

2.) Outer tracker at phase-2

- Conversion ratio up to 10 might be needed
- Converters installed close to silicon detectors
- Tight requirements in terms of size, material, conductive & radiative noise
- Radiation level: fluence $\approx 3 \times 10^{15} cm^{-2} s^{-1}$; dose $\approx$ 1.4MGy (TDR, 5000fb^{-1}, x2)
- Proof-of-principle needed for TDR (2012?), final production version needed later

Building Block 1: *the Buck Converter*

- Simplest **inductor-based** step-down converter
  → least number of components
- Can (in principle) provide currents of several Amps with relatively high efficiency - O(80%) - at a high conversion ratio
- Many challenges (technological & system level) ⇒ R&D needed

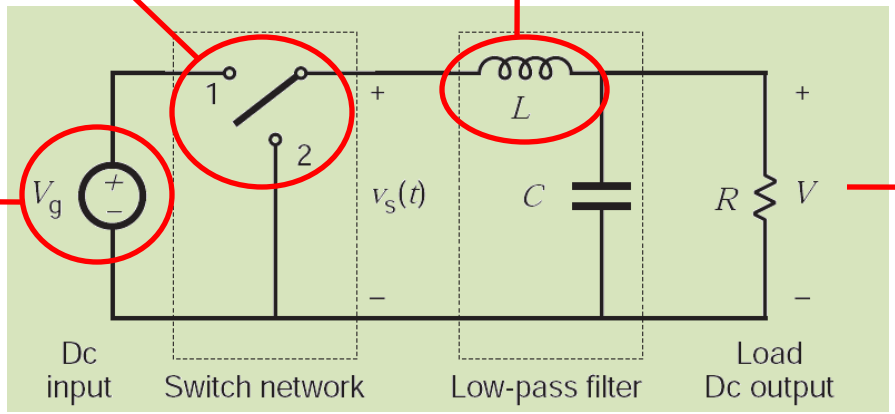
Switching noise

Ferrites saturate for B > ~2T
⇒ air-core inductor needed

bulky

radiates noise

$V_{in} \approx 12V$
⇒ HV-tolerant semi-conductor technology needed
→ radiation-hardness



Efficiency

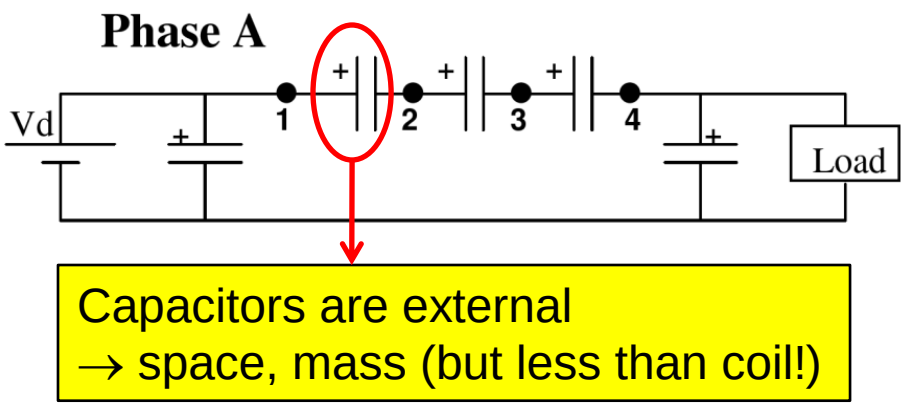
Material budget

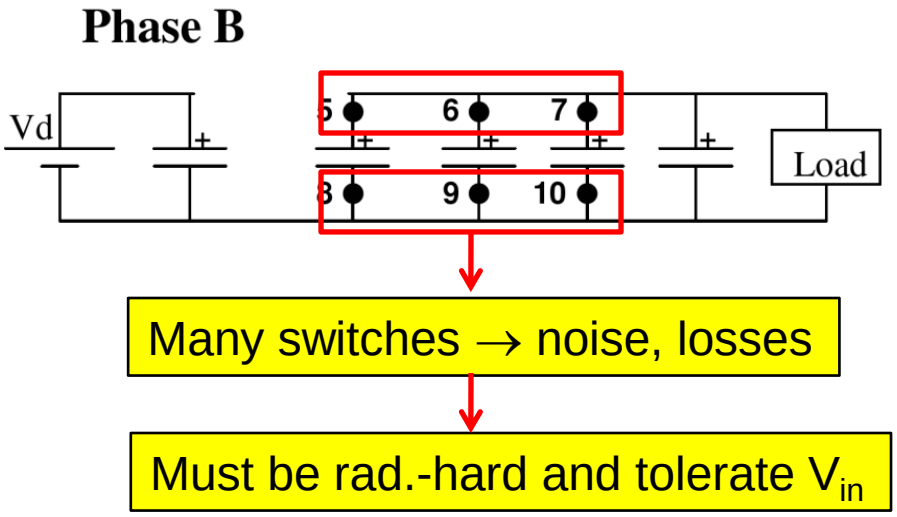
Space constraints

Schematic scheme of a buck converter (feedback control loop not shown)

Building Block 2: *the Charge Pump*

- Based on **switched capacitors** (step-down or step-up possible)
- Simple step-down layout: capacitors charged in series, discharged in parallel
  $\rightarrow I_{out} = n \cdot I_{in}$, with n = number of parallel capacitors
- Cannot provide very large currents
- No regulation ($\Rightarrow$ LDO needed for analog voltage)
- Could be integrated into read-out chip





Semi-Conductor Technology

Requirements:

- Sufficient radiation-hardness
  - For 5000 fb^{-1} and r = 22cm: fluence ≈ 3 x $10^{15} cm^{-2} s^{-1}$; dose ≈ 1.4MGy (TDR, scaled, x2)
- HV transistors for power switches (~ 15V)
- LV transistors for control circuit
- Low transistor on-resistance (→ efficiency)
- Long-term access to a stable technology
- Support & good information flow from foundry

Technology evaluation: F. Faccio (CERN)

- Proton irradiation at PS (24GeV, room temperature, floating bias)
- TID irradiation at CERN X-ray facility (worst-case & switched bias, +27 & -30°C)

Best candidate: **IHP SGB25V GOD** 0.25µm SiGe BiCMOS (IHP, Frankfurt/O., Ger.)

Back-up: **AMIS I3T80** 0.35µm (ON Semiconductor, Phoenix, US)

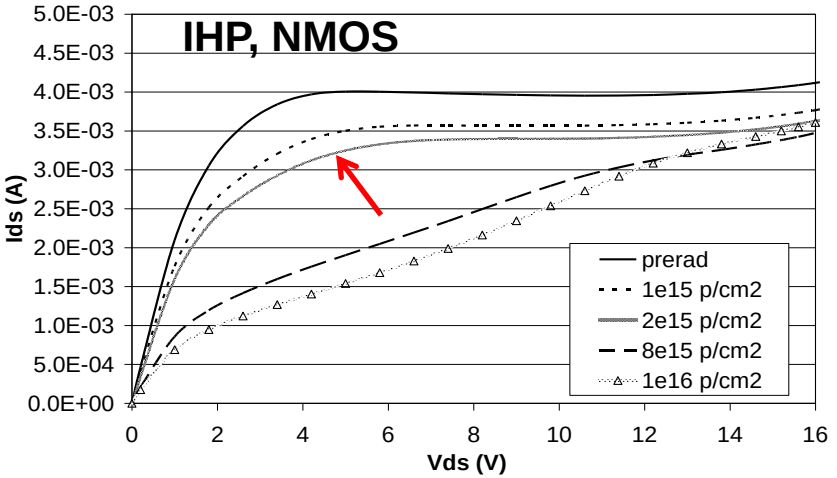
Semi-Conductor Technology

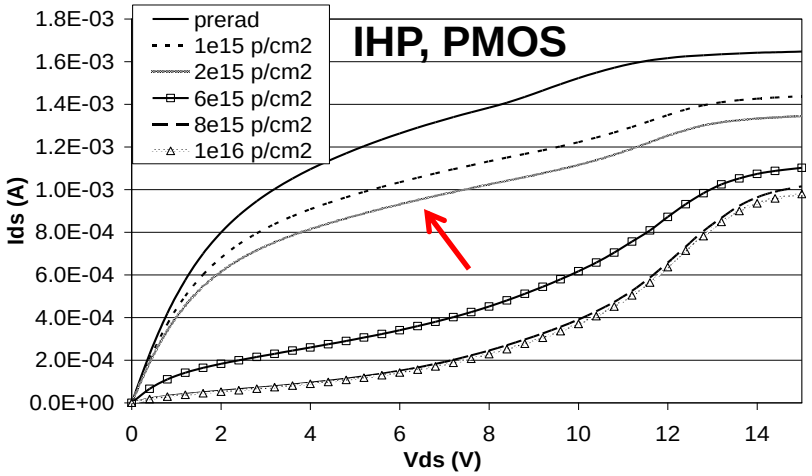
Technology	Tech. node	Transistor type	Max Vds [V]	Max Vgs [V]
A AMIS	0.35μm	Vertical N	80	3.3
		LDMOS N	14	3.3
		LDMOS P	80	3.3
B IHP	0.25μm	LDMOS N	22	2.5
		LDMOS P	16	2.5
C	0.18μm	LDMOS N & P	20	5.5
D	0.18μm	LDMOS N & P	20	1.8
		LDMOS N & P	50	1.8
		LDMOS N & P	25	5
E	0.13μm	LDMOS N & P	20	4.5

F. Faccio, TWEPP09, ATLAS/CMS Power WG

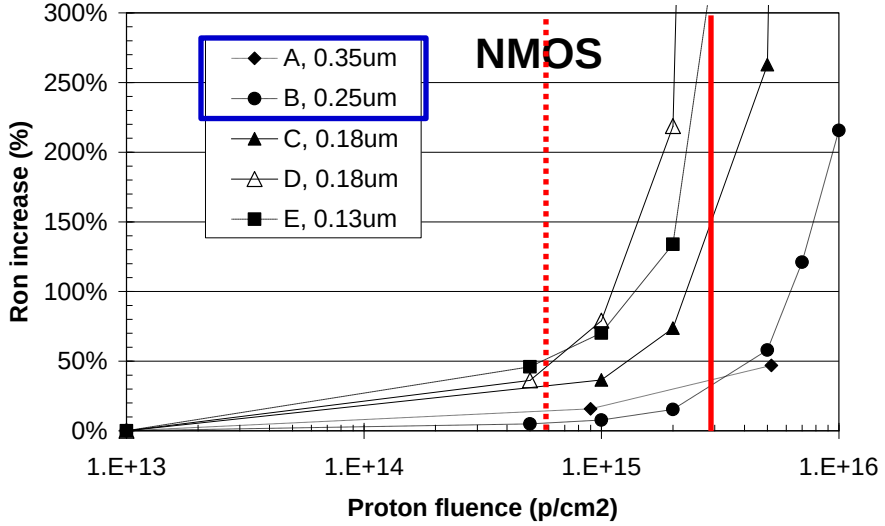
Semi-Conductor Technology

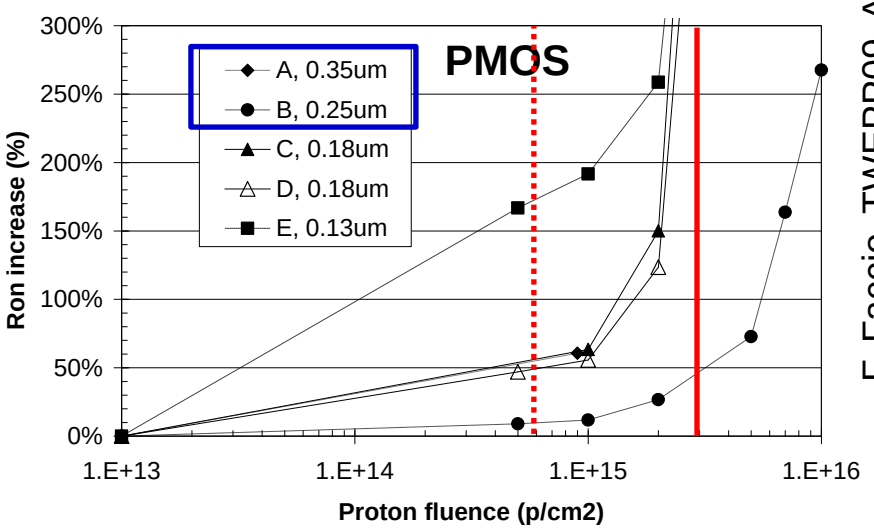
Distortion of output characteristics with fluence:





Increase of on-resistance with fluence:

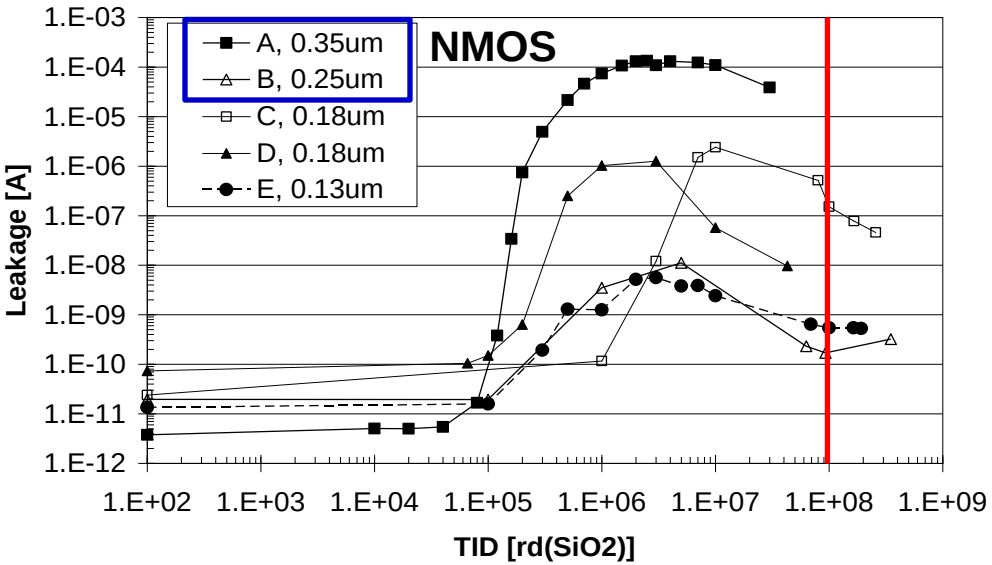




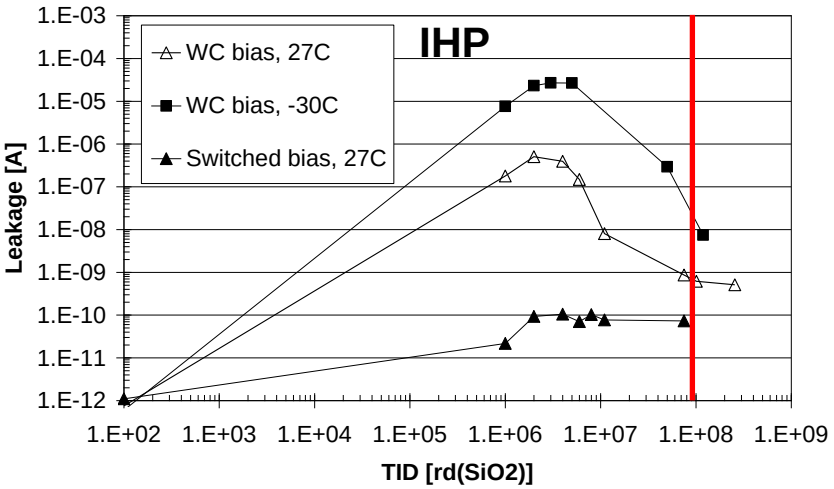
F. Faccio, TWEPP09, ATLAS/CMS Power WG

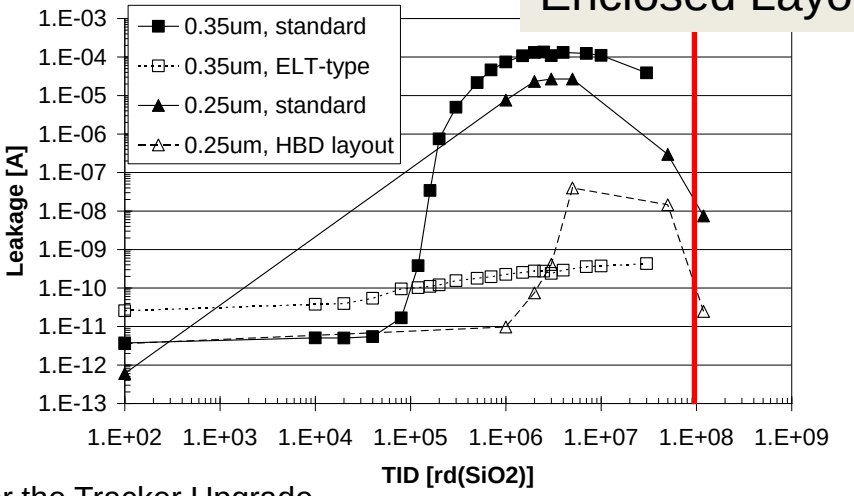
Semi-Conductor Technology

Increase of leakage current with TID (NMOS, worst case bias, room temp.):



Improvement with Enclosed Layouts





Buck ASIC Development

Firmly in the hand of the CERN group (St. Michelis)

Requirements:

- Decent efficiency (~ 80%)
- Delivery of 3-4A
- Conversion ratios up to 10
- Low switching noise
- Control loop stable wrt variations of load, input voltage, temperature
- Robustness, reliability, easy handling
- Small package

First prototype ASIC in IHP technology:

- Back from foundry since September; 9 chips tested at CERN
- Layout seems to be ok; but many basic problems due to “rework“ of wafers from 4 to 5 layers; not usable for CMS
- Next submission in January; expected back in March

Prototype ASICs in AMIS technology: AMIS1 & AMIS2

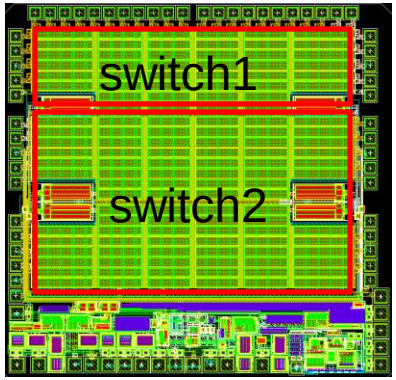
Buck ASIC Development: *AMIS2*

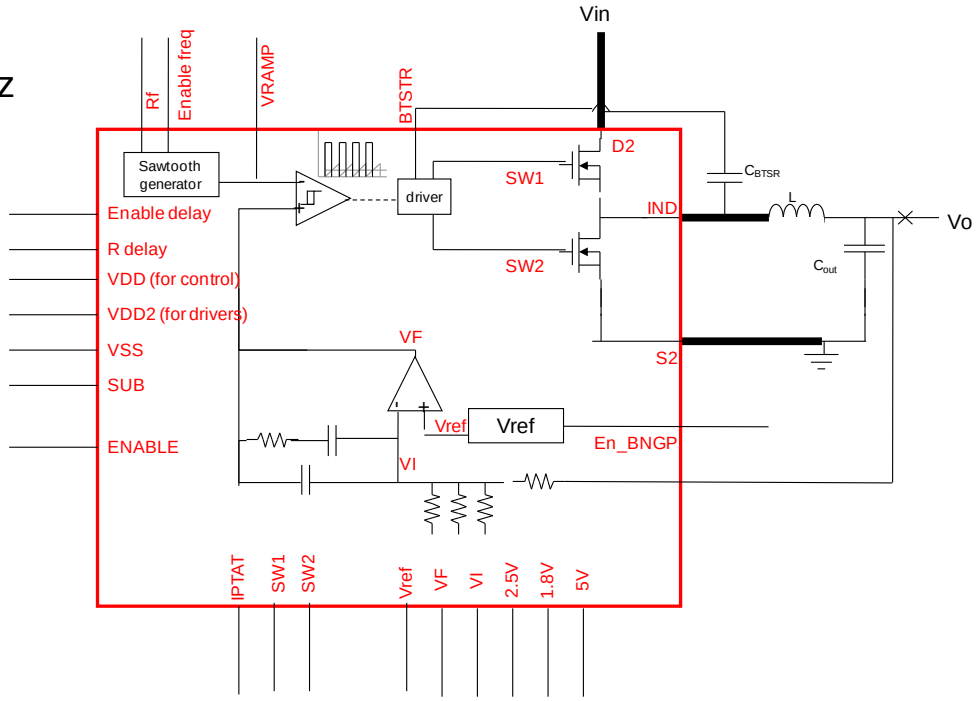
AMIS1 (June 2008): low efficiency due to overlap in open-states of switches

AMIS2 (back from foundry since May 09):

FEATURES

- VIN and Power Rail Operation from +3.3V to +12V
- **Internal oscillator** fixed at 1Mhz, programmable up to 2.5MHz with external resistor
- **Internal voltage reference**
- **Programmable delay** between gate signals
- **Integrated feedback loop** with bandwidth of 20Khz
- Different Vout can be set: 1.2V, 1.8V, 2.5V, 3V, 5V
- Lateral HV transistors are used as power switches
- Enable pin

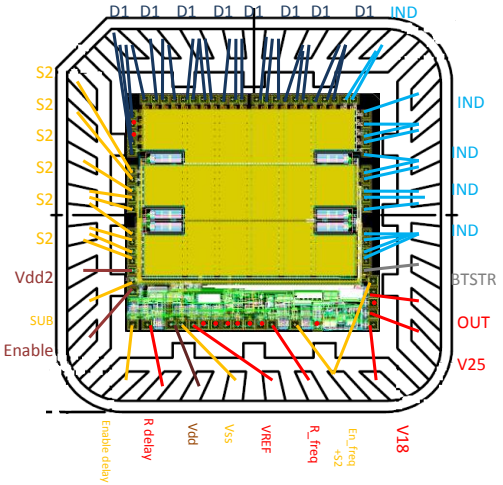


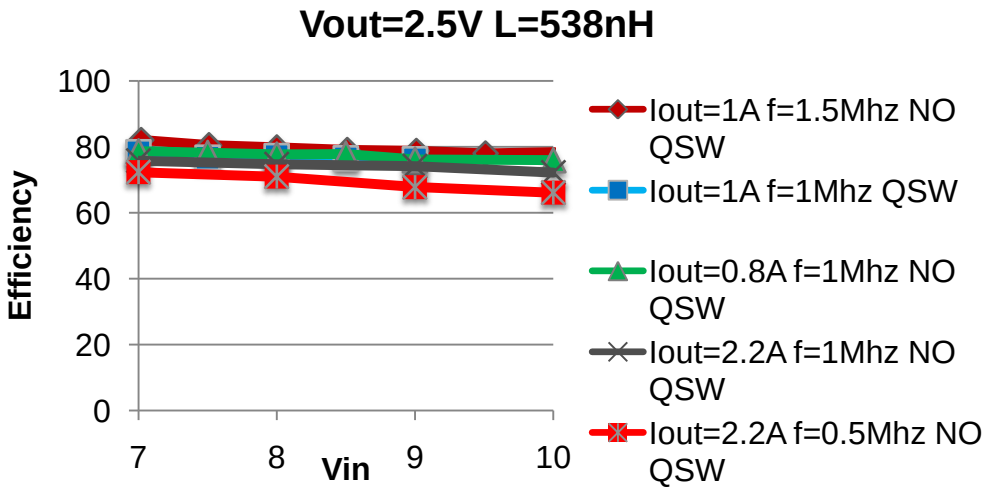


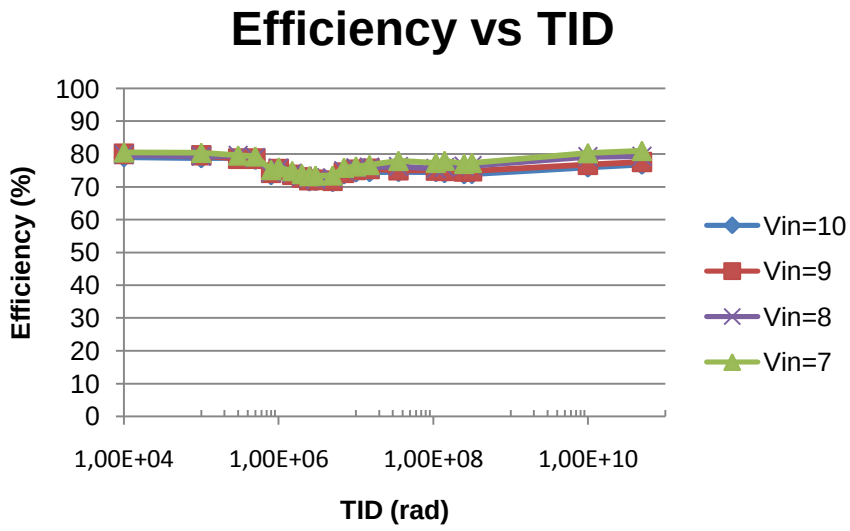
St. Michelis, TWEPP09

Buck ASIC Development: *AMIS2*

- Package size: QFN48 (7mm x 7mm) for testing; bulk of chips will be packaged in QFN32 (5mm x 5mm)
- Efficiency better than AMIS1, but lower than expected from Ron, due to resistive losses in bonds and on-chip routing
- Efficiency vs. TID stable due to compensation between leakage current and threshold voltage shift
- **Issues**: regulation not working for conversion ratios below 2-3; thermal instability of bandgap reference; no protection features







DC-DC Buck Converter Development

RWTH Aachen University (L. Feld, W. Karpinski, K.K. et al.)

Talk by R. Jussen

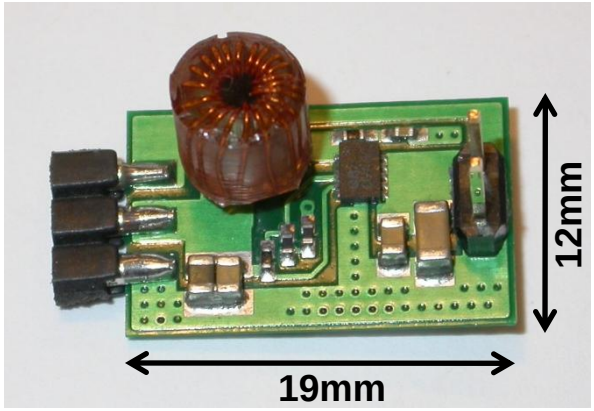
Ingredients:

- PCB
- ASIC (commercial or CERN)
  - 15 boards manufactured with AMIS2 QFN48 (3 chips already broken)
  - Waiting for AMIS2 QFN32, hope to receive ~ 30 (will provide boards to US colleagues)
- Air-core inductor (custom)
- Filter networks
- Sometimes additional circuitry (e.g. provision of VDD for AMIS2)
- Possibly shielding

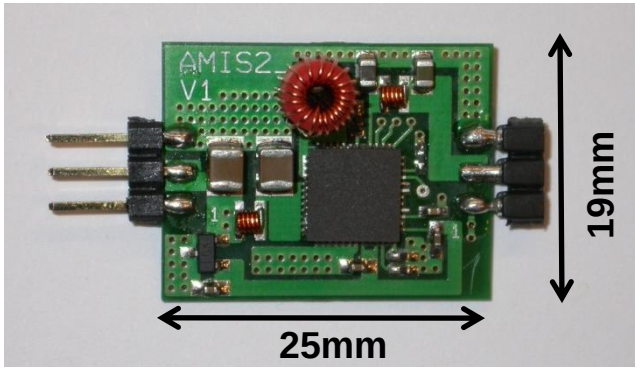
Requirements:

- High efficiency (no losses due to filters, ESR of coil etc.)
- As small & light as reasonably possible!
- Low switching noise
- Low radiative noise (clever coil design or shielding)
- Thermal management

Buck Converters: Size & Mass



“AC2-StandardC“
Enpirion chip EQ5382D
Standard filter caps
Area: 2.3cm^2
Height: 10mm
Weight: 1g



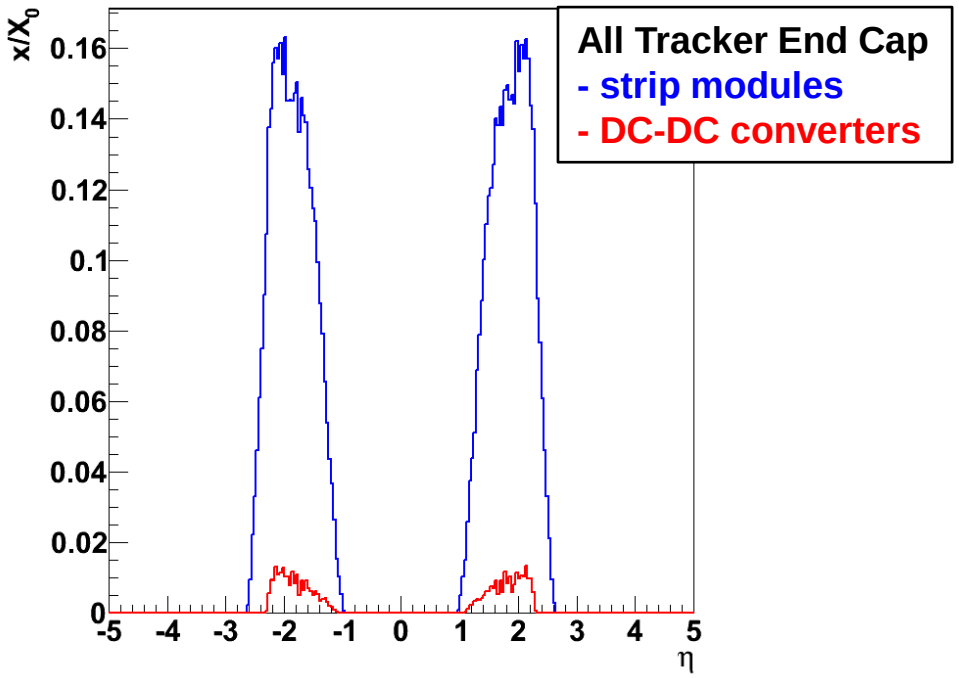
“AC-AMIS2-V1“
AMIS2 chip with QFN48
Pi filters at in- and output
Area: 4.75cm^2
Height: 10mm
Weight: 2.5g

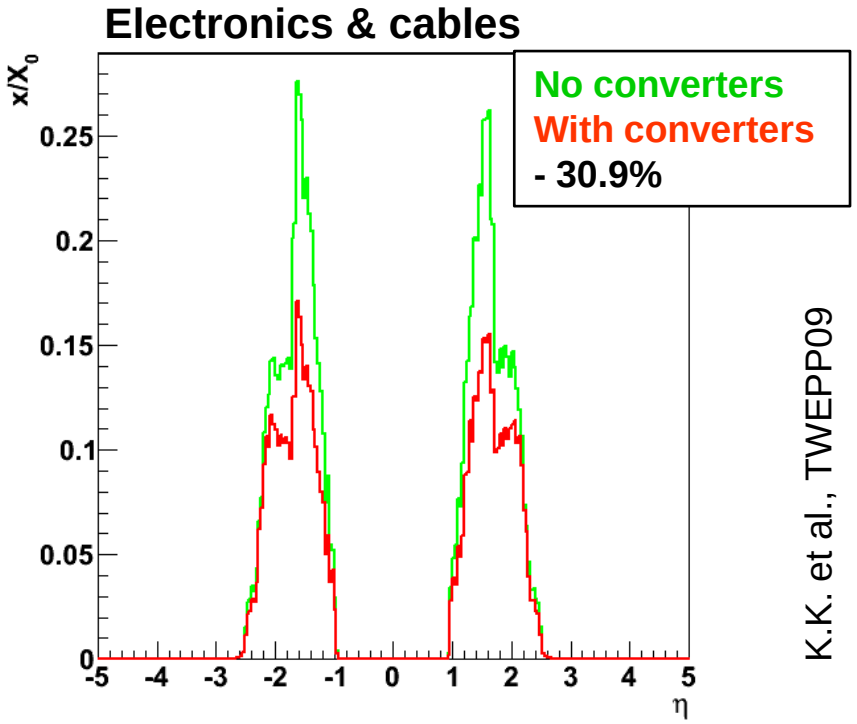
- Prepare for objects with 2-4cm^2 area, 10mm height, 1-2g weight
- Further savings possible, but typically on cost of efficiency or noise performance

K.K. et al., TWEPP09

Buck Converters: Material Budget

- Simulation within CMSSW based on current tracker layout
- One AC2-StandardC converter per TEC module; located on FE-hybrid
- Contribution from DC-DC converters ≈ 10% of current strip modules
- Savings in cables & PCBs estimated for conversion ratio = 8 and 80% efficiency
- Within our model, can save 30.9% in TEC “electronics & cables“ and 8.0% in total





Buck Converters: Noise

RWTH Aachen (strips), Fermilab/Iowa/Mississippi (pixels), CERN (ATLAS strips)

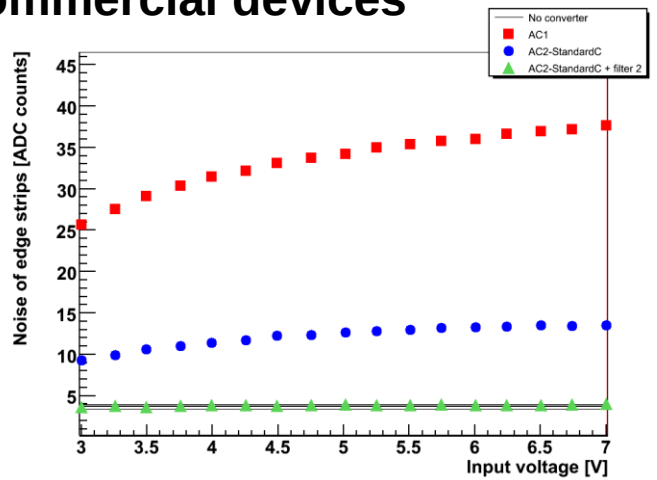
Tasks

- System tests with commercial and custom DC-DC converters
- Understand susceptibility of module prototypes to conductive noise
- Understand noise coupling mechanisms
- Design and optimization of filters to reduce conductive noise
- Inductor engineering to reduce radiative noise
- Design of shielding

A lot of experience already gained with commercial devices

Talk by R. Jussen

- **No converter**
- **AC1 (2008)**
- **AC2-StandardC with Mini Toroid**
- **AC2-StandardC with Mini Toroid + pi-filter**



Charge Pump Development

- Some initial work by PSI (B. Meier) & Florence (G. Parrini), not followed up
- M. Bochenek (Krakow/CERN) developes charge pump blocks for ATLAS
  - step-up (0.9V $\rightarrow$ 1.6V) and step-down (2V $\rightarrow$ 0.92V)
  - 130nm
  - Step-down: 60mA nominal output current, 92% efficiency (in simulation)
- Potential usage in CMS Binary Chip (V_{ana} (1.2V) $\rightarrow$ V_{dig}(0.9V), 3:4)
  - Worries about substrate noise, number & size of passives
  - Could/should be bypassable
  - Would certainly be a step forward
  - Have to come to a decision this year
- Use in track trigger chips not envisaged

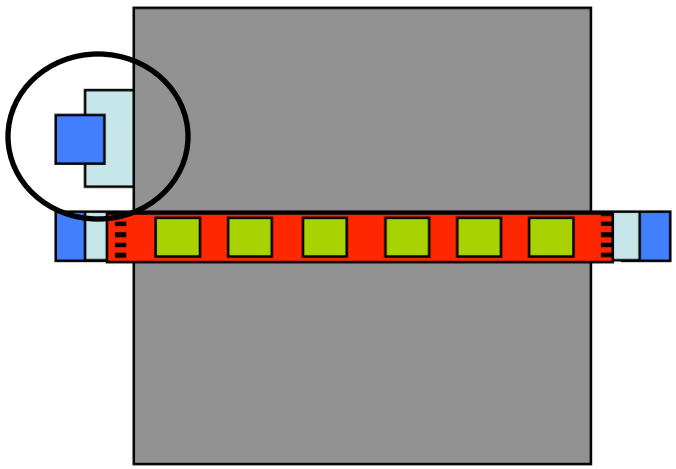
M.Bochenek. et al., TWEPP09

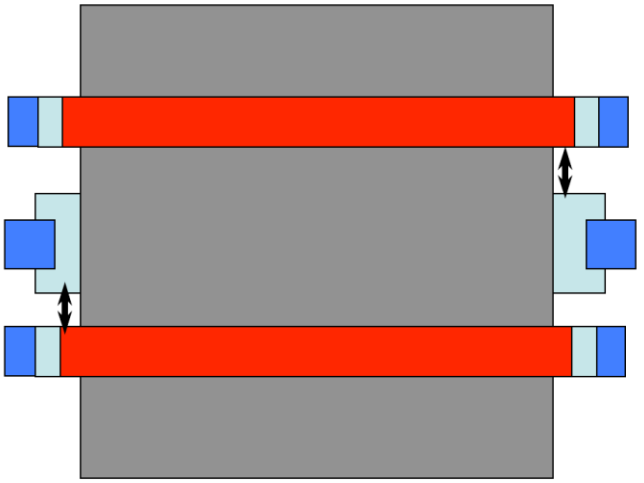
Converter Integration

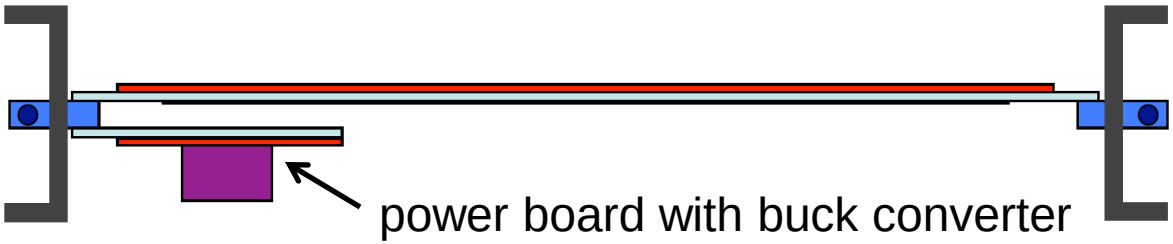
- Same buck converter for tracking and trigger layers
- Converter located close to silicon modules
- Integration with separate PCB
  - space constraints (no motherboards, small FE-hybrids)
  - decoupling of converter development from hybrid/module development

DC-DC Conversion for the Tracking Layers

- DC-DC buck converter located on **separate "power board"**, below the sensor
- 1 board per FE-hybrid (P = 0.8W) [symmetry reasons only]
- Board connected to cooling block (diss. power is low → could be same as hybrid)
- If $V_{dig} < V_{ana}$: 1 on-chip charge pump per CBC, or 1 charge pump on power board







TUPO, June 17th
Sketches by Duccio

DC-DC Conversion for the Trigger Layers

Conversion ratio: up to 10 might be needed
(depends on total power consumption & e.g. limits for current in cable channels)

Estimated FE-Power consumption per module:

pT-module a la Geoff: ~ 1.7W
pT-module a la Sandro: ~ 2.5W ?
} 1 buck converter

Vertically integrated hybrid module: up to 9W $\Rightarrow$ 2-3 buck converters

However, $V_{ana} \neq V_{dig}$ $\Rightarrow$ (at least) 2 buck converters per module (charge pumps no option)

Integration onto FE-hybrid will be very difficult (space)
Long barrel double stack proposal: integration into beam structure

DC-DC Conversion for the GBT

- Typically 1 GBT per trigger module
- 1 GBT needs P = 2-3W
- Two operation voltages
  - 2.5V for GBTIA & GBLD; P(2.5V) ≈ 700mW
  - 1.2V for other parts
- Two options:
  - 2 buck converters per GBT
  - 1 buck converter per GBT for 1.2V; plus step-up charge pump for 2.5V

- In total (at least) 3 converters per trigger module:
  - buck or charge pump for 2.5V for GBTIA & GBLD
  - buck for 1.2V for rest of GBT + analogue FE-power (1/3 or 1/4 of total)
  - buck for 0.9V for digital FE-power
  - could all sit on one PCB

Open Questions

- Performance limits of buck converters (practical experience needed): maximal output current and conversion ratio, at what efficiency?
- Usage of charge pumps
  - e.g. to provide the digital voltage for CBC
- Bias voltage
  - LICs are rated for 600V
  - Higher bias voltage highly desirable for charge collection efficiency
  - Compatibility of LICs and connectors with higher voltages to be understood

- Uncovered topics
  - Power supplies: specification, contact with company, qualification, ...
  - Cables & PP1: compatibility with new requirements, design of components that need replacement, connection scheme etc.

Summary

- Buck converters will be used by pixels at phase-1 & outer tracker at phase-2
- Semi-conductor technology plus back-up identified by CERN group
- Prototypes in both technologies being developed at CERN, teething troubles
- Continous converter development at Aachen, using most recent custom chips
- Understanding of noise issues growing & mitigation strategies developed
- Integration on separate power boards foreseen
- Good progress, but still a long way to go