Pt Module Design Considerations

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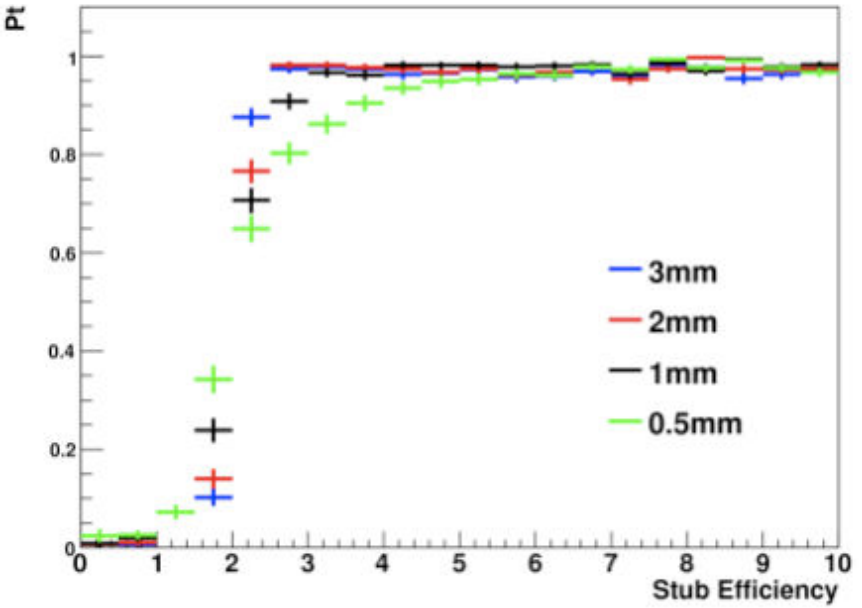
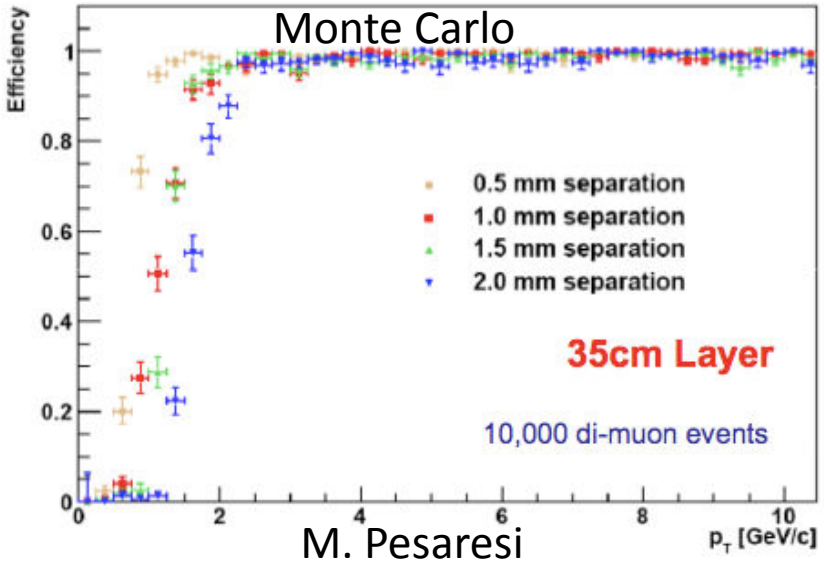
- The Pt module embodies an attempt to engineer unprecedented levels of intelligence into the front end of a silicon tracker. This talk is an attempt to take a look at the tradeoffs that we will eventually have to face when considering a final design.
- There are some basic parameters that control the design – Pt threshold, and data rates and relation to layer spacing
- Use “back of the envelope” calculations to get a feeling for some of the tradeoffs – but detailed MC are crucial
- Bring up issues for discussion and debate
- Full disclosure – I am a proponent of a 3D design R&D project so most of my thinking is in that context

Layer Separation

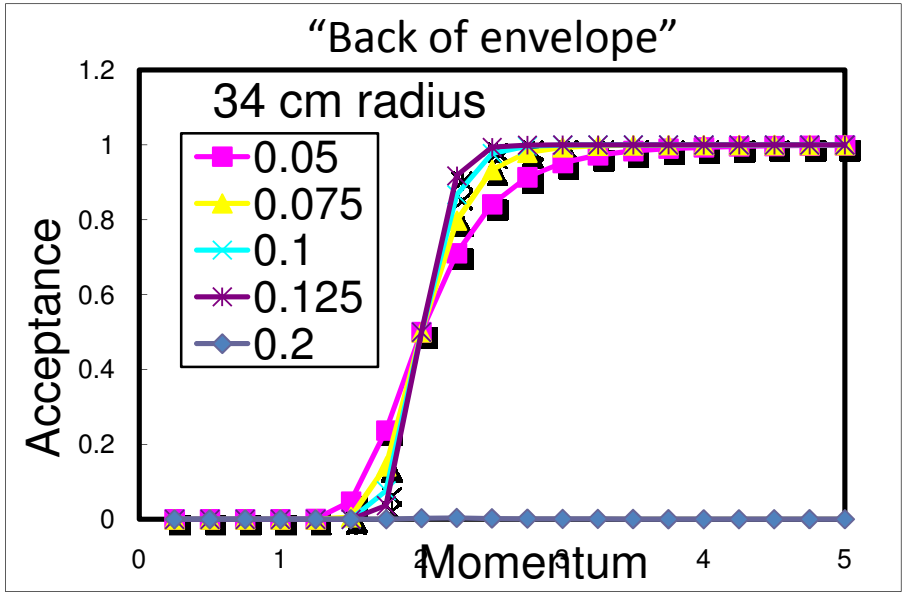
- Layer separation and detector resolution directly affect the sharpness of turn-on curves
- Assume 100 μm pitch, 100μm/sqrt(12) gaussian resolution and calculate the overlap of hits on two.
- Sharpness of the curve will tend to saturate, indicating "optimal" separation for a given Pt threshold



L. Fields

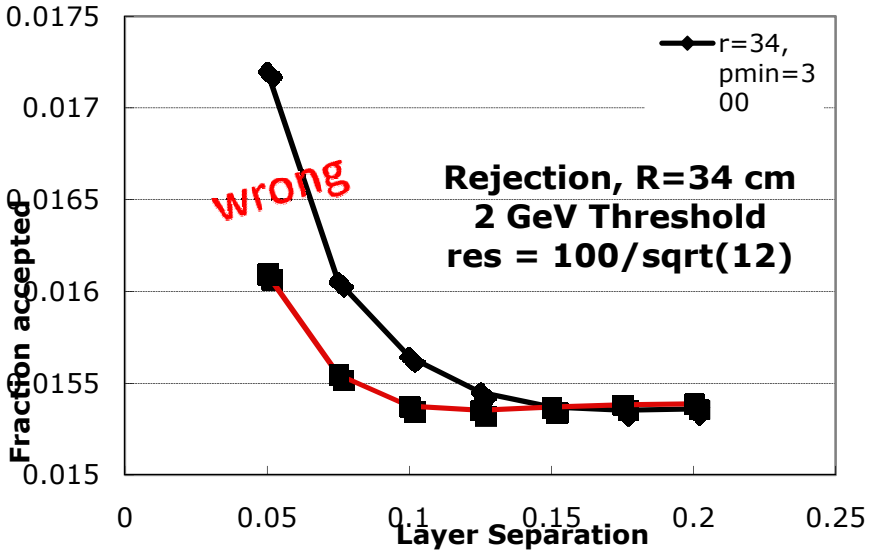


M. Pesaresi



Rejection

- To estimate this I folded a $1/Pt^8$ inclusive Pt spectrum and plot the result vs layer separation.
- This turns out to be wrong
- L. Fields sees almost flat stub distribution for 0.5-3 mm
  - Contributions from accidentals and conversions.
  - Rate – 5 Mhz x ~3 = .34/cm^2/xing about 3x lower than assumed 1/cm^2
  - Stubs ~ .3 Mhz x 3 = 0.02/cm^2/xing
- I assumed x10 to x20 rejection over 1/cm^2 at 35 cm at 2 GeV threshold (0.1 or .05 /cm^2/xing)



Peak TTP Rates (in MHz/cm2):

2 GeV Stub/Tracklet Threshold ↓

Stack Sep →	0.5mm	1mm	2cm	3cm
SimHits	5	5	5	5
Digis	9	9	9	9
Clusters	4	4	4	4
Stubs	0.3	0.3	0.27	0.25
Tracklets	0.1	0.15	0.18	0.17

1 mm Stack Separation

L. Fields

Stub/Tracklet Threshold →	1 GeV	2GeV	3GeV	5GeV
SimHits	5	5	5	5
Digis	9	9	9	9
Clusters	4	4	4	4
Stubs	0.9	0.3	0.14	0.06
Tracklets	0.3	0.15	0.05	0.01

Radial and Pt Dependance

- To first order the track can be considered in the small angle approximation:

$$y = b + \phi \times r + k \times \frac{r^2}{2}, \frac{\partial y}{\partial r} = \phi + k \times r$$

2 GeV tracks,
1 mm layer offset

Radius	Doublet hit offset(μm)
34.00	408.6
50.00	600.6
104.00	1248.6

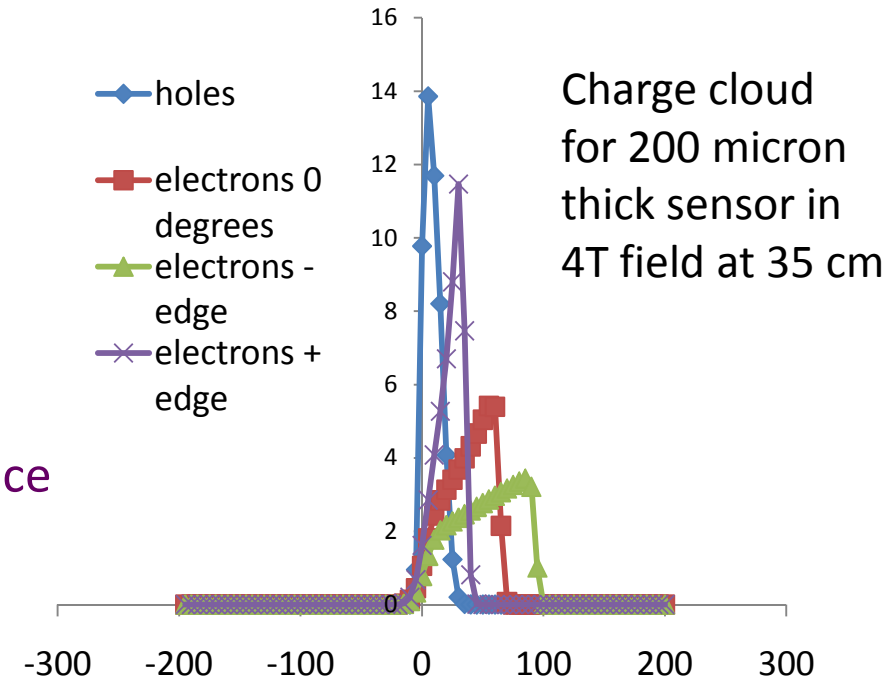
The sensitivity of hit separation to curvature is proportional to r.

- Of course cost also increases with radius
- For z we can use

$$\sigma_z = \sigma_{hit} \frac{\sqrt{1 + \frac{r_i}{r_o}}}{1 - \frac{r_i}{r_o}}$$

R-Phi Pitch

- Another way to improve the sharpness of turn-on curves is to improve sensor resolution.
  - More power in front-end
  - More complex algorithms in front end chips
- If electrons are collected charge can spread over several strips
  - Shape depends on angle of incidence
  - Better hit resolution due to increased charge sharing
  - Need to have algorithms aware of charge sharing and position in detector



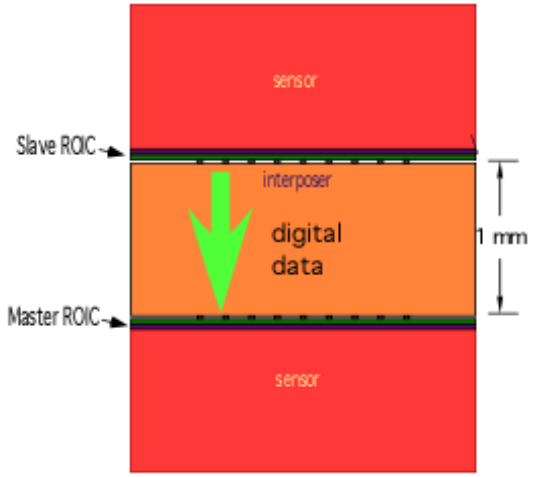
Charge cloud for 200 micron thick sensor in 4T field at 35 cm

- 100 micron pitch, hole collection seem to be good assumptions at the moment

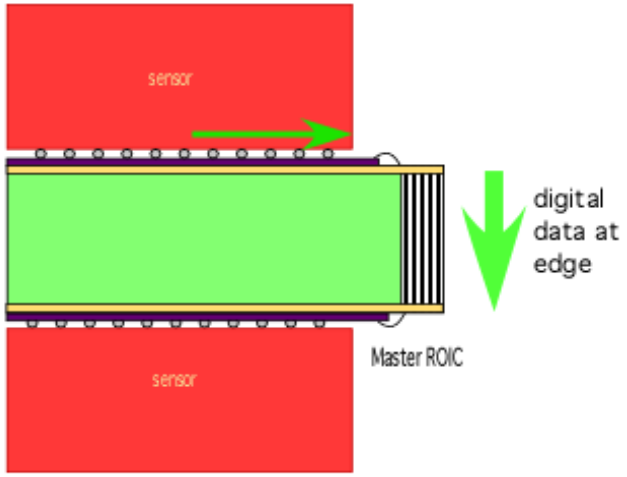
Top to Bottom Data Transfer

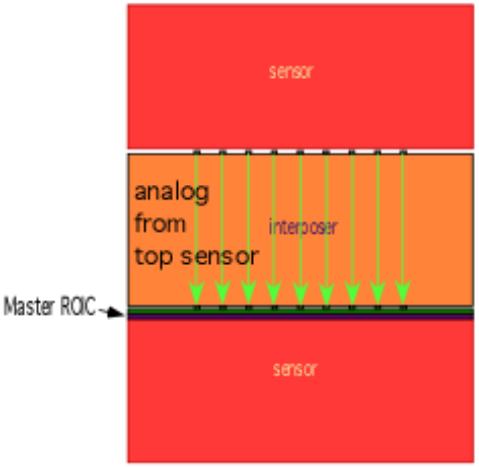
- Options:
  - Digital transfer through interposer
  - Digital transfer at edge
  - Digital transfer through PCB (conventional)
  - Analog transfer through interposer
-

Vertical solutions

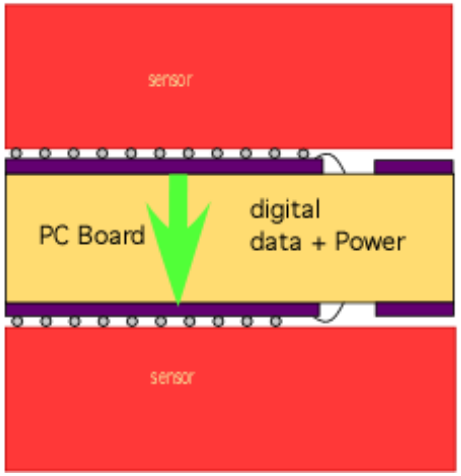


Horizontal solutions





Model explored in 3D R&D program



Models explored in Pt module R&D program

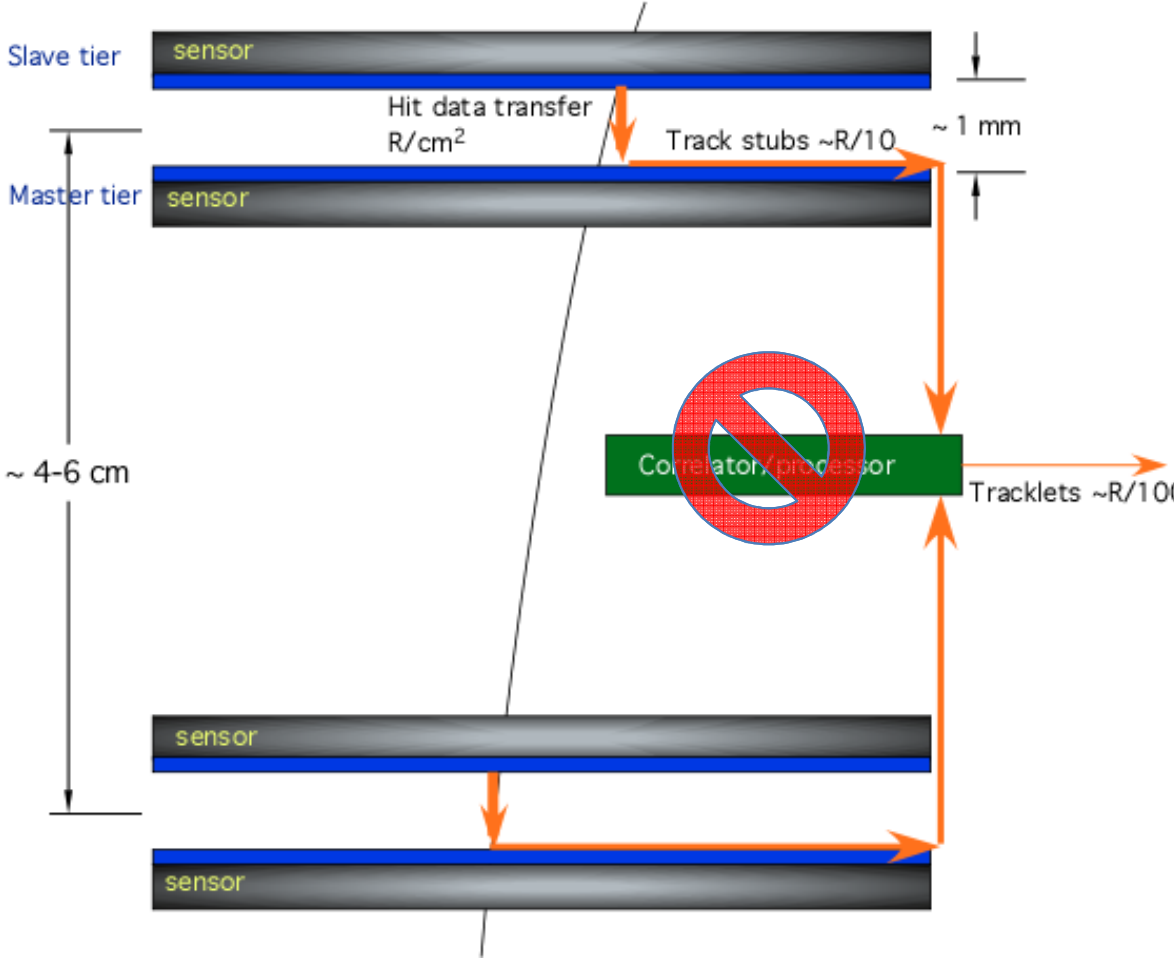
Data transfer options

- Digital transfer
  - Chips must encode/decode hit addresses (power?)
  - Data must be routed at high speed through interposer/PC/interconnect
    - Noise injection into sensor many 100 Mhz busses-> current mode transmission or balanced differential signals.
    - Neighbor chip connections will be needed in phi and z
    - Does data need to be buffered? Where?
- Analog transfer from top sensor
  - Possible in 3D design
  - Requires long (~1 cm) z strips in top tier (limit interposer vias)
  - Allows for local processing of correlations (no address decoding)
  - More front-end power due to more capacitive top->bottom connections
  - Single layer may simplify cooling
  - Allows design with only one tier of chips ($£¢¥)

Z Resolution

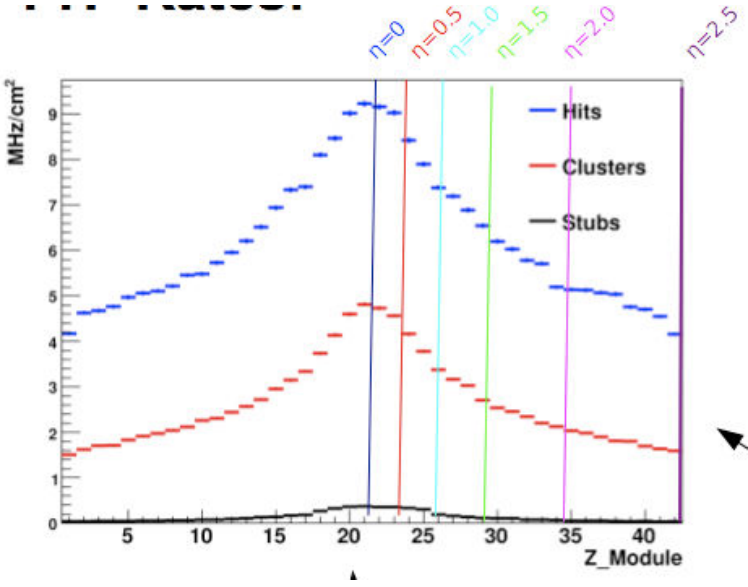
- Any trigger based on multiple track objects will benefit from additional z resolution to limit candidate primary vertices
- Z resolution is most relevant for correlations between doublet hits (stubs are too close)
  - 3D design assumes ~1 cm strips on top and 1 mm on bottom
  - Top strip (logical) length sets the interposer density in 3D design
- We assume ~1-2 mm z pitch is possible for both conventional and 3D designs. Smaller pitch is possible, but assembly is more complex, technology challenging, and power may be a problem.
- What is needed for trigger rates? Rate for many triggers is likely to be linear in z resolution.

Tracklets?



- A design which combines stubs into local tracklets can substantially reduce data flow by making layer separation several cm
- However any missing hit on any of the 4 layers will loose the tracklet
- This lack of redundancy is a serious problem which probably means that all stub data needs to be transferred.
- Tracklets must be formed off-detector (Marvin)
- In that case the only way to reduce the off-module rate is to improve the rejection raise Pt threshold. The actual values needed should be carefully considered and the MC understood in detail

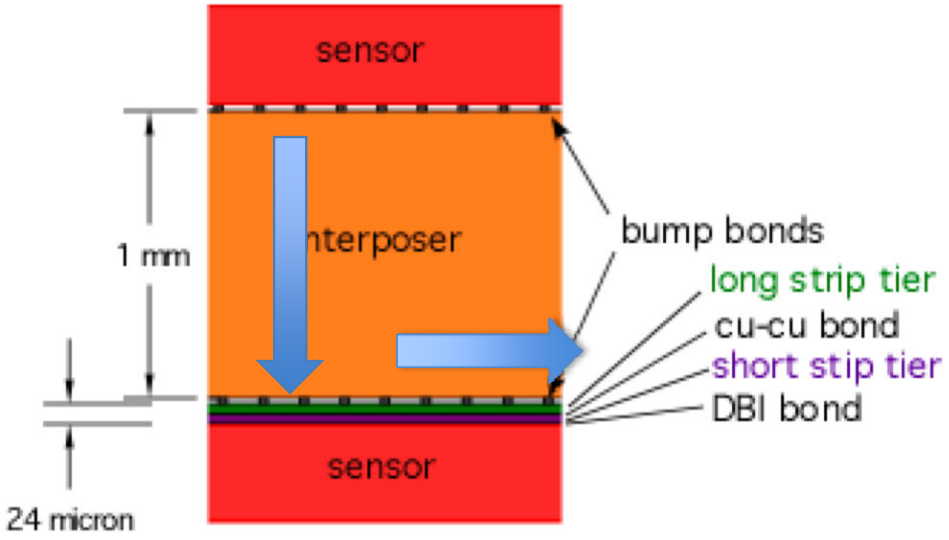
Module Size



L. Fields, 2 GeV thresh
1 mm separation 34 cm

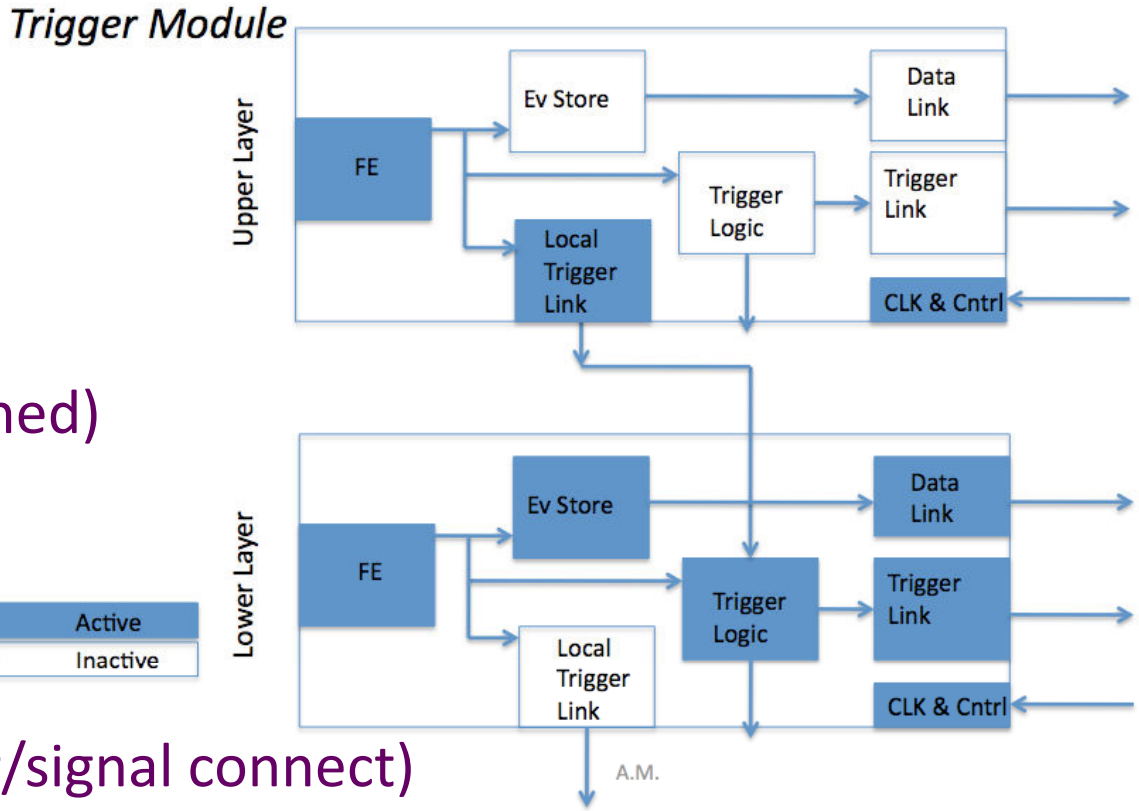
- Maximum dictated by ~10 x 10 cm sensor size
- Edge readout limits width to ~2x IC size, about 5 cm x Z
- A 10 cm tiled design would require ~16 ICs/layer
  - What is the yield of the fabrication process (>99%/IC)?
  - Must use known good die
  - What is the yield of the die as a function of die size
  - Can parts be reworked?
- Occupancy decreases with z – change logical module size to minimize link power?
- How is power supplied and signals routed from inner chips?
  - PC board (mass?)
  - Passive components (bypass caps)
- How is the module cooled?
  - Must the interposer be thermally conductive?
  - CO_2 lines above and below doublet?

In-Module Transfer



- High rate bus in close proximity to sensors
- All designs but analog transfer require transfer of some digital data at full hit rate within the module
  - Proper electrical shielding will be crucial
- In 3D design both horizontal and vertical transfers must be integrated
  - Extra PC board or flex layers
  - Integration of horizontal bus on interposer
  - Other technical solutions (twisted wire …)
  - Bump bonds include both analog and digital transfer
  - Guess about 200 bumps/cm^2 half analog

Power



- Components
  - Analog front end (reasonably well defined)
  - On chip trigger logic
  - Clock control
  - Local trigger link (across PC/interposer/signal connect)
  - Data link off chip to optical drivers
  - Optical driver power
  - L1 accepted events readout from EV store
- There is a *lot* of wiggle room in the power estimates

Analog Power

- The analog front end needs to have low enough noise and fast enough risetime.
- Both depend on the transductance of the input transistor, which in turn depends on current (power)

$$e_n^2 = \frac{4kT}{g_m}, \quad f_0 = \frac{g_m}{2\pi C_0} \quad (Spieler)$$

$$g_m = \frac{I_d}{kT/e} \quad (for\ weak\ inversion)$$

- They also depend on C_{load}
- We can scale analog power for current chips to lower load capacitance and smaller feature sizes of 0.13 and 0.09 micron processes.
- Add capacitance for interposer for 3D design (~0.5 pf)
- Look at long (1cm ~ 1.5 pf) and short (1mm ~ .2 pf) strips for 3D design

Digital Power

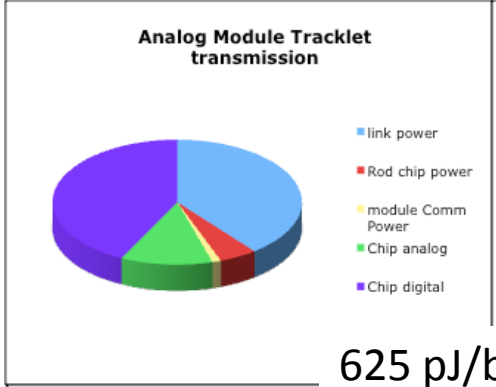
- Base chip power (14 mW/chip) (RH, MM) $P = k \times freq \times C_{\text{int}} V^2$
- Chip hit processing power (assume 180 pJ/hit) ???
- Data transmission from master to slave (0.5 pf)
- Data transmission to optical interconnect or tracklet chip 12 cm x .8pf/cm
- Optical link power (z=0 module)
  - N links = (Gbits/sec)/(Gbits/link)
    - 1 module (10x10 cm) (3.2 Gb link) if tracklets used
    - 2/module if stubs are transmitted
    - *ASSUMING x20 STUB REJECTION*
  - Link picojoule/bit numbers range from 50 – 625
  - Link power will dominate if tracklets are not used and current GBT power is assumed

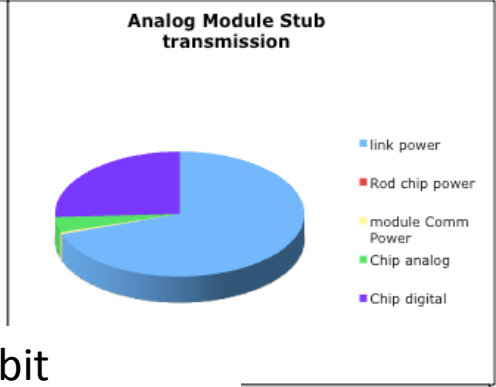
Chip Power estimates

- Survey of RO Chip estimates – single layer only
  - ~ 80μW/pixel→0.032 W/cm^2 (GH)
  - ~ 0.026 W/cm^2 (MM+RH)
  - ~ 0.034 W/cm^2 (RL one analog tier 3D)
  - CMS pixel chip 0.194 W/cm^2 ~ 7x more
- Not including 1/(.75-.8) penalty for DC-DC
- Perhaps some single/double counting of layers/module
- All assume power savings at 90 nm
- Estimates are not completely independent.
- Scaling with pixel size is complex due to
  - Effects of lower load capacitance on analog
  - How does digital processing load scale with pixel size?

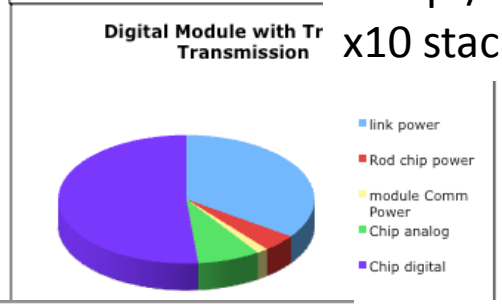
Power Summary I

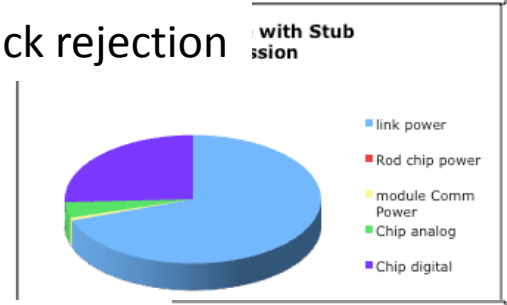
Vary stub level rejection assuming
1 hit/cm^2/xing (10->20) and
GBT link power/bit
Current GBT bandwidth (3.2 Gb/link)



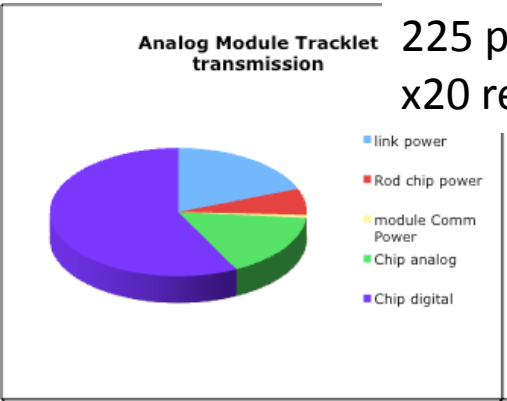


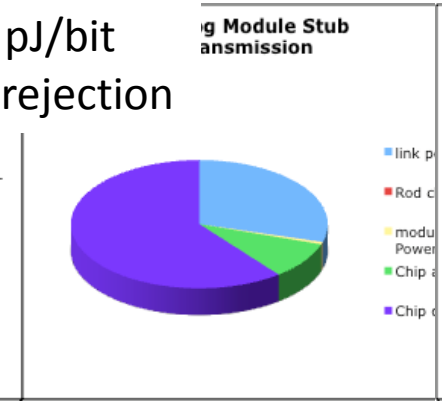
625 pJ/bit
x10 stack rejection



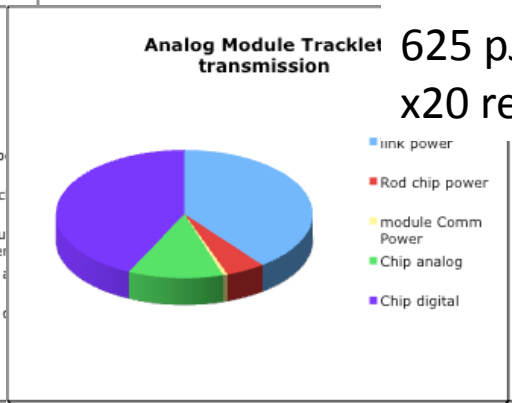


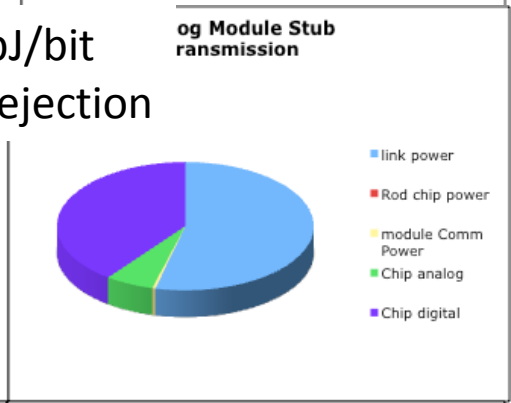
225 pJ/bit
x20 rejection

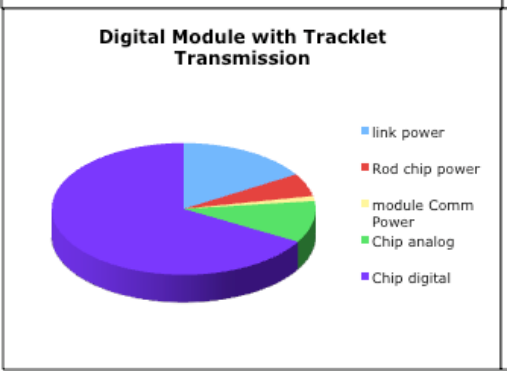


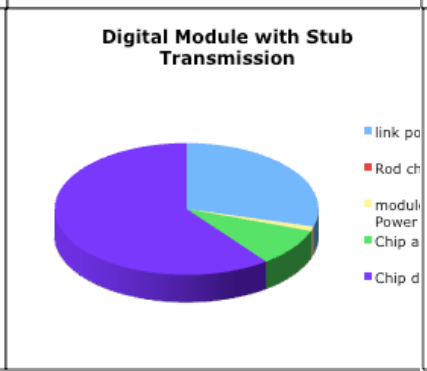


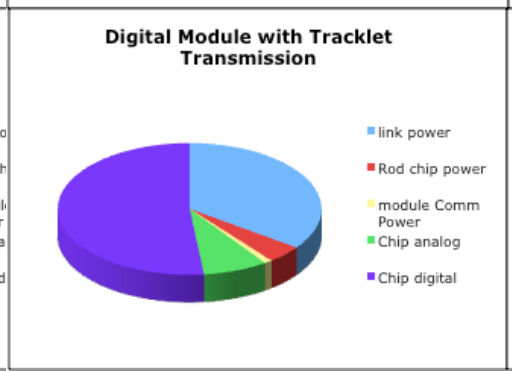
625 pJ/bit
x20 rejection

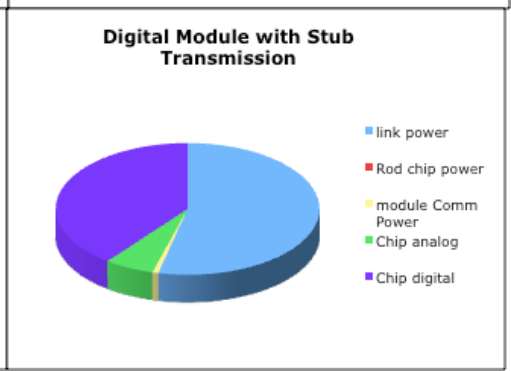






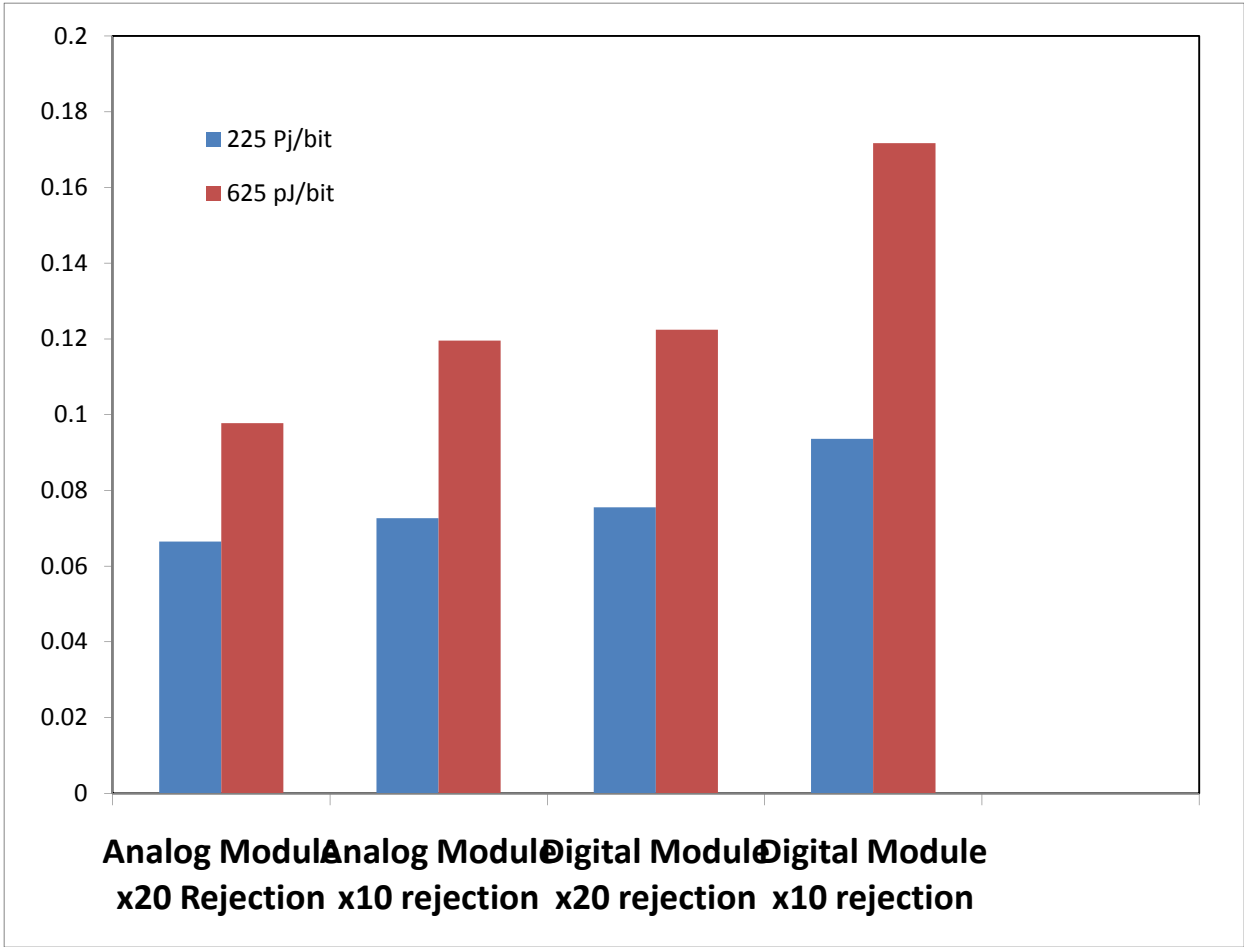






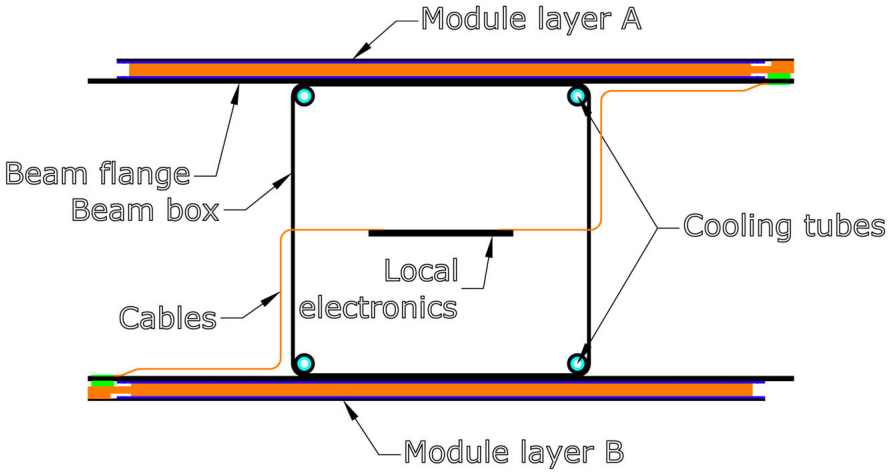
Power Summary II

- One particular model – many variables are not terribly well prescribed
- Not including 1/(.75-.8) penalty for DC-DC
- # of GBT=rate/3.2Gbit



Thermal considerations

- 5x smaller power dissipation/area than CMS pixel chip means cooling is simpler
- Simple 1d thermal calculation for 3D module design – heat generation at top or bottom tier
  - Both tiers $\Delta T < 1$ degree x ? For variation in local flux
  - GBT DC-DC 2W *local* heat source, is a concern and would be best placed off-module
  - DC-DC converters 20-25% of total load
- Real problem is 2D with local coupling to cooling pipes, DC-DC converters and GBTs – being started

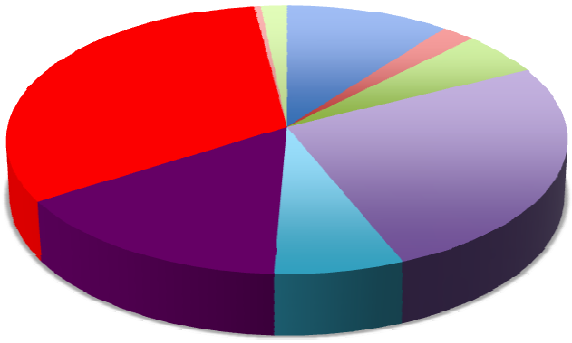


Clearly not a 1D problem
heat spreading is important

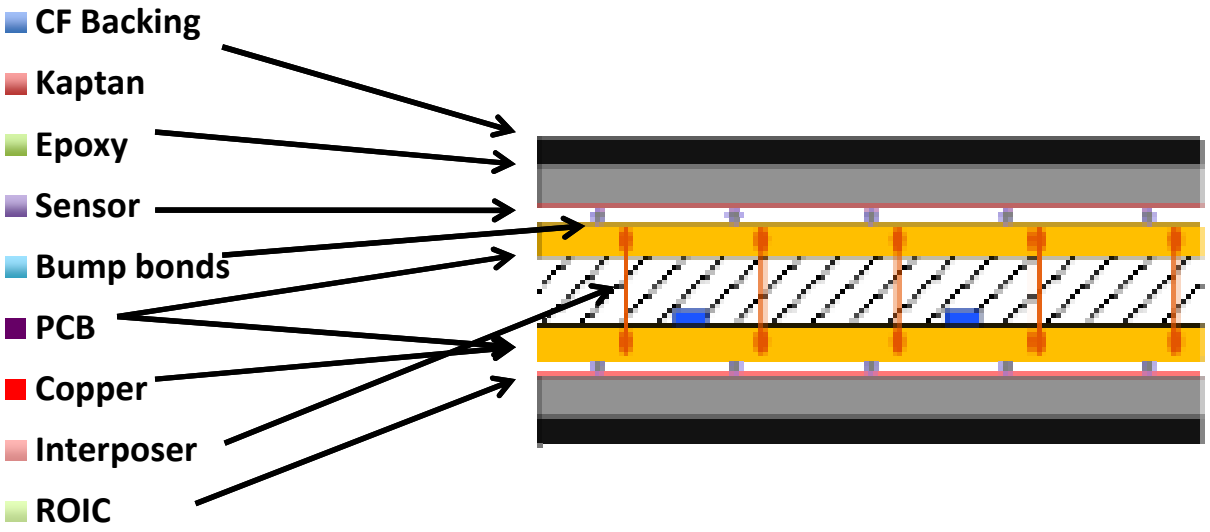
	Type	Thickness		Thermal Property			Thermal
	CF Backing	200	microns	0.1	w/m deg C		0.002
	Kaptan	50	microns	0.37	w/m deg C		0.0001
	sensor	200	microns	148	w/m deg C		1E-06
	Bump bonds	100	microns	0.35	w/m deg C	x area	0.0003
	PCB	200	microns	0.5	w/m deg C		0.0004
	silicon						
	Interposer	500	microns	37	w/m deg C	x area	1E-05
	PCB	200	microns	0.5	w/m deg C		0.0004
	Bump bonds	100	microns	0.35	w/m deg C	x area	0.0003
	ROIC	25	microns	340	W/M^2	generated	
		200	microns	148	w/m deg C		1E 06
	sensor						
	kaptan	50	microns	0.37	w/m deg C		0.0001
	CF Backing	200	microns	0.1	w/m deg C		0.002

Mass

- Ongoing work (Duccio, Lenny) much more detailed.
- Picture based on thermal model ~1.6% (DC-DC converter and GBT not included)
  - Copper 2x D0 HDI density, low mass interposer
- How to minimize mass (in 3D design)
  - Minimize copper
  - Low mass interposer
    - Local bypass of power lines (?)

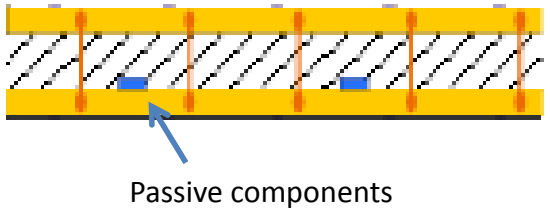


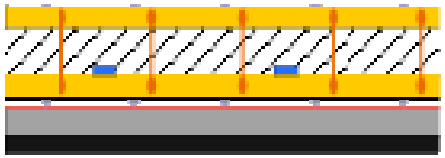
Radiation Length

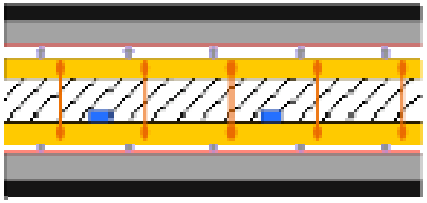


Module Fabrication

- Use 3D analog module as example
  - Assemble interposer with electronics
    - Bed of nails test?
    - Sacrificial test connector?
  - Test components
    - Test ROIC die on production wafer
    - Test sensors
  - DBI bond die to sensor (industry)
  - Glue sensors to bottom CF, Kapton (HV connection)
  - Bump bond interposer to bottom sensor
    - Test bottom assembly
  - Bump bond sensor/interposer to top sensor
    - Test full module

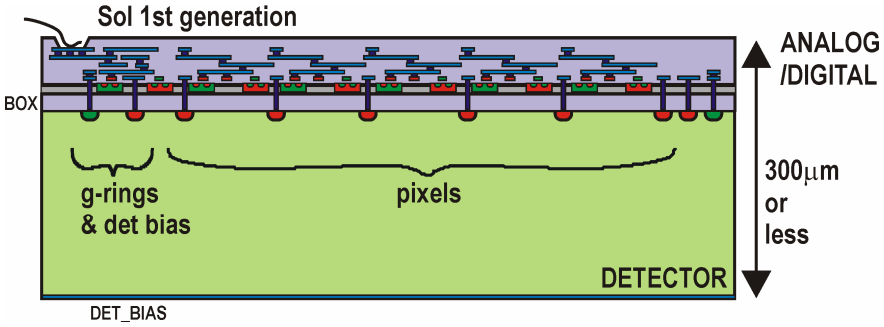


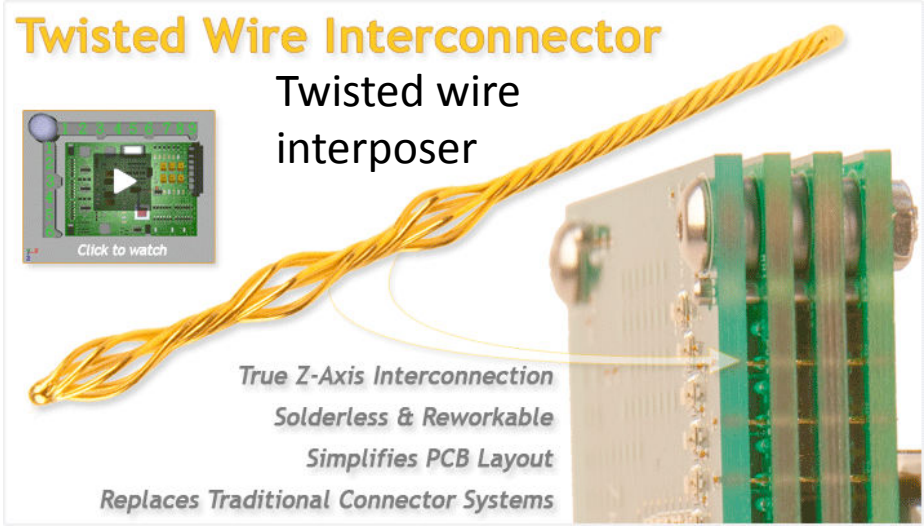




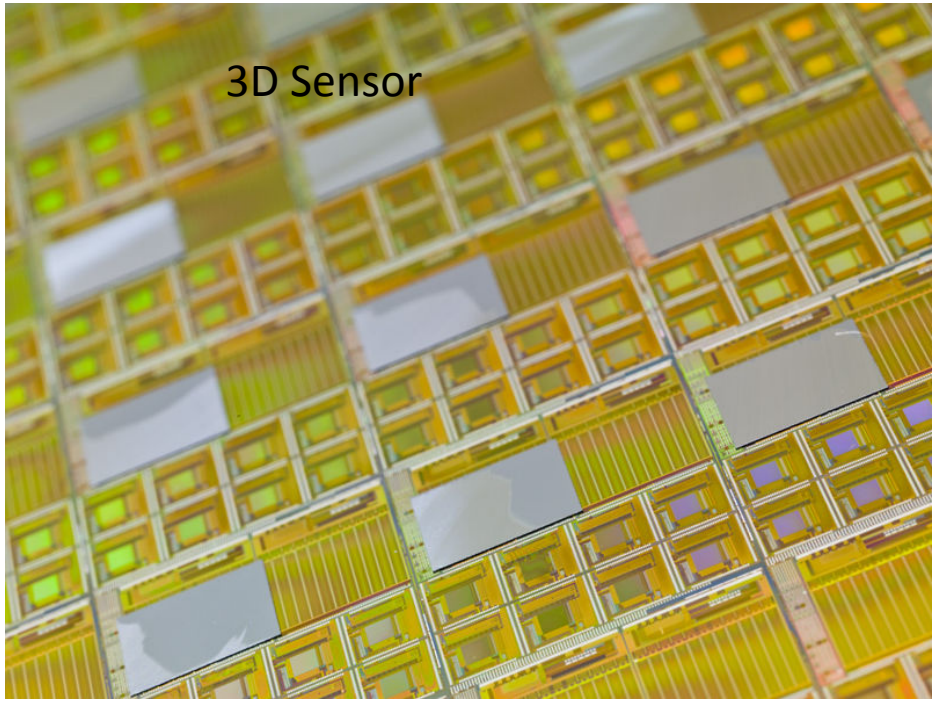
Parts for Vertical Module

SOI or MAPS

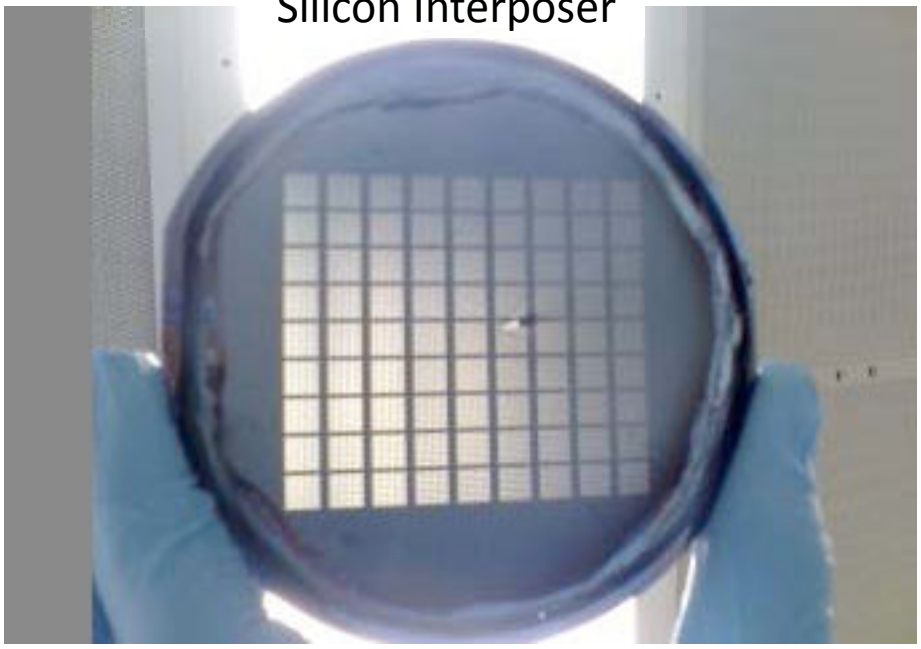




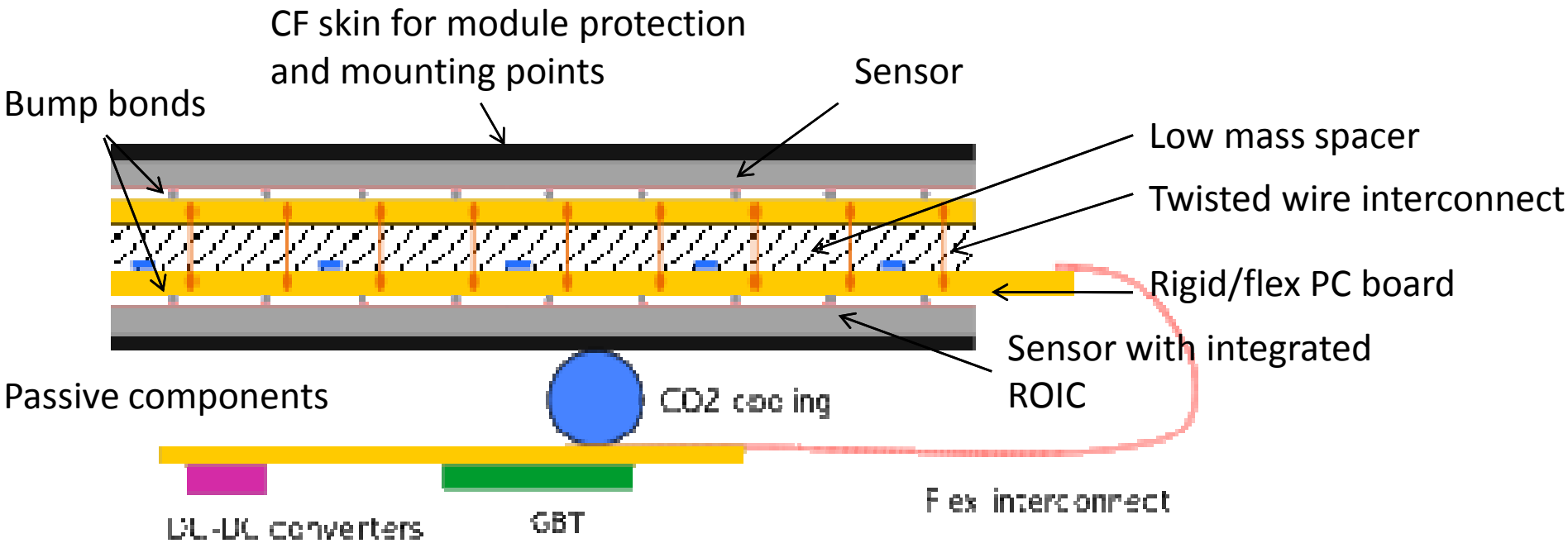
3D Sensor



Silicon Interposer



Vertically Interconnected Module conceptual design



Physically robust module

Power hungry parts near cooling

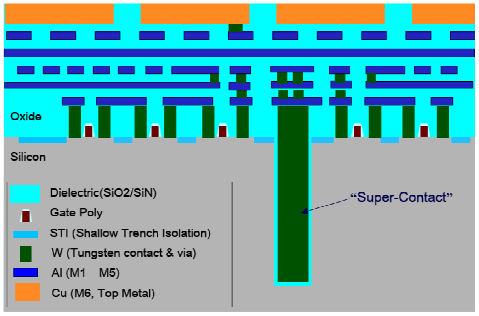
Provides electrical interconnect paths which should be conventional

- Needs 2 layers of bump bonding
- Relies on vertical interconnection of sensors and ICs

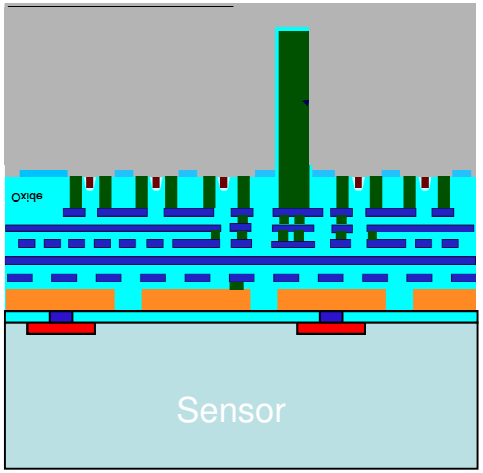
Conclusions

- Module design ideas are taking form – both vertical and horizontal
- We will need to refine the design parameters in the near future
  - Stub rejection – correlation algorithms
  - Algorithm and connectivity – how much is hard-wired?
  - Pt threshold
  - Need for tracklets?
  - Power consumption – IC design modeling
  - Power consumption – optical link power
  - Power consumption – data bandwidth
  - Z segmentation
- There are many uncertainties but I believe prospects for a robust, low mass module are good – many encouraging developments in the last few months.

Building a Trigger module with 3D

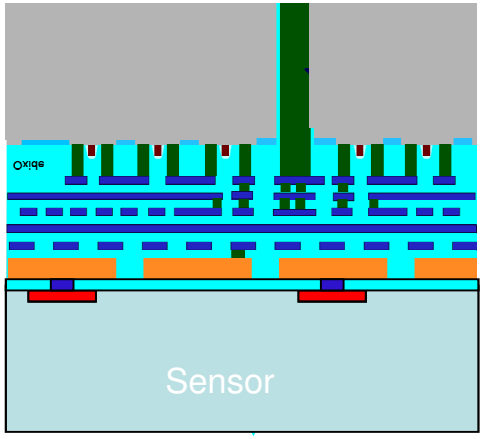


Readout IC wafer with TSV from foundry

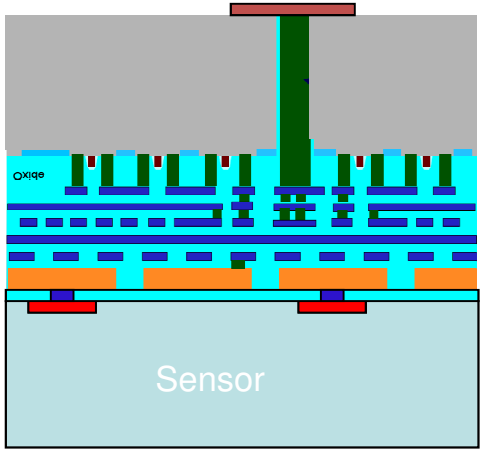


DBI bond

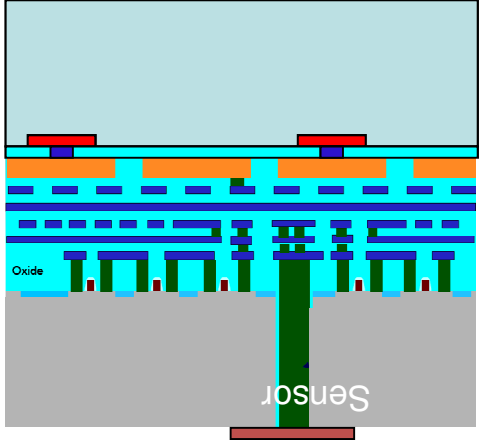
Oxide bond diced ROIC to sensor Wafer.

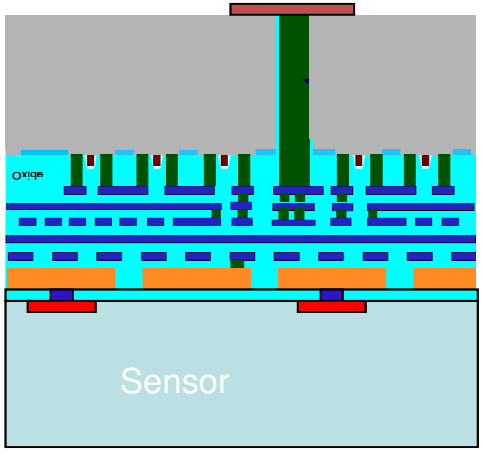


Thin to expose TSV



Contact lithography provides
Access to topside pads for vertical data path





Bump Bond module

VICTR Logic and Floorplan