GBT use in HCAL

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GBT = GBTX (serdes chip) + transceiver parts + fibers

GBTX is the baseline for the upgraded HCAL RM and is a candidate for the upgraded HCAL CCM.
GBTX specifications are not yet set in stone...

We will likely use (and customize ?) the **transceiver parts:** laser, Laser Driver, optical receiver, Trans-Impedence Amplifier.

Our baseline is to keep the existing **fibers**, although it may be possible to add some fibers for the CCM [Alexander Singovski].

Data Encoding (1/2)

- GBTX has an encoding scheme ("Reed-Solomon") that consumes 27% of the bandwidth for error correction. This is motivated by the radiation levels of SLHC.
- The encoding provides an equivalent gain in optical power
- With no radiation the code gain is 2.5 dB

The "40 MHz" 120-bit GBT frame

HEADER bits	Internal control bits	Ext. control bits	User Data bits	Encoding bits
4	2	2	80	32

Data Encoding (2/2)

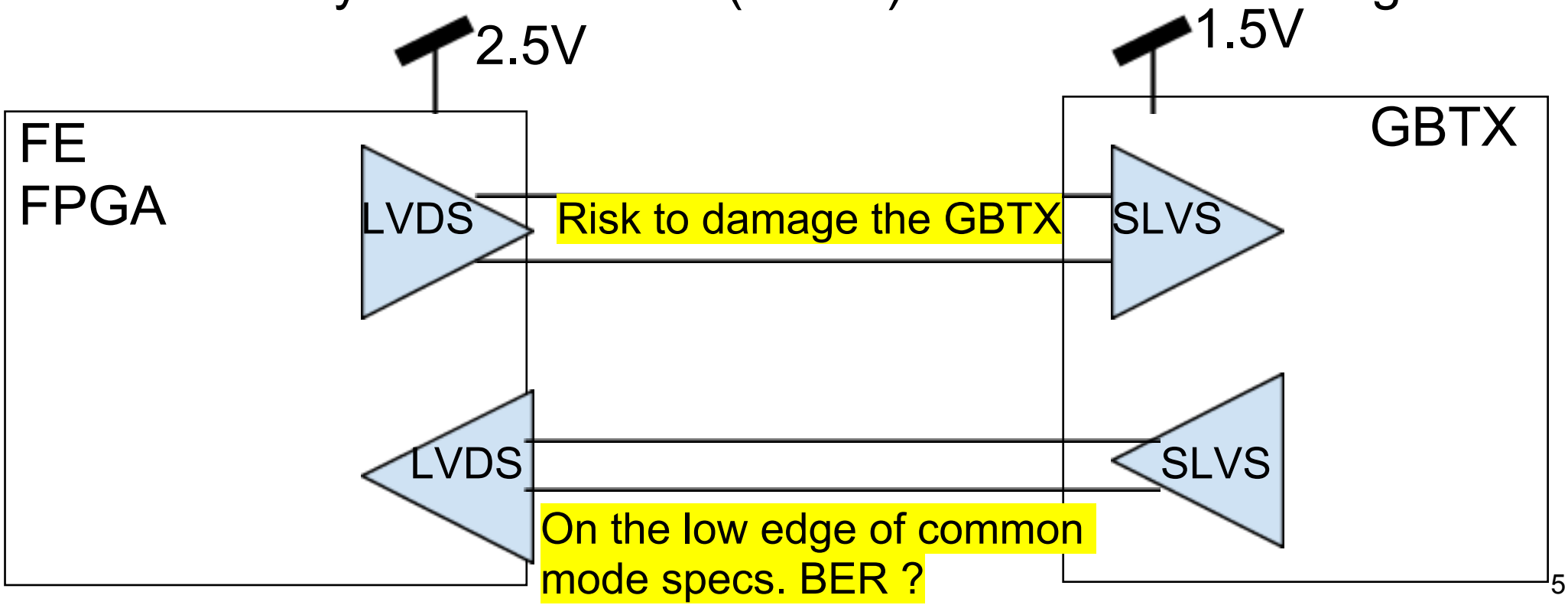
- After request from HCAL et al., the GBT group is considering the programmable option to **by-pass the encoding**, so the user will have almost the full bandwidth (~114bit @ 40 MHz)
- Using more bandwidth may complicate the interface to the rest of the FE (if there are not enough parallel bits)
- **Application for the data link**: we should use the encoding in the areas most exposed to radiation (HF, HE, ...). We could disable it in HO (lowest radiation, not in the trigger)
- Use the encoding in the CCM downlink has no disadvantages.

Interface with the Front End (1/3)

Electrical Interface: GBTX pins use the **SLVS** differential standard:

- Low-level = 0 mV
- High-level = 400 mV

Today´s FPGA do not support this standard ---> **problem.**
It could actually talk to FPGAs (LVDS) with near-zero margins:



Interface with the Front End (2/3)

SLVS interface problem.

What are our options ?

1) Use early GBTX prototypes to **test** the interface with FPGAs and assess the reliability of the interfac. This requires to establish more collaboration with the GBT group and maybe sharing costs.

2) If the test result is not satisfying, then we need to plan for a separate **level-translator chip**.
The GBT group has certainly the know-how to do it, but not many resources.
Maybe other groups could be interested.

Interface with the Front End (3/3)

Also the **logical interface** with the GBTX is more complicate than the GOL interface.

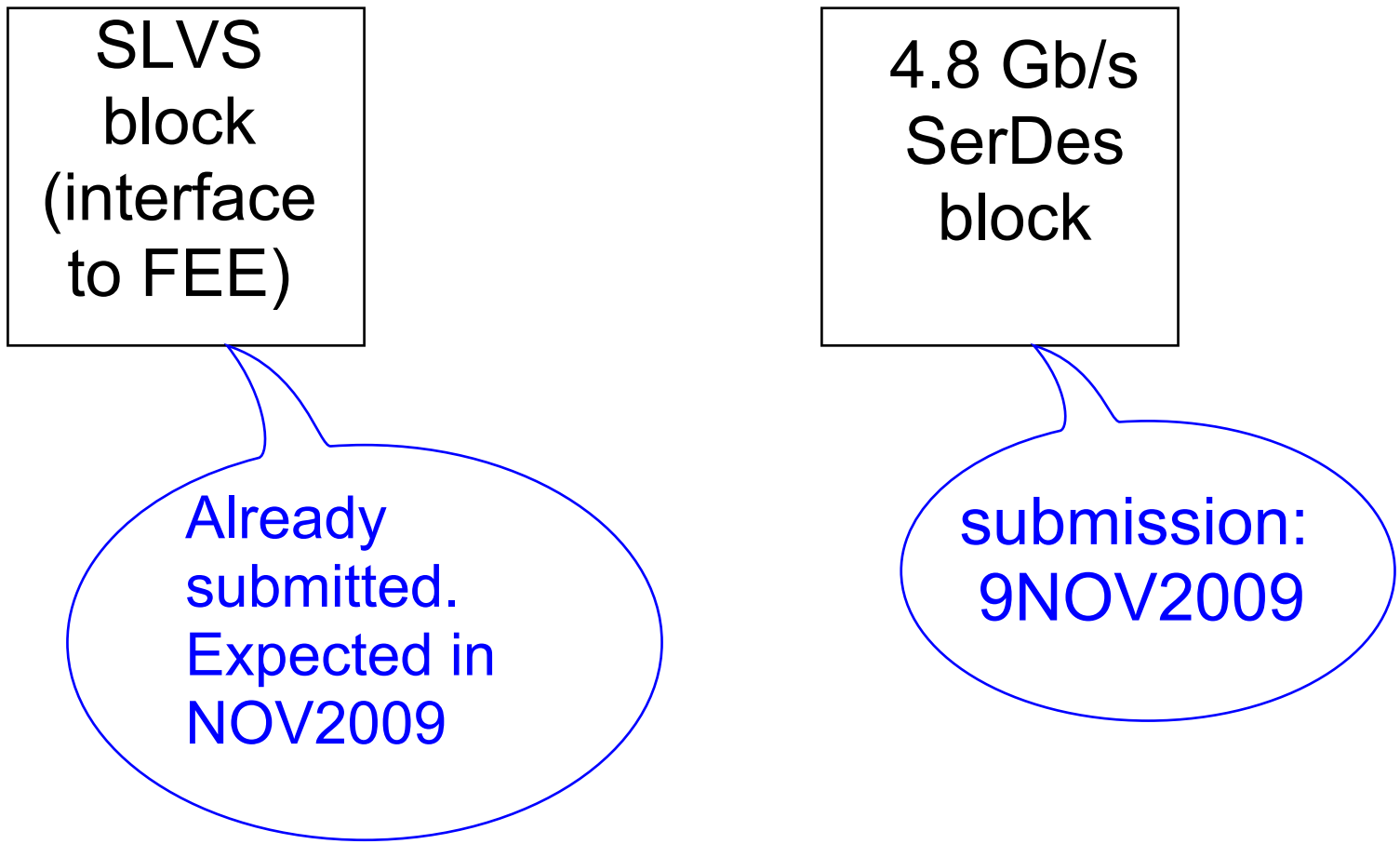
Signals will need do be at least 40 MHz Double-Data-Rate. This is equivalent to an 80 MHz interface + some logic.

More advanced interface modes are 2x and 4x faster.

Today´s FPGAs (Actel, Xilinx,...) do support this requirement.

GBT Submission Status

Separate submission of main building blocks



Other parts

Laser Driver and Transimpedence Amplifier

- Prototypes available in April 2010.
- We might get some chips to play with.

PIN diode and laser.

- Promising work
- An issue is to emulate SLHC dose and annealing

Packages

- GBTX package 16 x 16 mm2 **?**
- SFP transceiver (laser + LD) package 14 x 10 x 50 mm3 **?**

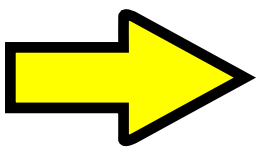
The "packaging" of multiple laser devices is a R&D opportunity for HCAL + ECAL + GBT teams.

Counting Room

- It has been demonstrated the FPGA to receive the GBT link in the counting room.
- It takes a lot of the FPGA logic resources.
- On a Virtex-5, it takes 1481 slices per link .
- Having multiple links allows some optimization.

Example: miniCTR2

- XC5VFX70T FPGA
- 11200 slices
- 16 high-speed links.
- receiving "only" 7 GBT links would use all FPGA resources



CTR may need to use more modern and bigger FPGAs

Other news (non GBT)

- CERN MIC is working on a DC-DC converter (switching regulator) for SLHC.
- The existing HCAL FE has linear regulators.
- The switching regulator may reduce a lot our power dissipation
- If we are interested we should talk soon to the developers about schedule and specs.

Comments ?

Questions ?