Plans and Progress on the FPGA+ADC Card Pack

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Upgrade Workshop, Fermilab

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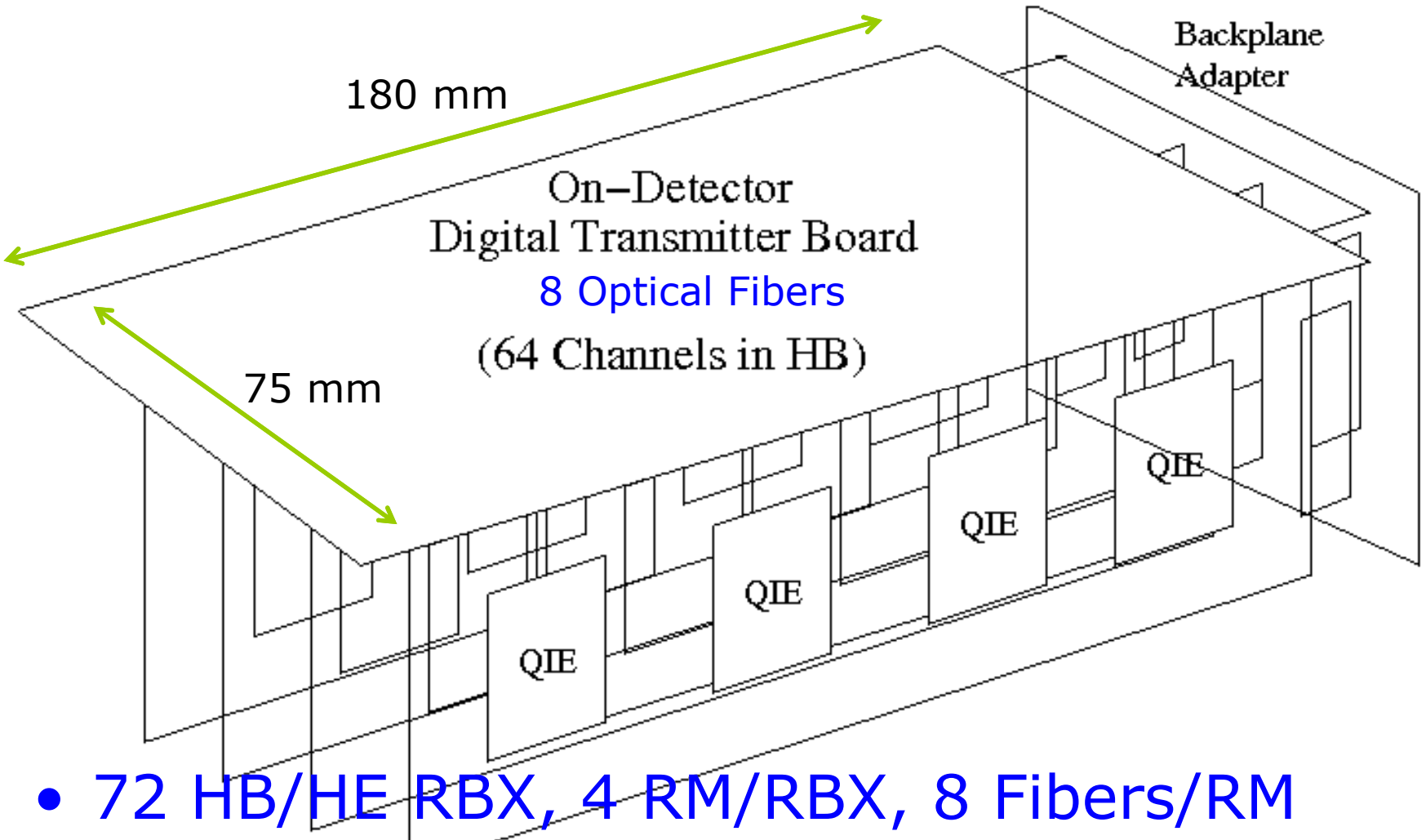
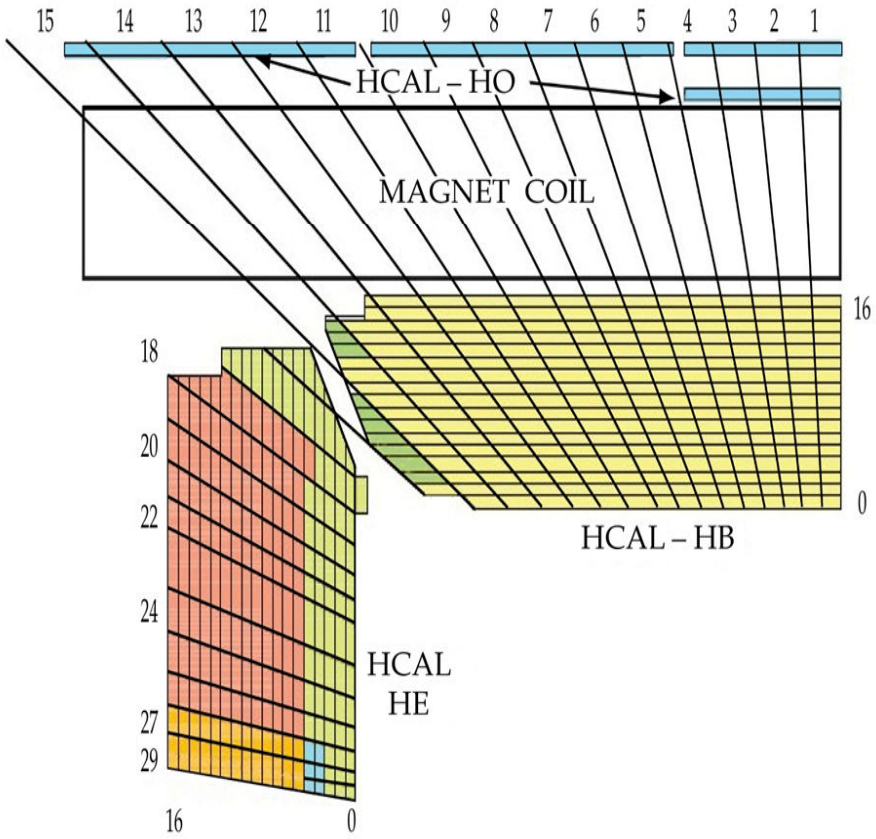
General Concept



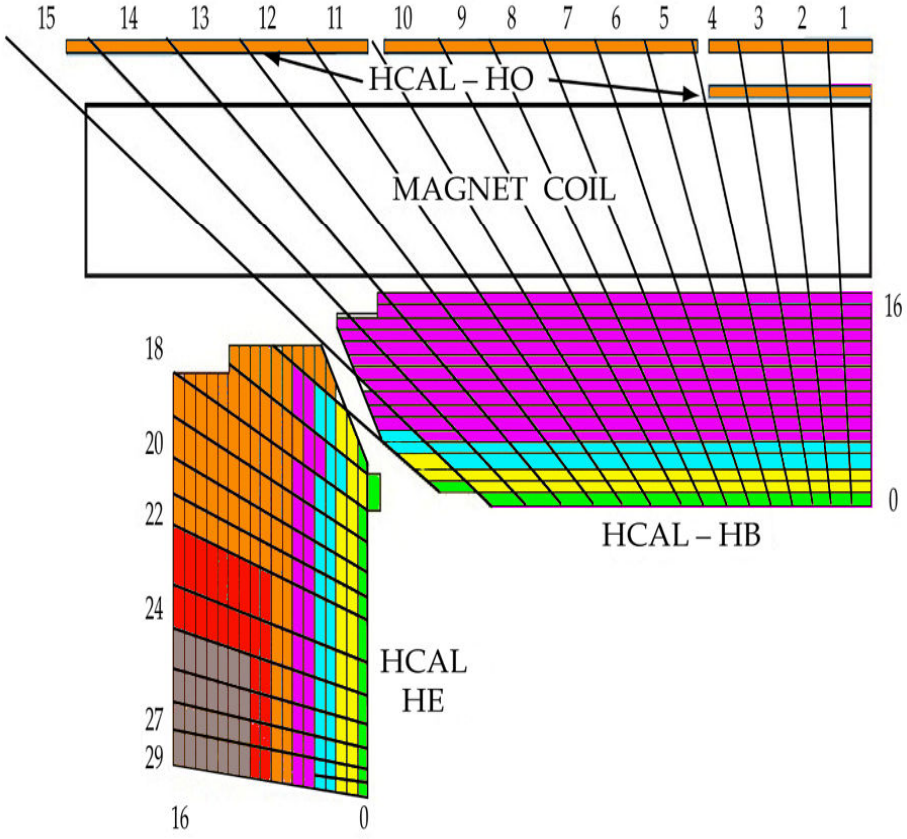
- 72 HB/HE RBX, 4 RM/RBX, 8 Fibers/RM
  - 2304 Digital Links in HB/HE

More Depth Segmentation in HCAL

Current
18-Channel RMs



Upgrade
64-Channel HB RMs
48-Channel HE RMs

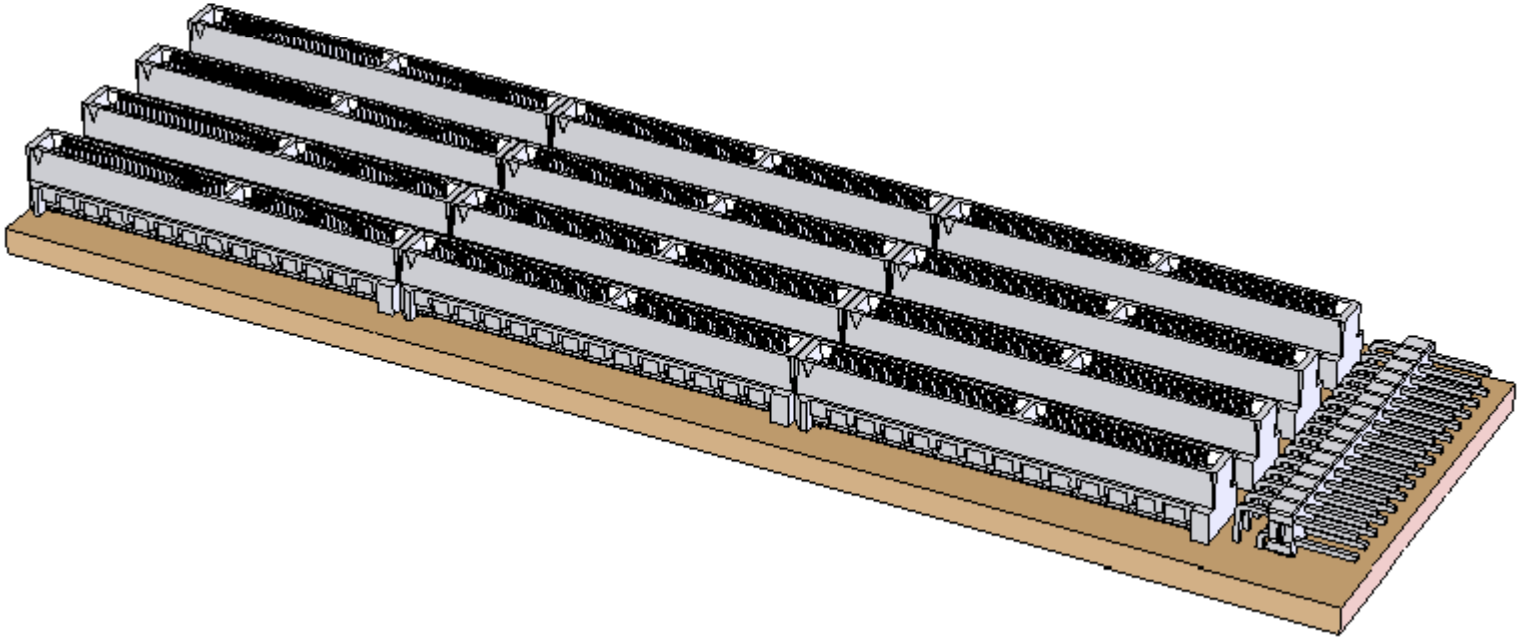


Pin Count

- Quad-Pack QIE10 outputs to FPGA board:
  - 4x8-bit QIE
  - 4x2-bit CapID (eventually 1x2-bit all sync'd)
  - 4x1 diff. pair of TDC
- Inserting ample grounds for single-ended connections (connector specific) gives ~64 lines total per Quad-Pack or 256 lines for a 16-Channel ADC Card
- For the Barrel, the design goal is 64 channels per RM, or 4 ADC card per FPGA board

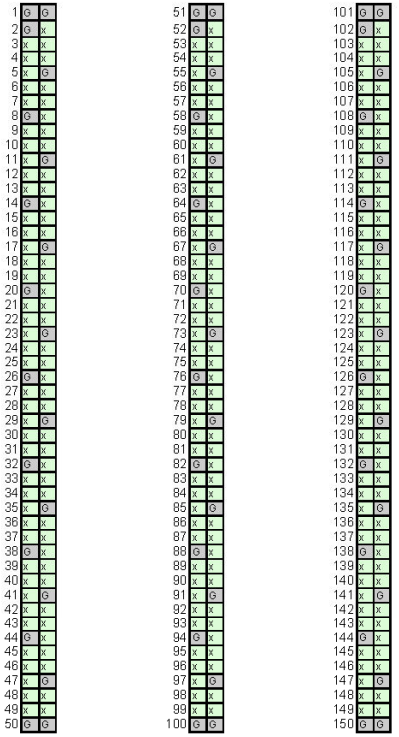
Mechanical Mock-up of FPGA card

- UMN design of FPGA card with 3x100 pin Samtec connectors
- End connector is for backplane interface board (I2C, LV power and clocks)



Samtec Connectors

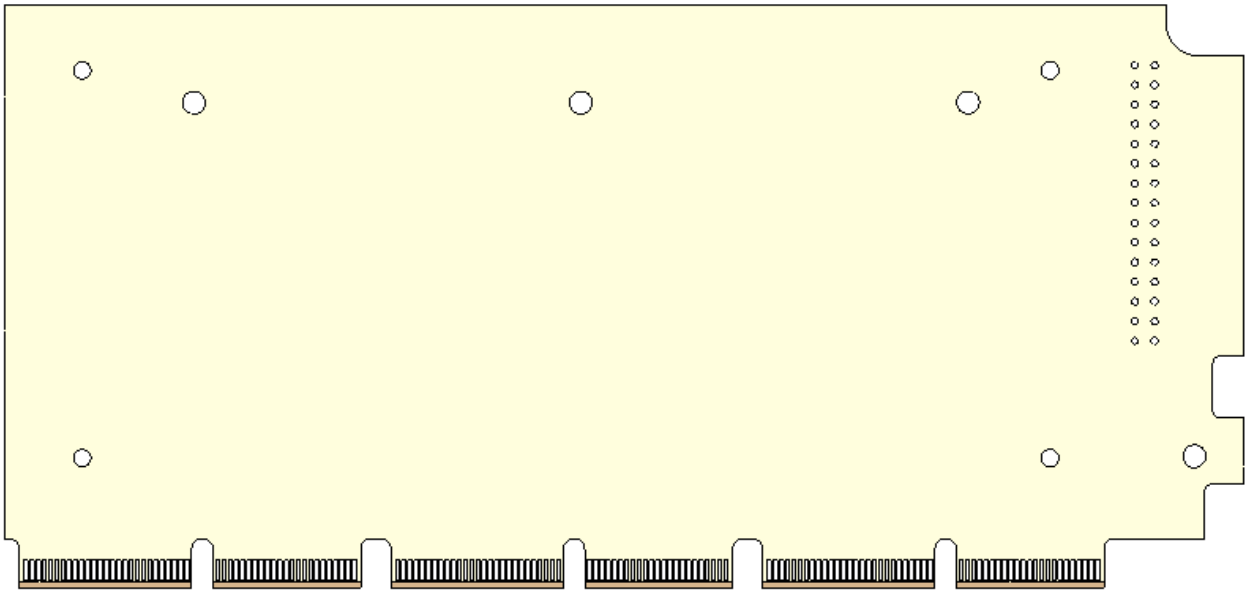
Samtec HSEC8-150-01-SM-DV-A
Digikey (365 in stock)



3 Connectors = 300 pins
240 signals
60 grounds

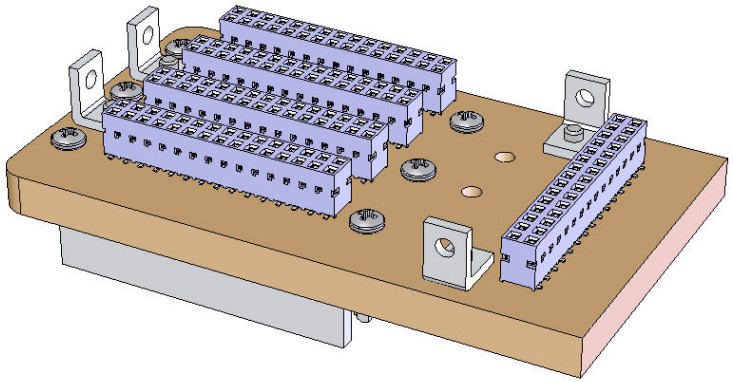
Mechanical Mock-up of ADC card

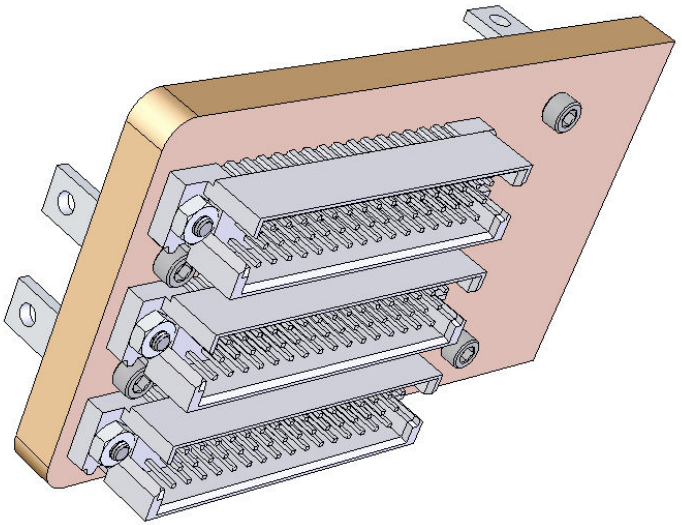
- UMN design of ADC card
- End connectors make board removal somewhat difficult – could be a problem
- Also gets I2C, LV power and clocks from backplane interface board



Mechanical Mock-up of Interface Board

- UMN design of Interface Board
- Mates to RBX backplane and CCM system
- Provides I2C, LV power and clocks
- Problem with Connector Alignment in Current Design





TB 2010 Proposal Part I

- What can be practically achieved for TB 2010 and what can we learn from it?
- Proposal:
  - 12-channel ADC cards (one pseudo-quad pack per Samtec connector)
  - FPGA card serves only 2 ADC card (slots 1 and 3)
  - Allows TB2010 to readout 6 phi for one eta or potentially all layers for a selectable tower (for calibration)
- Provides space to work on ADC cooling plate prototypes and EDU analog cable routing
- Reduces FPGA pin-count requirements

TB 2010 Proposal Part II

- What functionalities would be check?
- Full-speed digital links between front-end and back-end (using Rocket I/O and protocol emulators)
- Bootstrap QIE10 functionalities by placing a support FPGA on ADC card to handle I2C communication, Pedestal DAC setting, 2-bit Digital Programmable Delay and 1ns Clock Phase Adjustment per Quad-Pack
  - FNAL is doing the QIE Card Pack and it may turn out to be QIE8 singles with a Spartan bootstrapping the QIE10 functionality

TB 2010 Proposal Part III

- Not so critical goals for TB 2010
  - Based on TB 2009, the RM mock-up does not have to fit into the existing RBX – allowing the RM to be standalone simplifies testing and allows the Interface Board to be services with an external I2C communication cable, LV power and clock source

Summary

- Proposal and Mechanical Mock-up provided for FPGA+ADC+InterfaceBoard card pack
- Proposal limits card pack to 24-channels and no direct RBX interface requirement (RBX interface can be added later in the year)
- Full-density EDU and control cards are still planned for TB 2010
- Need to test whether switching layer configurations can be done and how