

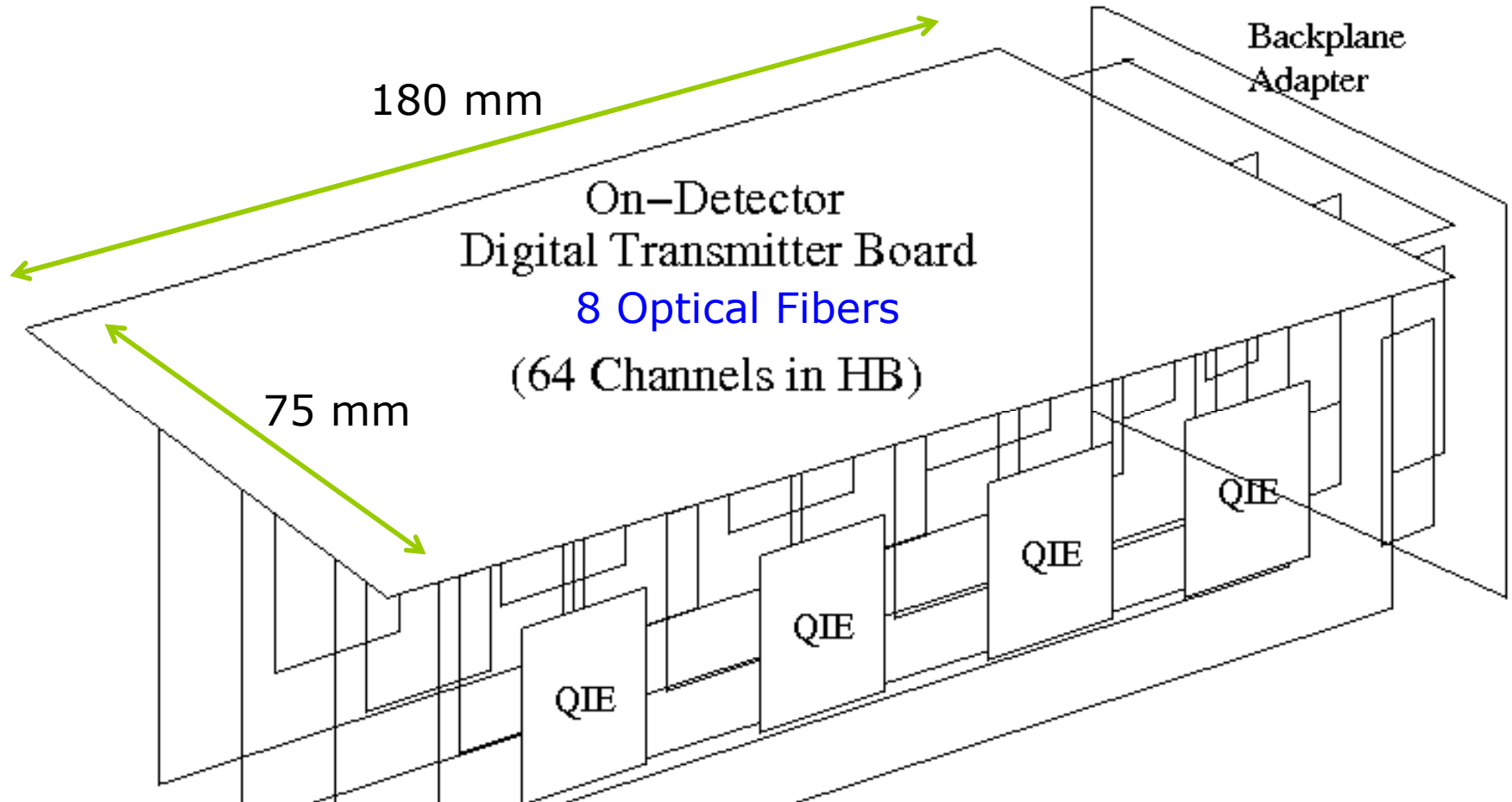
# Plans and Progress on the FPGA+ ADC Card Pack



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Upgrade Workshop, Fermilab  
October 28, 2009

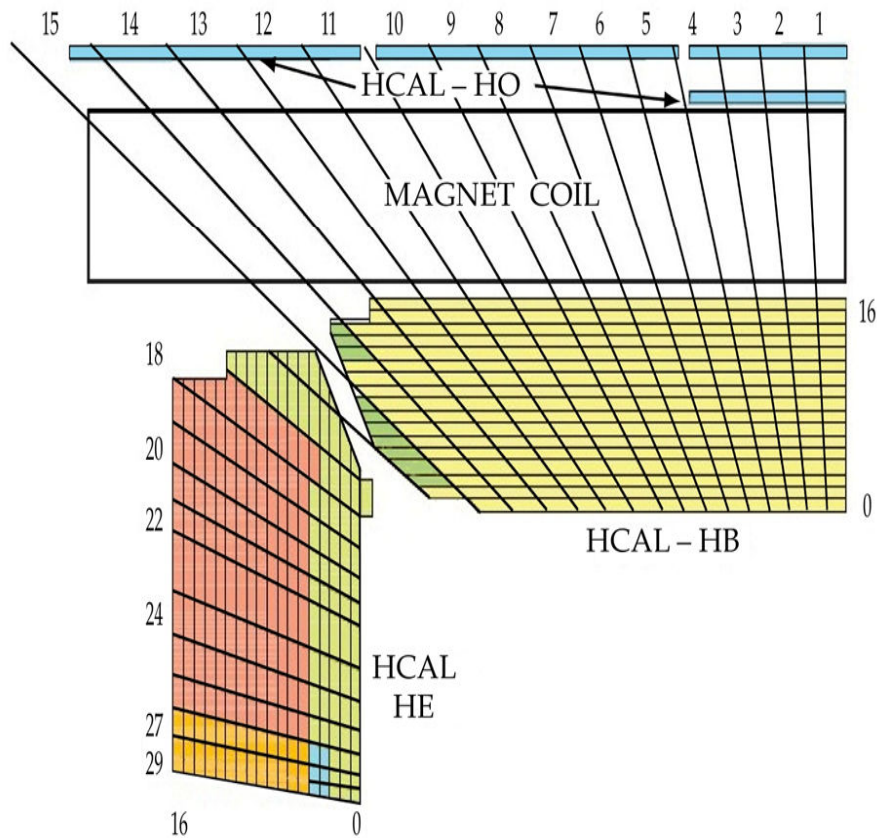
# General Concept



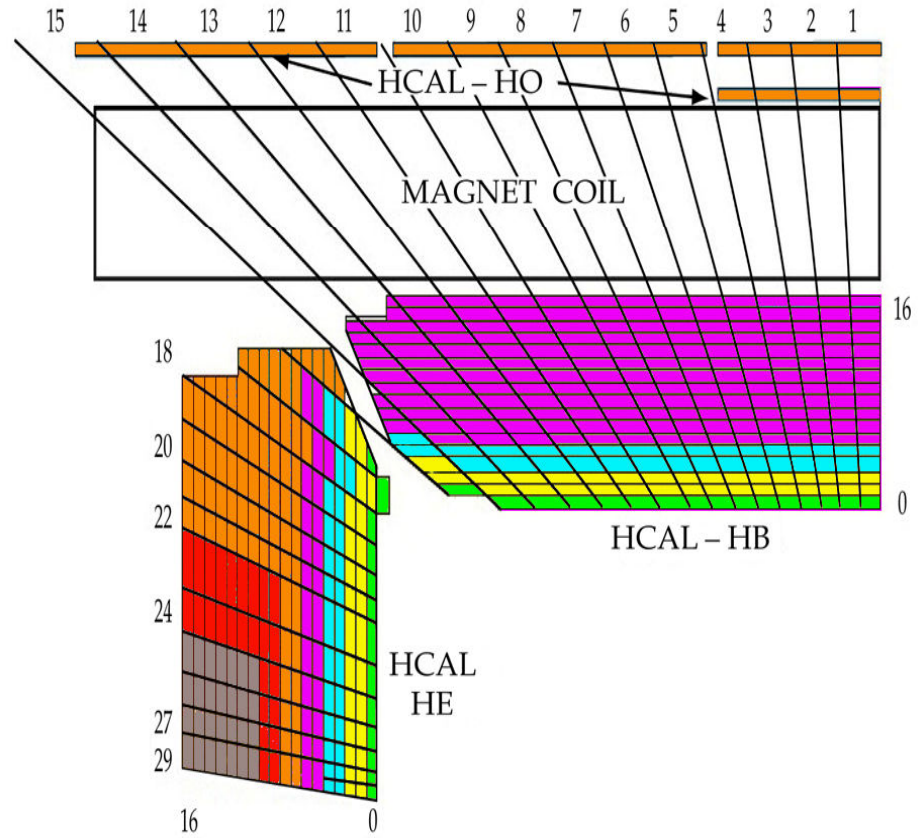
- 72 HB/HE RBX, 4 RM/RBX, 8 Fibers/RM  
– 2304 Digital Links in HB/HE

# More Depth Segmentation in HCAL

Current  
18-Channel RMs



Upgrade  
64-Channel HB RMs  
48-Channel HE RMs



# Pin Count

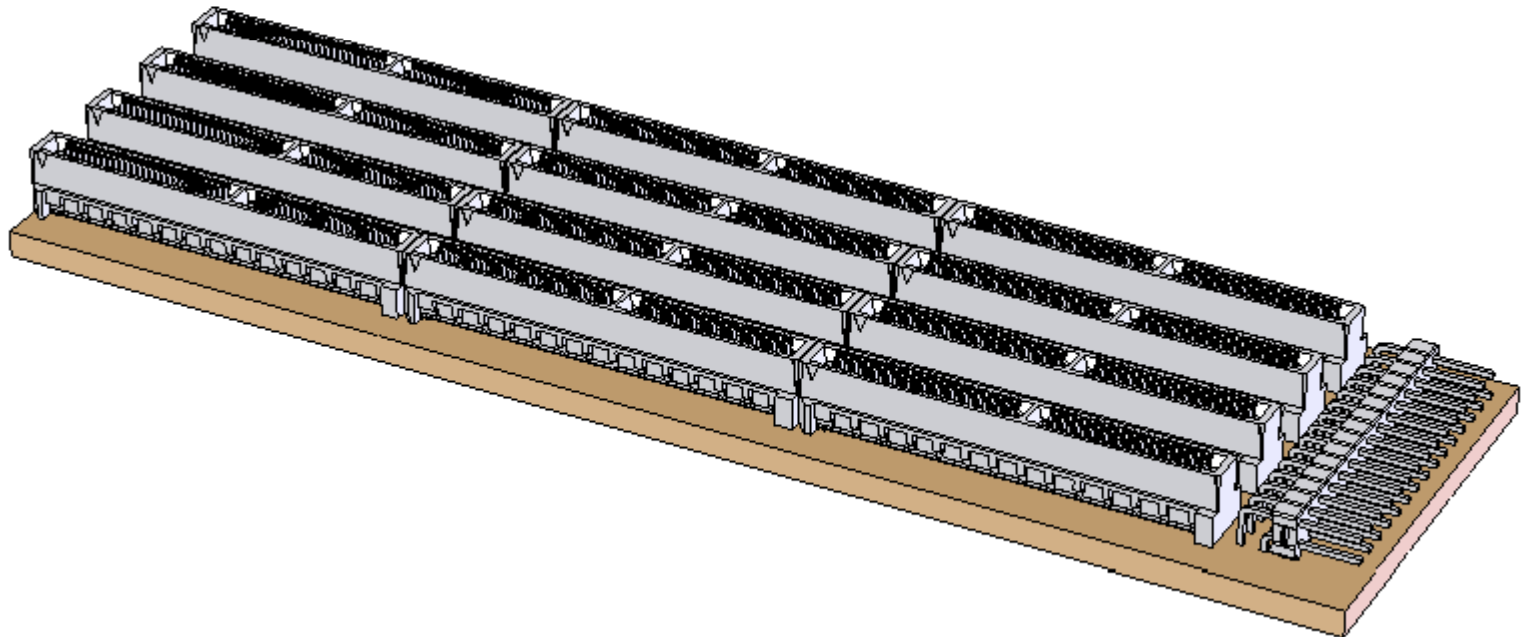
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- Quad-Pack QIE10 outputs to FPGA board:
  - 4x8-bit QIE
  - 4x2-bit CapID (eventually 1x2-bit all sync'd)
  - 4x1 diff. pair of TDC
- Inserting ample grounds for single-ended connections (connector specific) gives ~64 lines total per Quad-Pack or 256 lines for a 16-Channel ADC Card
- For the Barrel, the design goal is 64 channels per RM, or 4 ADC card per FPGA board

# Mechanical Mock-up of FPGA card

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- UMN design of FPGA card with 3x100 pin Samtec connectors
- End connector is for backplane interface board (I2C, LV power and clocks)



# Samtec Connectors



Samtec HSEC8-150-01-SM-DV-A  
Digikey (365 in stock)

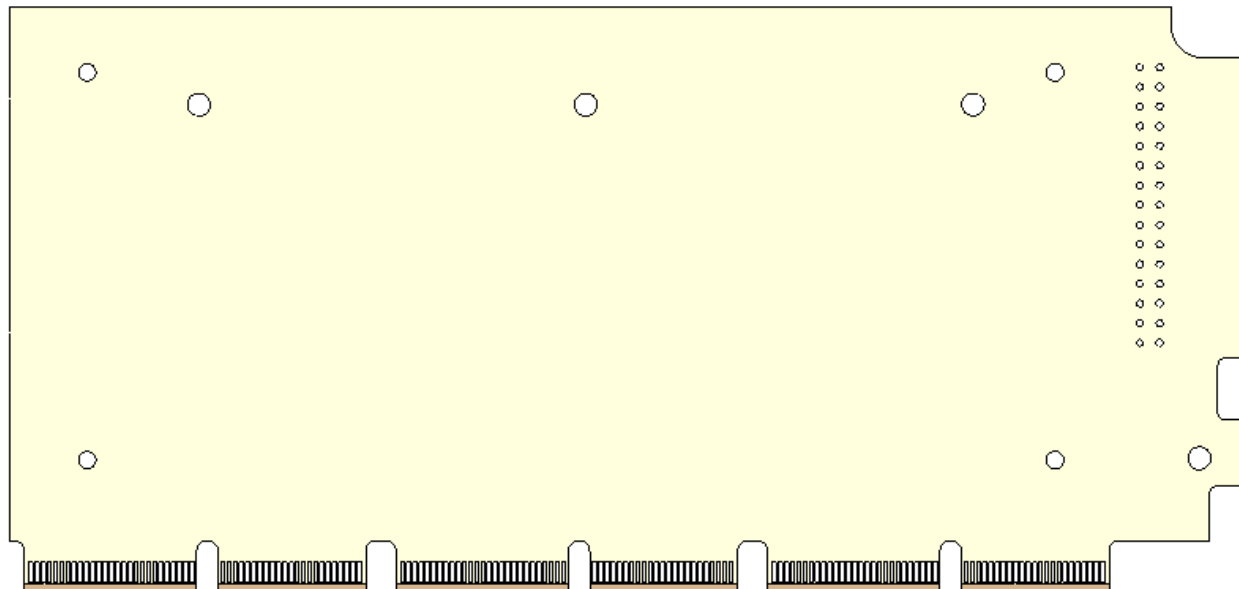
1	G	G	51	G	G	101	G	G
2	G	K	52	G	K	102	G	K
3	K	K	53	K	K	103	K	K
4	K	K	54	K	K	104	K	K
5	K	G	55	K	G	105	K	G
6	K	K	56	K	K	106	K	K
7	K	K	57	K	K	107	K	K
8	G	K	58	G	K	108	G	K
9	K	K	59	K	K	109	K	K
10	K	K	60	K	K	110	K	K
11	K	G	61	K	G	111	K	G
12	K	K	62	K	K	112	K	K
13	K	K	63	K	K	113	K	K
14	G	K	64	G	K	114	G	K
15	K	K	65	K	K	115	K	K
16	K	K	66	K	K	116	K	K
17	K	G	67	K	G	117	K	G
18	K	K	68	K	K	118	K	K
19	K	K	69	K	K	119	K	K
20	G	K	70	G	K	120	G	K
21	K	K	71	K	K	121	K	K
22	K	K	72	K	K	122	K	K
23	K	G	73	K	G	123	K	G
24	K	K	74	K	K	124	K	K
25	K	K	75	K	K	125	K	K
26	G	K	76	G	K	126	G	K
27	K	K	77	K	K	127	K	K
28	K	K	78	K	K	128	K	K
29	K	G	79	K	G	129	K	G
30	K	K	80	K	K	130	K	K
31	K	K	81	K	K	131	K	K
32	G	K	82	G	K	132	G	K
33	K	K	83	K	K	133	K	K
34	K	K	84	K	K	134	K	K
35	K	G	85	K	G	135	K	G
36	K	K	86	K	K	136	K	K
37	K	K	87	K	K	137	K	K
38	G	K	88	G	K	138	G	K
39	K	K	89	K	K	139	K	K
40	K	K	90	K	K	140	K	K
41	K	G	91	K	G	141	K	G
42	K	K	92	K	K	142	K	K
43	K	K	93	K	K	143	K	K
44	G	K	94	G	K	144	G	K
45	K	K	95	K	K	145	K	K
46	K	K	96	K	K	146	K	K
47	K	G	97	K	G	147	K	G
48	K	K	98	K	K	148	K	K
49	K	K	99	K	K	149	K	K
50	G	G	100	G	G	150	G	G

3 Connectors = 300 pins  
240 signals  
60 grounds

# Mechanical Mock-up of ADC card

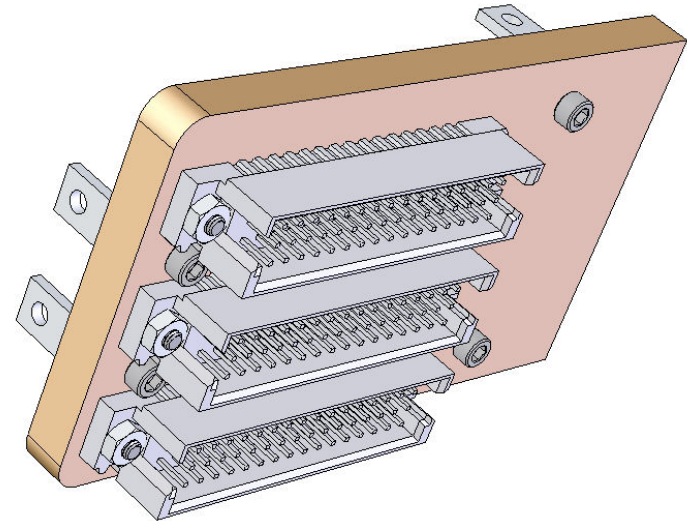
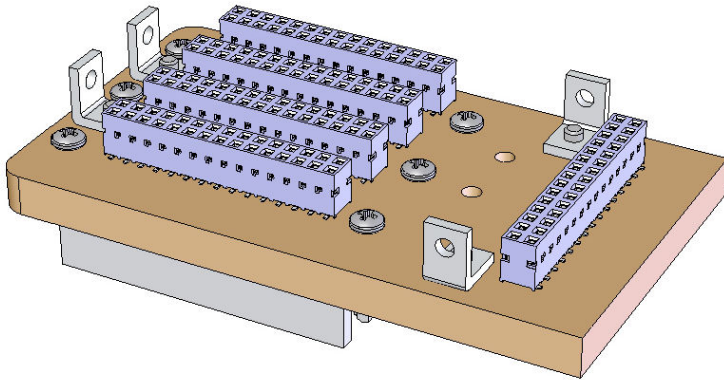
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- ❑ UMN design of ADC card
- ❑ End connectors make board removal somewhat difficult – could be a problem
- ❑ Also gets I2C, LV power and clocks from backplane interface board



# Mechanical Mock-up of Interface Board

- ❑ UMN design of Interface Board
- ❑ Mates to RBX backplane and CCM system
- ❑ Provides I2C, LV power and clocks
- ❑ Problem with Connector Alignment in Current Design





# TB 2010 Proposal Part I

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- ❑ What can be practically achieved for TB 2010 and what can we learn from it?
- ❑ Proposal:
  - 12-channel ADC cards (one pseudo-quad pack per Samtec connector)
  - FPGA card serves only 2 ADC card (slots 1 and 3)
  - Allows TB2010 to readout 6 phi for one eta or potentially all layers for a selectable tower (for calibration)
- ❑ Provides space to work on ADC cooling plate prototypes and EDU analog cable routing
- ❑ Reduces FPGA pin-count requirements

# TB 2010 Proposal Part II

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- ❑ What functionalities would be check?
- ❑ Full-speed digital links between front-end and back-end (using Rocket I/O and protocol emulators)
- ❑ Bootstrap QIE10 functionalities by placing a support FPGA on ADC card to handle I2C communication, Pedestal DAC setting, 2-bit Digital Programmable Delay and 1ns Clock Phase Adjustment per Quad-Pack
  - FNAL is doing the QIE Card Pack and it may turn out to be QIE8 singles with a Spartan bootstrapping the QIE10 functionality

# TB 2010 Proposal Part III

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- Not so critical goals for TB 2010
  - Based on TB 2009, the RM mock-up does not have to fit into the existing RBX – allowing the RM to be standalone simplifies testing and allows the Interface Board to be services with an external I2C communication cable, LV power and clock source

# Summary

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- Proposal and Mechanical Mock-up provided for FPGA+ADC+InterfaceBoard card pack
- Proposal limits card pack to 24-channels and no direct RBX interface requirement (RBX interface can be added later in the year)
- Full-density EDU and control cards are still planned for TB 2010
- Need to test whether switching layer configurations can be done and how