TMB Upgrade for ME1/1 CSCs

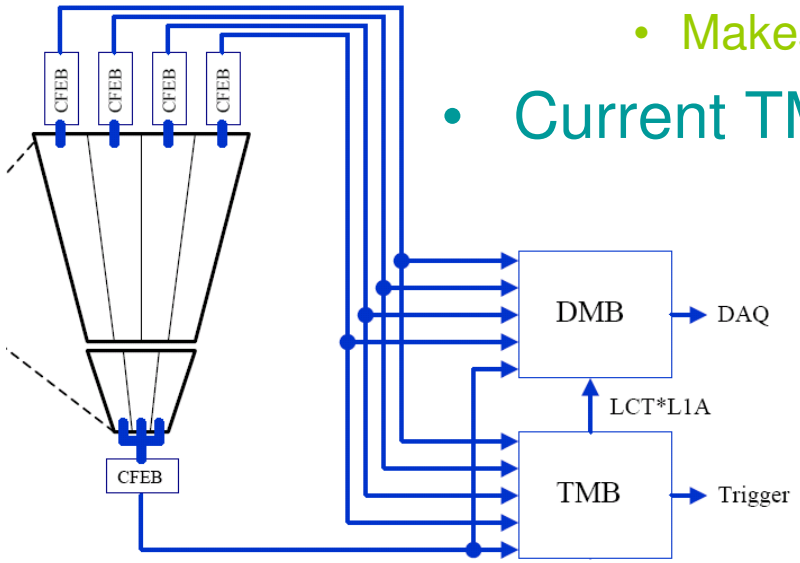
J. Gilmore

CMS Upgrade Workshop, FNAL

28 October 2009

Present constraints for ME1/1 CSCs

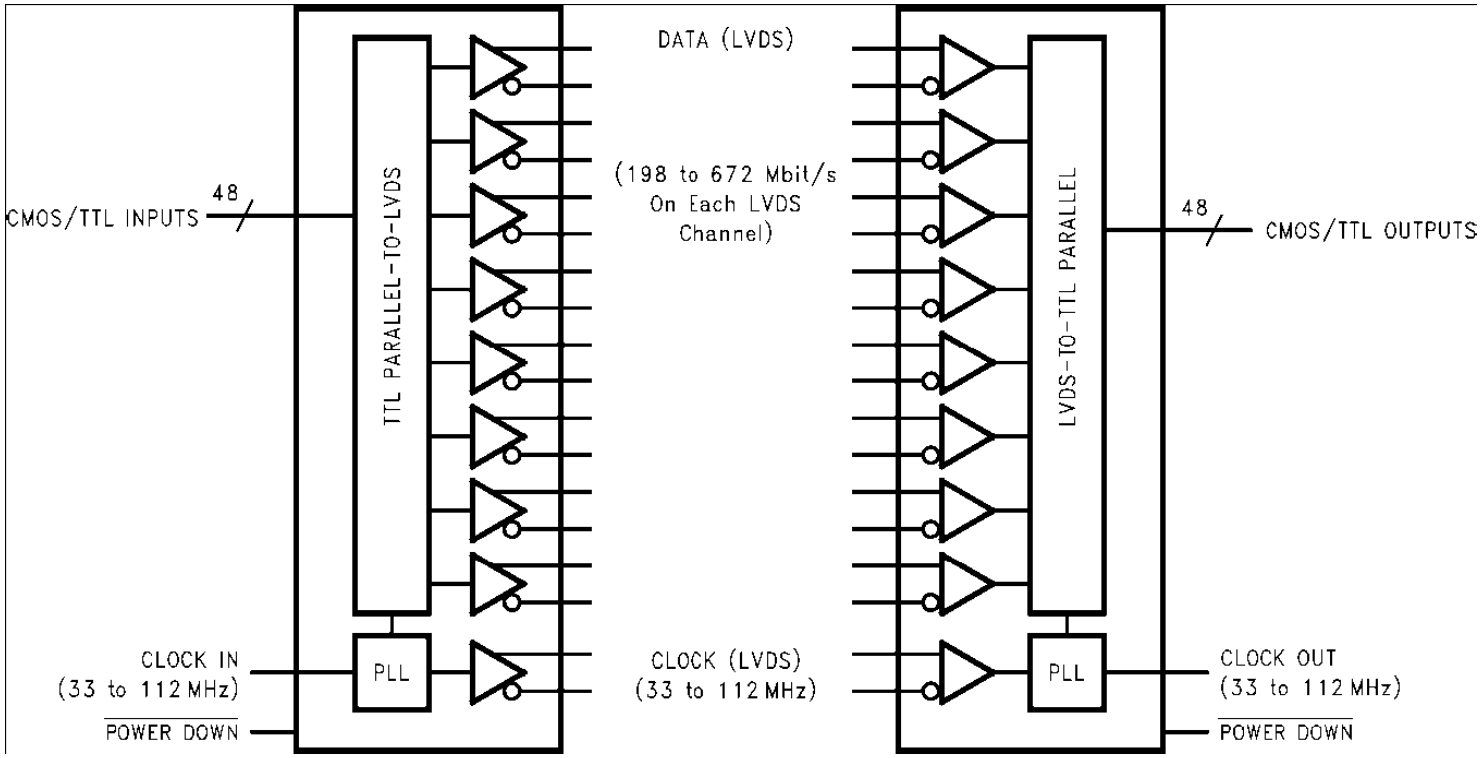
- ME1/1 CSCs have the highest muon rate
  - Accounts for about 60% of endcap track stubs
- ME1/1 chambers are divided into two sections
  - Low-eta has 64 strips, readout via 4 CFEBs
  - High-eta has 48 strips, readout via 1 CFEB
    - This is achieved by “ganging” strips 3-to-1
    - Makes efficient triggering at high-eta impossible
- Current TMBs can only accept 5 CFEB inputs



Upgrade plan for ME1/1 CSCs

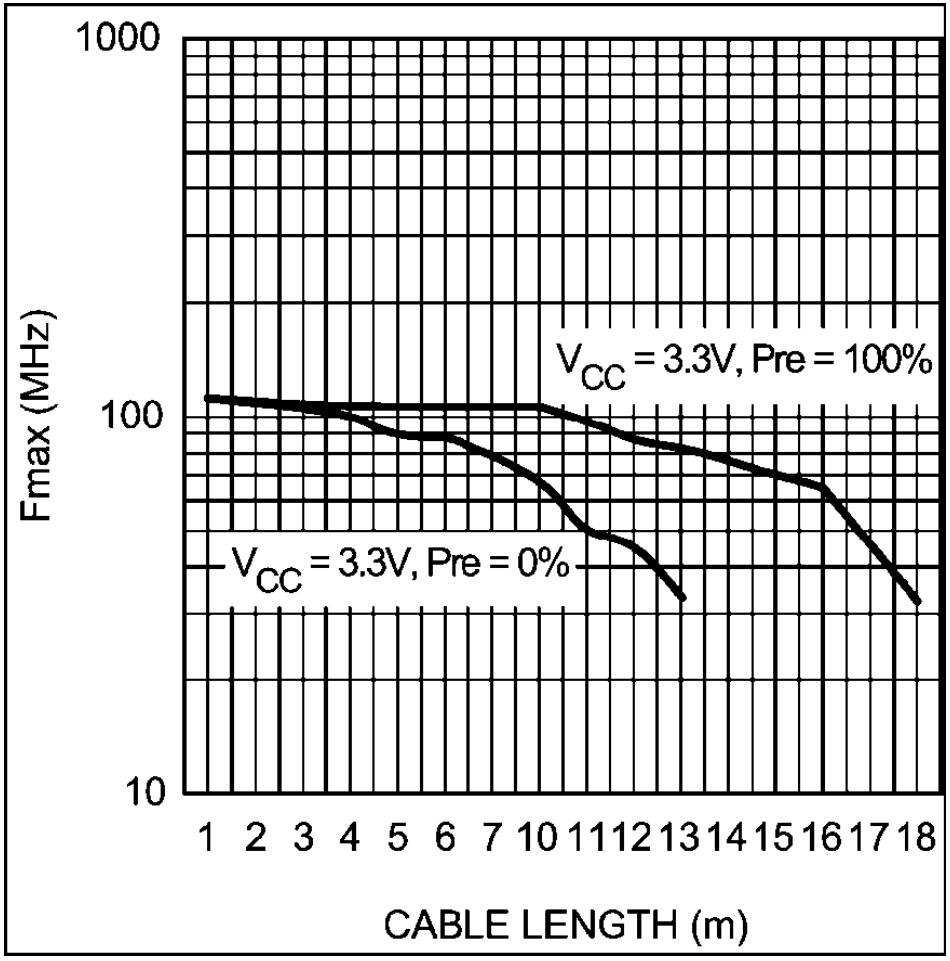
- Remove ganging for high-eta strips
- Use 7 CFEBs for strip readout
  - New digital dCFEB design with data readout via fiber
- Build a new TMB that accepts 7 CFEB inputs
  - One obvious choice is to use fiber connections for trigger path
    - Has some technological constraints, maybe not the best choice
  - There is also a reasonable copper cable solution to consider…

Comparator dCFEB-to-TMB option



- Channel Link: DS90CR483/484A
- 48-8 bit Ser/Deser, requires 19 conductors per CFEB
  - Consider 20th conductor as a cable detect
- Has options for pre-emphasis and DC balancing
  - Should provide reliable operation, even on our longest cables
- Adds ~3 BX to the trigger latency (~same as fiber options)

Channel Link Performance Spec



- Performance exceeds our needs: 14 m cable @40 MHz
- Use the same 50-conductor SkewClear, w/5 cables to TMB
  - Each cable can carry one OR two CFEB's comparator bits
  - ME1/1 patch panel will handle fan-out for two-CFEB case

TMB R & D Plans

Near-term: Prove reliability of new Channel Links

- Build test board for pseudorandom patterns over Skewclear
  - FPGA, new Channel Link Tx and Rx, two connectors
  - Run at 40 MHz and beyond, watch for bit errors
- Build a realistic mock-up of new patch panel
  - Two Skewclear connectors linked by optimized trace routing
- Use 2 Skewclear cables, test at ME1/1 length (14 m)
  - One 9 m cable and one 6 m cable, linked by patch panel

Longer-term: Build prototype for TMB upgrade

- Include new FPGA and new LCT stub algorithms