Forward Pixel Detector

FPix Upgrade

Readout Architecture

CMSpix-doc-XXXX

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Outline

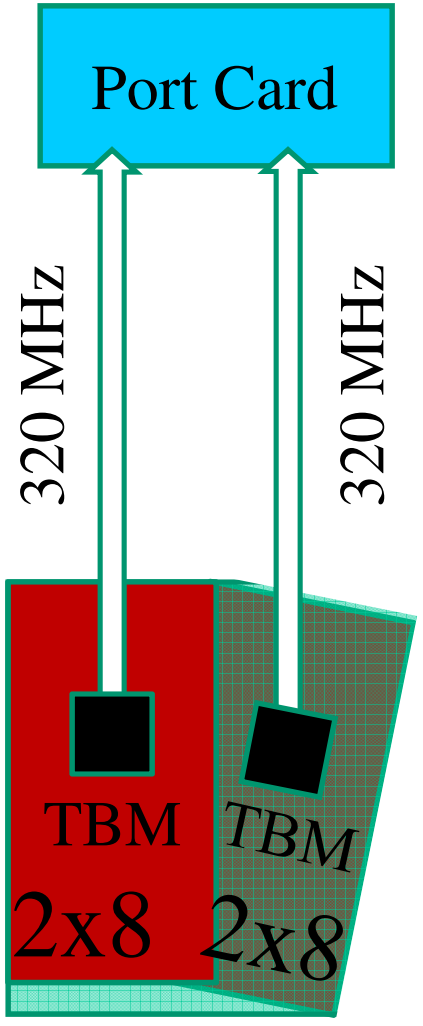
- Design constraints
- FPix disk electronics structure
- Half disk readout structure
- Phase I port card outline
- Multiplexing module readout
- FPix readout cable concept/prototype
- Conclusion

FPix Upgrade Design Constraints

- New FPix disks pack a lot more ROCs for the sake of a simpler and more uniform design (and a better coverage)
- Current FPix = 4,320 ROCs (6,480 for 6 disks)
- Phase I FPix = 10,752 ROCs (x1.66)
- Cable Plant for Phase I PP0 stays the same
  - 48 + 4 power cables
  - 8 control cables
  - 288 + 96 readout fibers / currently allocated 288
  - 288 + 96 control fibers / currently allocated 192
- Material budget should be kept to the minimum and pushed to the higher η, preferably beyond the tracking coverage region

FPix Disk Electronics Structure

- This information can be found in many more details in other talks, I'll just repeat what effects the electronic system
- Current disk design is based on trapezoidal blades with detector modules attached to both sides, providing complete surface coverage
- Each detector module is a 2x8 ROC/Sensor arrangement
- There were two major readout options for such a structure
  - One TBM – single readout channel
  - Two TBMs – two readout channels
- Longer electrical path from one side to another for a single TBM solution, and mechanical issues associated with assembly motivates us to find a way of independent module readout



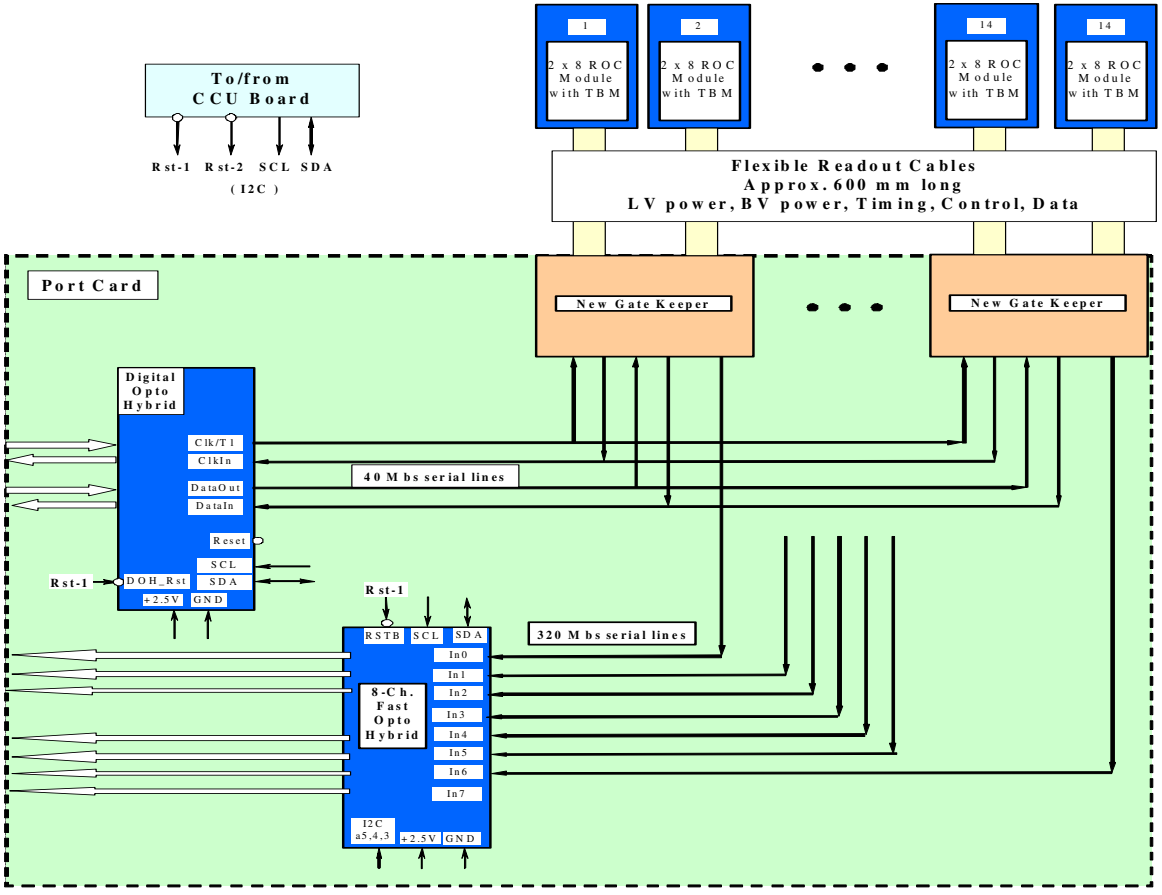
Two 2x8 Modules on both sides of a blade

Half Disk Readout Structure

- Mechanically FPix detector consists of half-disks installed in service half-cylinders (always called simply “service cylinder”)
- There are 4 power cables we can use to power up readout electronics of one half-disk, which makes it natural to have 4, 8, 16, etc. readout boards – I’ll continue calling them “Port Cards”
- In the current FPix we have 4 Port Cards per half disk, which was dictated by the 6-channel AOH boards
- For now we plan to keep the number of port cards (4) per half disk
- Half disk consists of two sections:
  - Inner – 11 blades, 22 detector modules
  - Outer – 17 blades, 34 detector modules
- On average that’s surprisingly an integer number of 14 modules per port card!
- In the current FPix one DOH slow control channel (available on a port card) is able to address up to 32 TBM nodes, so those 14 should not cause any new problems
- Having maximum of 8 data fibers available per port card creates a need of multiplexing several TBM outputs in a single readout channel
- It sounds reasonable to multiplex 2 channels in a single data fiber. The “AOH” best suited for that configuration should have 2, 4, or 8 channels per board

Phase I Port Card Outline

- A new Gate Keeper chip provides an interface to the detector modules:
  - Distributes system clock
  - Distributes L1a/Ctr commands
  - Provides write/read communication to/from ROCs and TBMs
  - Sequences readout from two TBMs, multiplexed to the same data fiber
- I2C slow control stays the same, using a CCU board
- Power distribution is based on air core DC-DC converters (see AMIS2 design report)



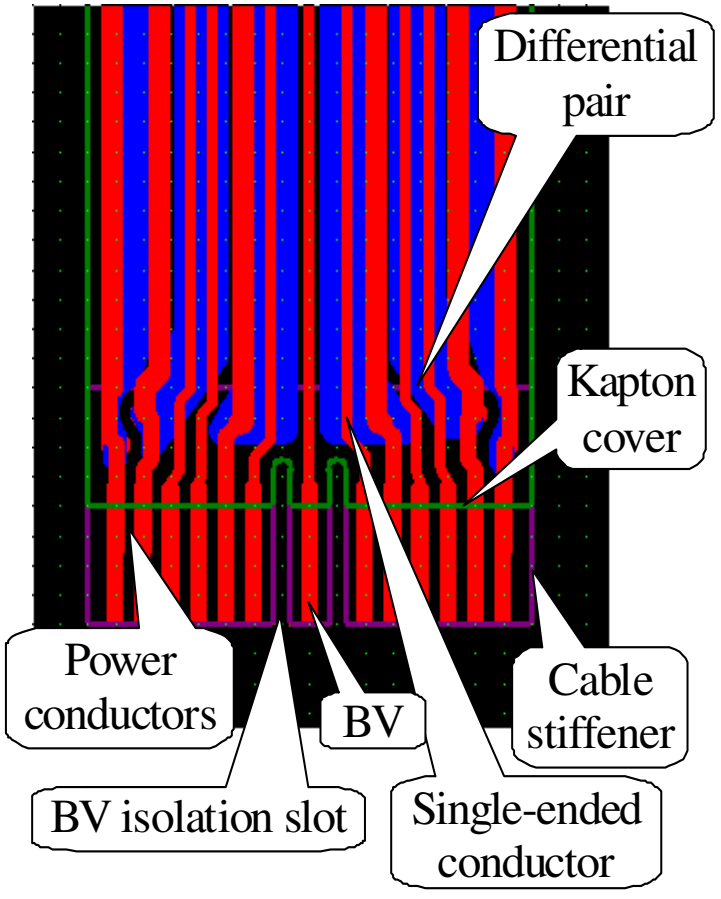
Multiplexed Module Readout

- Multiplexing of several detector modules to a single optical data fiber can be solved by an addition of one extra command (trigger) to the TBM lexicon:
  - On receiving an L1a command from the Gate Keeper TBMs distribute it to the ROCs, but delay issuing a readout token
  - Gate Keeper sends a TO (token out) command to the first module, and waits until it sees the end of the data packet (or a special "token in" signal)
  - Then the Gate Keeper sends a TO command to the next module …
- There are several ways to achieve that:
  - Using minimum invasive approach, which keeps the communication to the TBM intact, with addition of an extra line (token out / done)
  - A more radical one, inspired by Beat Meier's presentations, where all the signals going to the TBM (clock, ctr, slow control data, new token out signal) are packed in a single high speed serial line
- The same Gate Keeper chip can be used for BPix, sending all commands to both connected TBMs

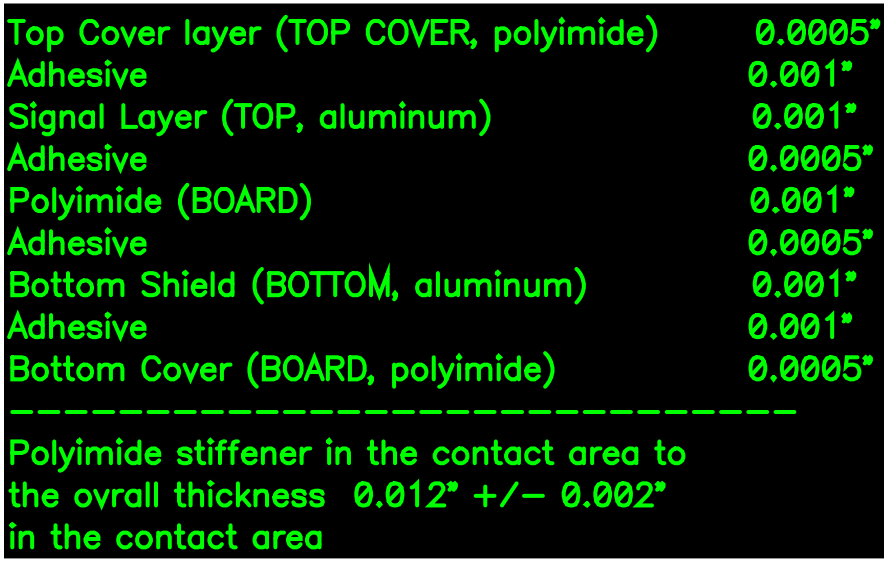
	Minimum Invasive	Radical
Cable composition (conductors)	2 power, 1 BV, 15 signal	2 power, 1 BV, 5 signal
Connector size	FPC 0.5 mm / 28 contacts	FPC 0.5 mm / 15 contacts
Effective thickness (rad. length)	0.2% / aluminum 0.8% / copper	0.1% / aluminum 0.4% / copper

FPix Readout Cable Concept/Prototype

- Readout cable will connect a port card to a detector module
- To simplify assembly readout cable will carry all needed signals, and power in a single package
- A test cable is being manufactured now with the following features:
  - **600 mm long, 8 mm wide**
  - **Symmetric design, so it is reversible**
  - **One BV conductor (aiming at 600V)**
  - **Two differential pairs**
  - **Two single-ended conductors**
  - **Six power conductors**
  - **Two-sided aluminum foil construction**
  - **Gold plated end connectors for 0.5mm ZIF SMD connectors (Hirose FH19)**
- This configuration will allow to study critical aspects of the BV and POWER distribution, and high speed digital signal propagation



FPix Readout Cable Prototype Details



- This prototype will be made with a 0.001" aluminum foil, gold plated in the connector area, it has to be seen whether manufacturers can go to a thicker aluminum to allow for a narrower cable (currently at 8.5 mm wide)
- Minimum trace width is 0.008", all prospective manufacturers have advised against trying narrower traces at the first run
- 0.0005" polyimide is typically rated at 3000kV/mil, and should be sufficient to hold a 600V BV, while providing good abrasion resistance. Adhesive layer should take care of any pin holes in the polyimide film.
- Cable bending radius is expected to be close to 2mm
- FPix Extension cable, which is 450 mm long was measured to have 600 MHz individual trace bandwidth (see **CMSpix-doc-2472),** this provides me with hopes for the adequate performance of the new prototype

Conclusion

- There are several ways we can go depending on how much risk we can tolerate in redesigning the chips
- One of the benefits of redesigning the Gate_Keeper–to–TBM timing/control channel is a lighter readout cable in the low η region
- I should mention micro twisted copper plated aluminum wire cable as a very strong alternative to the flat flex cable:
  - It has smaller material overhead (should check on the copper plating amount)
  - It is easier to bend to a 3-D path
  - Material in micro twisted is less uniformly distributed along φ
  - Termination of a micro twisted cable is a big deal (compared to widely available now gold plated FPC connectors)
- Next step for me would be to test the prototype cable, and start designing one to match the Gate Keeper architecture we'll decide upon