

# SLHC CMS EMU Upgrade

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## Digital CFEB

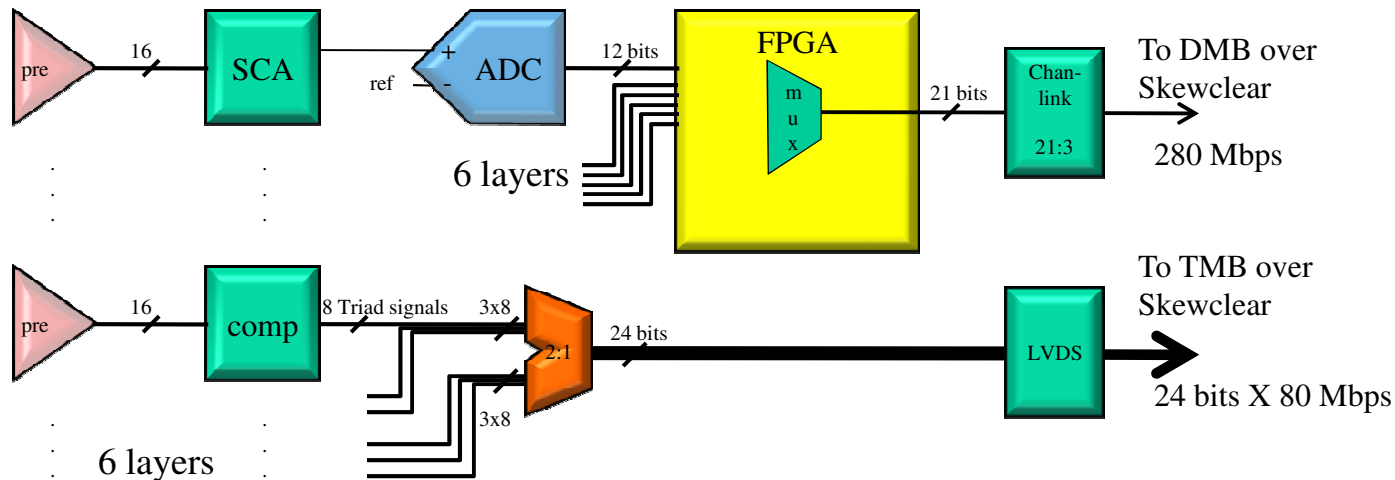
Ben Bylsma

The Ohio State University

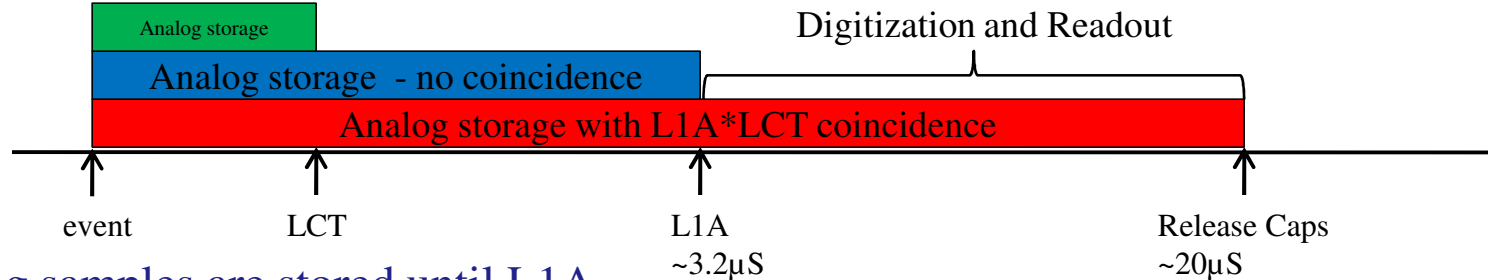


# Current CFEB

## Basic Block Diagram:



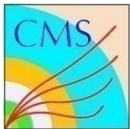
## Time Line:



Analog samples are stored until L1A.

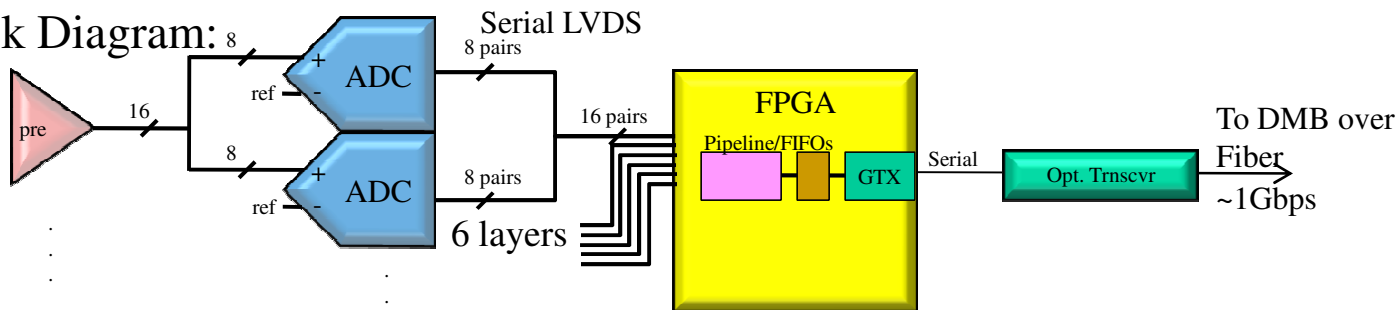
Then ADC must digitize 8X16 samples one at a time.

Limited number of capacitors and single channel ADC impose constraints on LCT and L1A latencies.



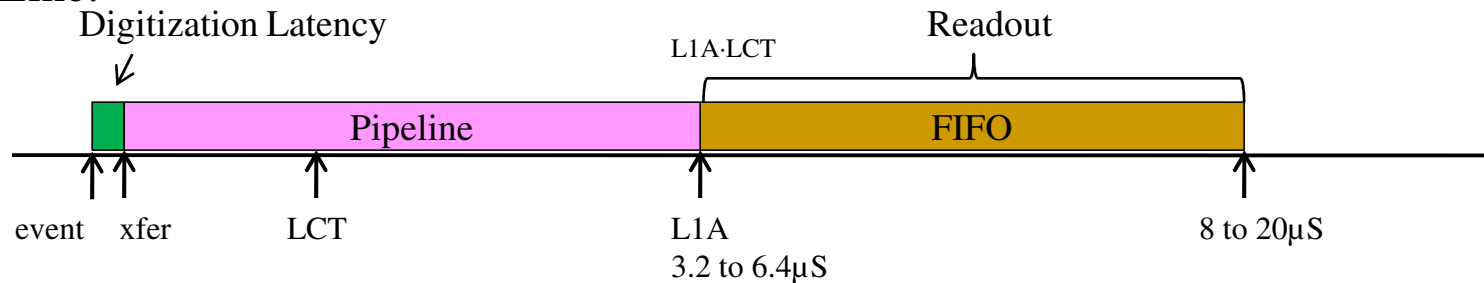
# New DCFEB DAQ Path

Basic Block Diagram:



## DAQ path

Time Line:



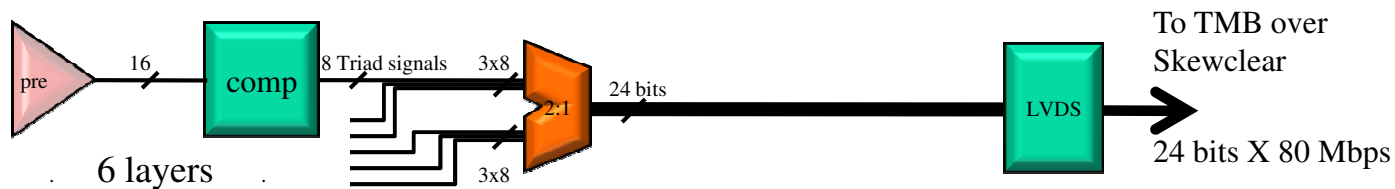
No Dead Time.

All 96 channels continuously digitized (no multiplexing).

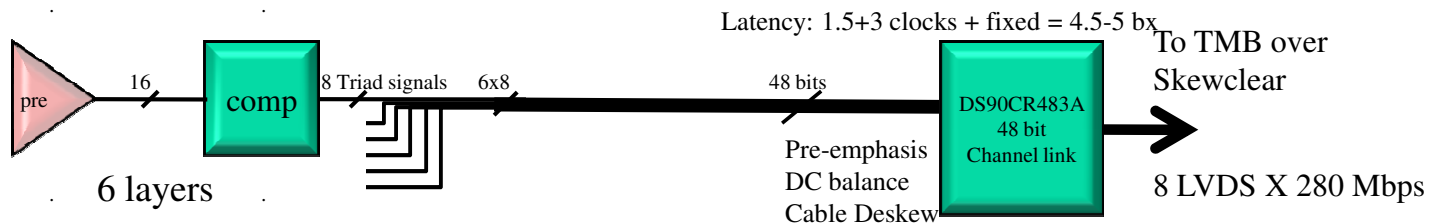


# New DCFEB Trigger Path

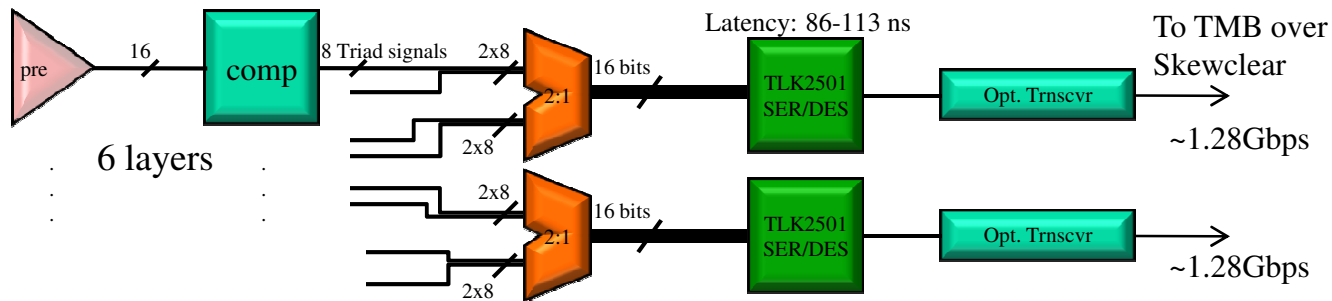
Current Design:



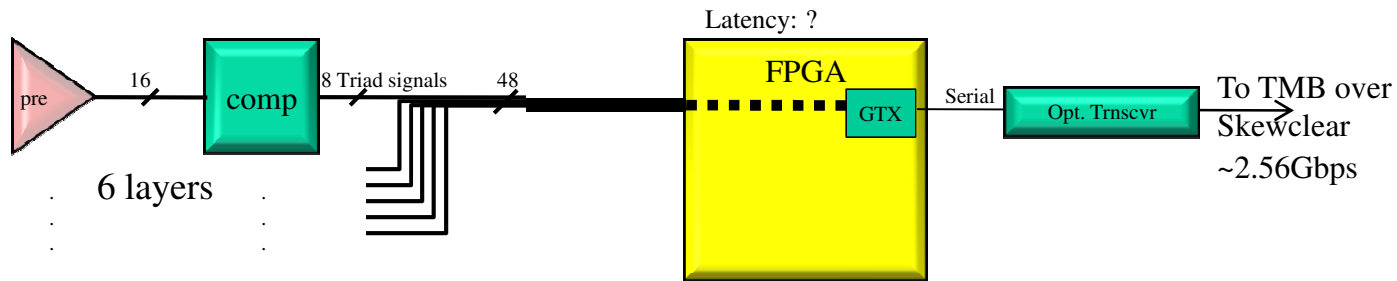
Option A:



Option B:



Option C:





# First Step – Choose ADC

- ADC choice drives subsequent design considerations
  - Interface between pre-amp and ADC
  - Voltage/Power requirements
    - Could impact LVDB design
- ADC choices:(8 ch, 12 bit, 20-65 MSPS, Serial LVDS output)
  - **MAX1437** (Maxim) 1.8V supply,  $1.4V_{pp}$  range
  - **ADC12EU050** (National) 1.2V supply,  $2.1V_{pp}$  range
  - **AD9222** (Analog Devices) 1.8V supply,  $2V_{pp}$  range
  - **ADS5281** (Texas Instr.) 3.3V analog, 1.8V digital,  $2V_{pp}$  range



# Issues with ADCs

- None are suitable drop-in replacements for SCA/ADC

- ADC's

- All have differential inputs
    - Limits on common mode
    - Have internal input bias network

- Pre-Amp

- Single ended output
    - Limited range of baseline level
    - Designed to drive small capacitive load

- Pre-Amp/ADC Interface

- Mnfr. suggest transformer coupling  
(not an option for us)
    - Amplifier to generate differential signal  
(requires 96 amplifiers)
    - Direct couple single ended signal  
(common mode consequences)  
(level shifting/scaling)
    - AC couple single ended signal  
(common mode consequences)  
(no level shifting, but still have biasing to consider)



# Constraints (ADS5281)

## •ADC Constraints:

- $V_{cm} - 600mV < (IN+ + IN-)/2 < V_{cm} + 300mV$  (1.8V<sub>pp</sub> on IN+)
- $(IN- - 1V) < IN+ < (IN+ + 1V)$  (ADC output range)

## •Pre-Amp Constraints:

### ▪Baseline Level

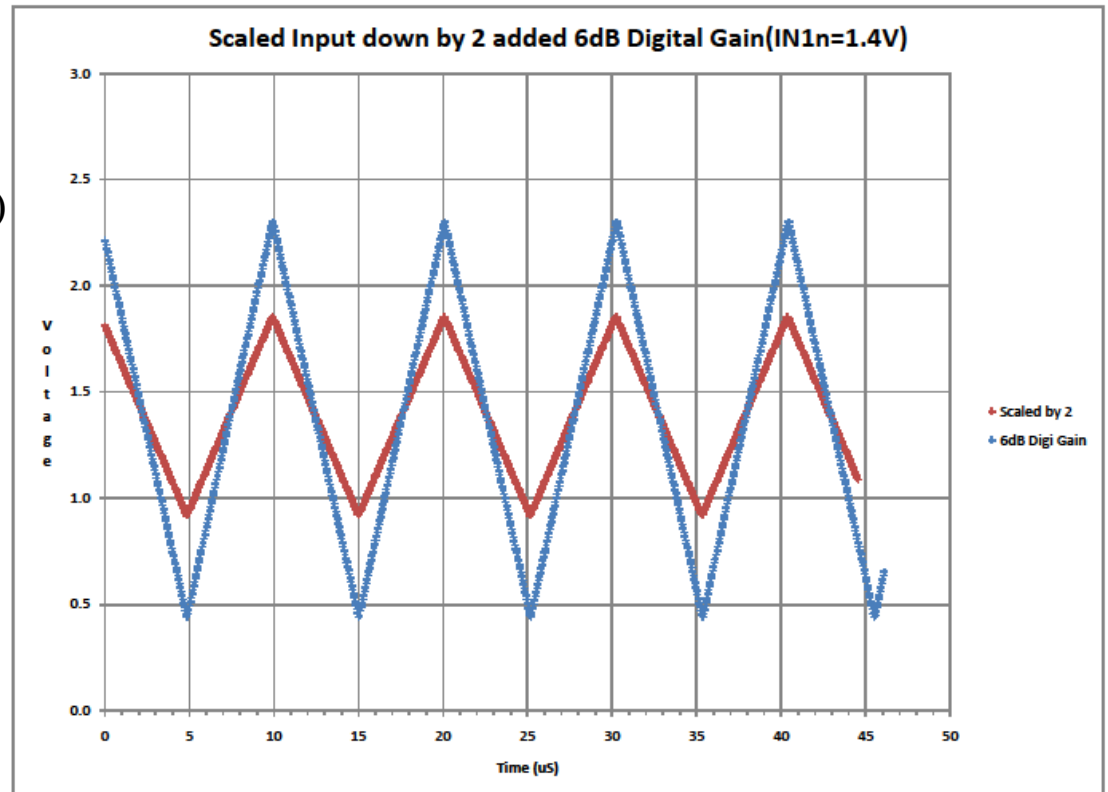
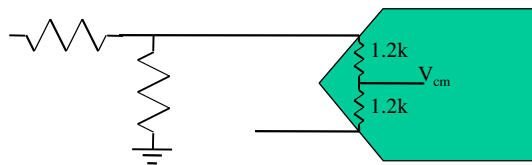
- Currently 1.8V
- Max ~2.0V
- Min ~1.2V (maybe 1.0V)

### ▪Drive Capability

- Small (few mA at best)

## •Scaling:

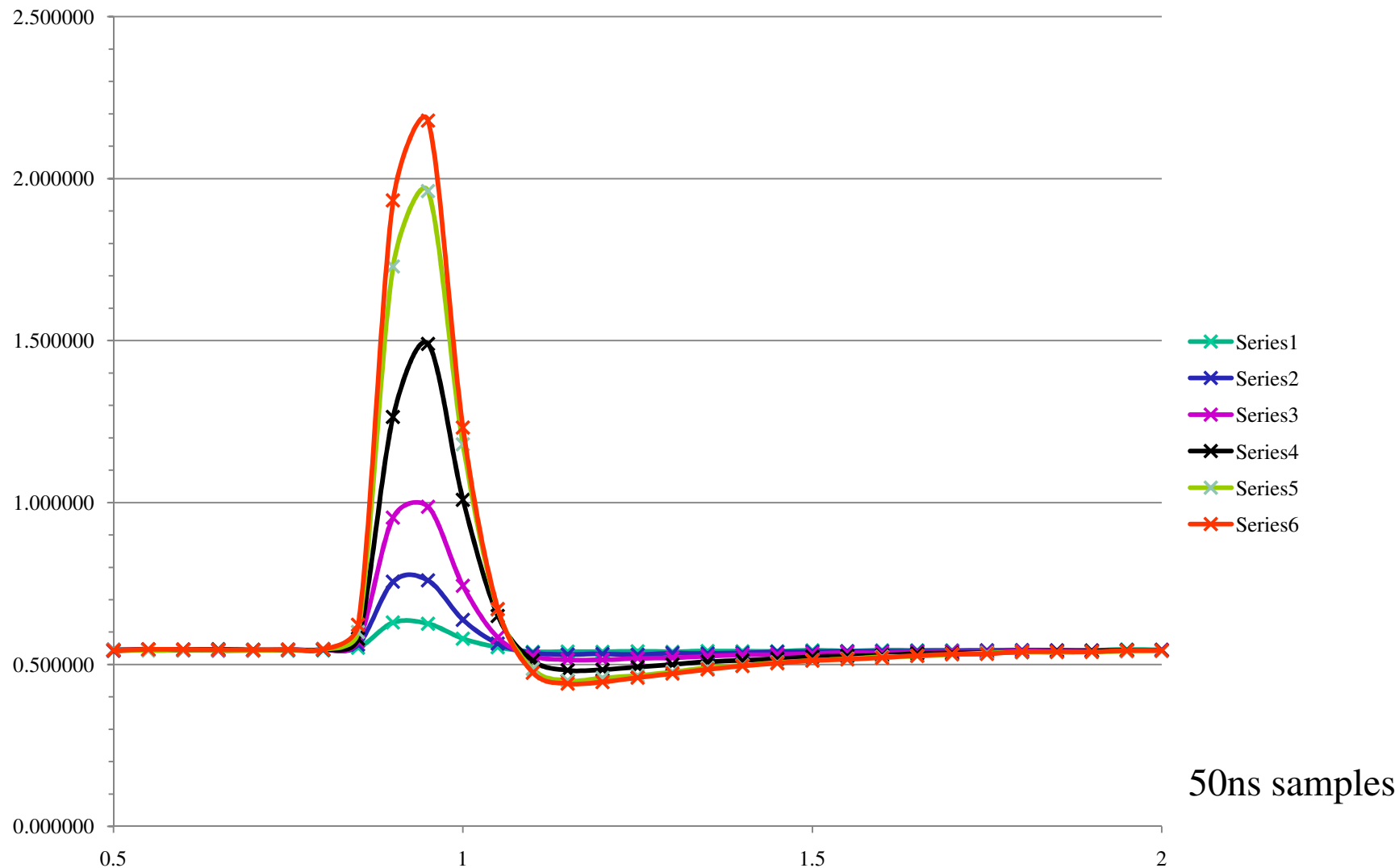
- Scale down input
- Add digital gain on output
- Resistor divider





# Digitize Amplifier Pulses

Connect CFEB to Evaluation Board:







# DCFEB Prototype

Build prototype with four options for preamp/ADC interface

Options include:

- Direct Coupling with scaling
- AC Coupling with scaling
- Single to Differential with Analog Devices ADA4950
- Single to Differential with TI THS4524

DAQ path:

- Virtex 5 or 6
- Data sent in MAC level ethernet packets

Trigger path:

- Three options (see slide 4) fiber or copper?
- Major concern is additional latency (seems unavoidable)
- Other concerns: additional components/power consumption
- On TMB end: compatibility with mezzanine board



# Related Work

## Changes on ME1/1 to accommodate DCFEBs:

- 7 DCFEBs, same form factor (scheme exists)
- Copper (and fiber) cables from DCFEBs to patch panel
- New patch panel (copper cables 7 to 2)
- New LVDB (power requirements TBD)

## Peripheral Crate:

- New DMB (PCB design relatively straight forward)
- New TMB (dependent on comparator transfer scheme)

Decisions need to be made but should not be rushed