

Endcap Muon (CSC) Trigger Phase I and II Upgrade Plans and Status

Ivan K. Furić
University of Florida

on behalf of the CSC Detector and Trigger communities

Overview

- CSC - “low” occupancy in LHC running
- utilized in design of trigger, DAQ data flow
- SLHC challenge: handle internal rates, control trigger?
- **Phase I:**
 - **Detector upstream:** trig primitive quality good enough, focus is on handling increased rate
 - **Track Finder:** handle increased rate + improve CSC standalone momentum resolution
- **Phase II:**
 - **Detector upstream:** relax upper limits on number of trigger primitives (another internal rate increase)
 - **Track Finder:** combine CSC and tracker information for ultimate momentum resolution

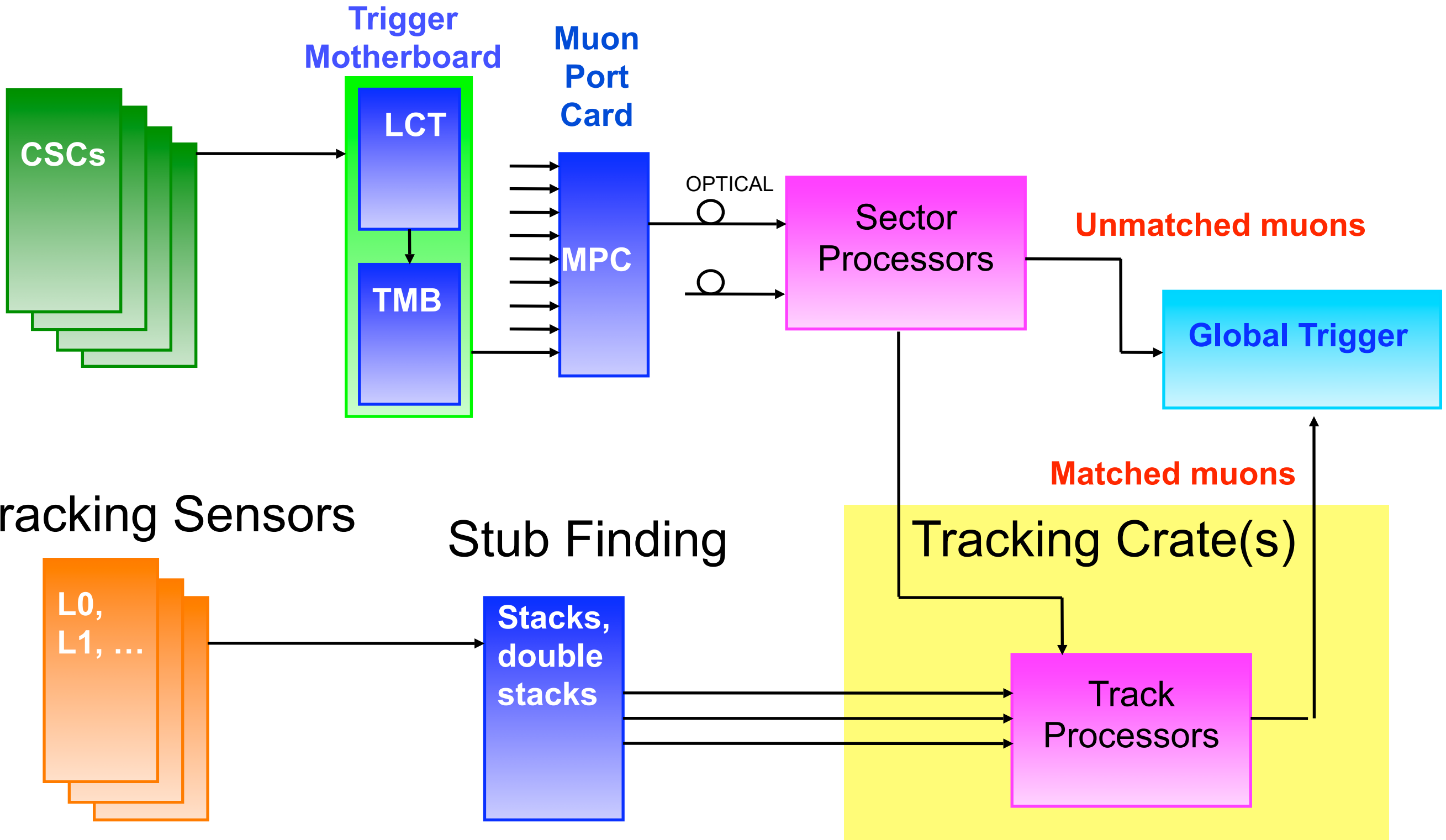


Dataflow Architecture Sketch

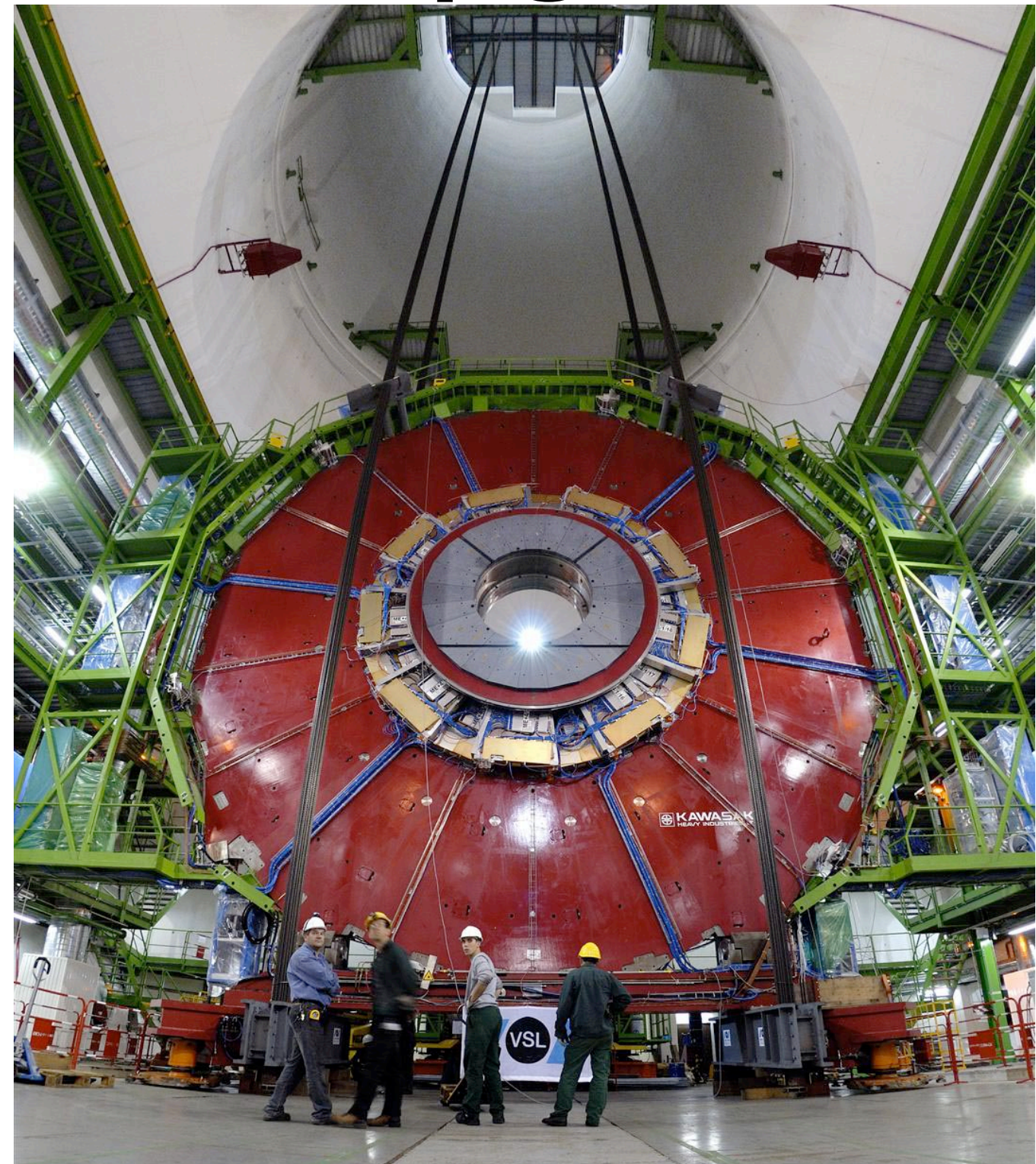
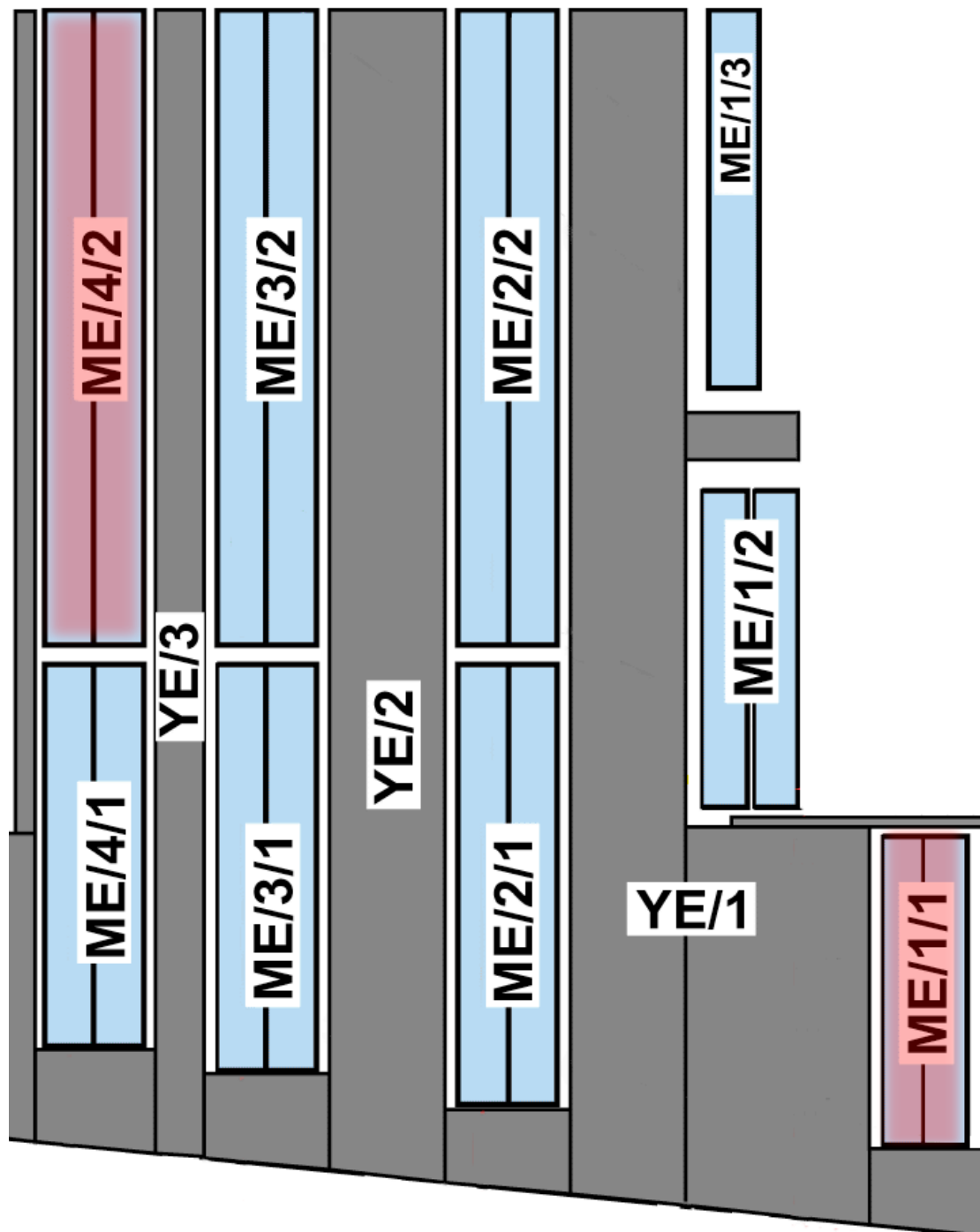
Chambers

Peripheral Crates

CSC Track-Finder Crate



ME4/2 and ME1/1 upgrades

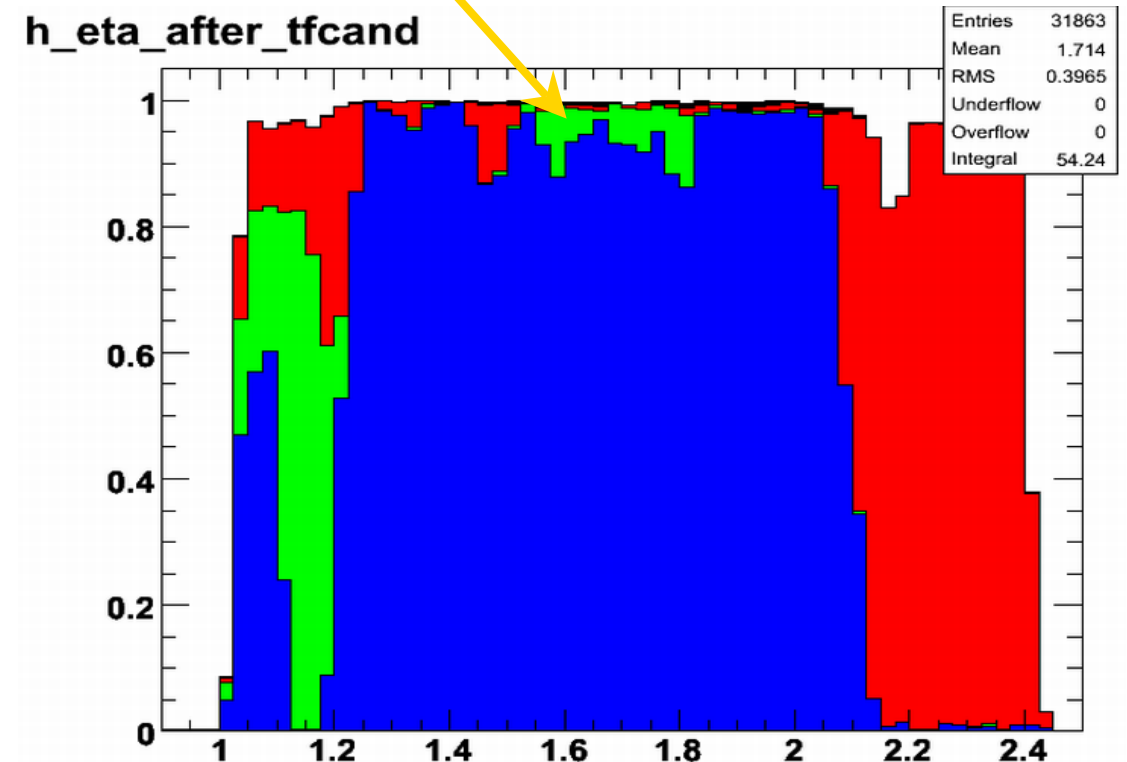
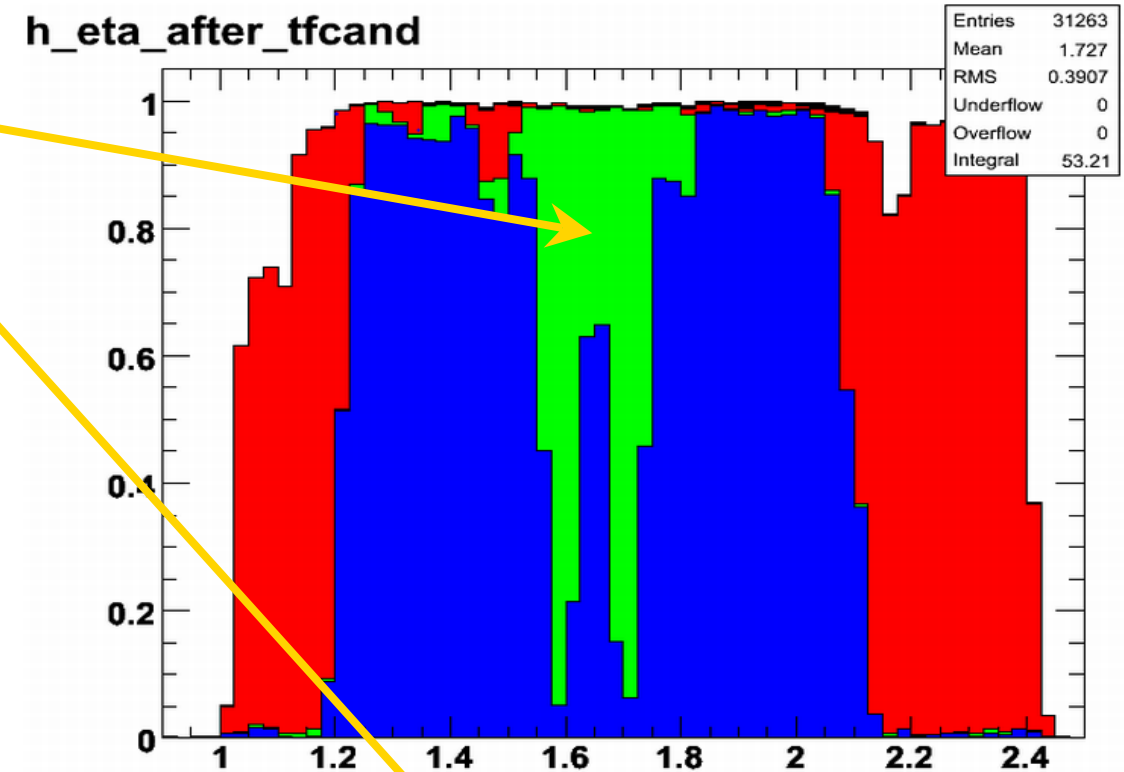


“Empty” YE3 disk ready for ME4/2

Simulation result (May '09)

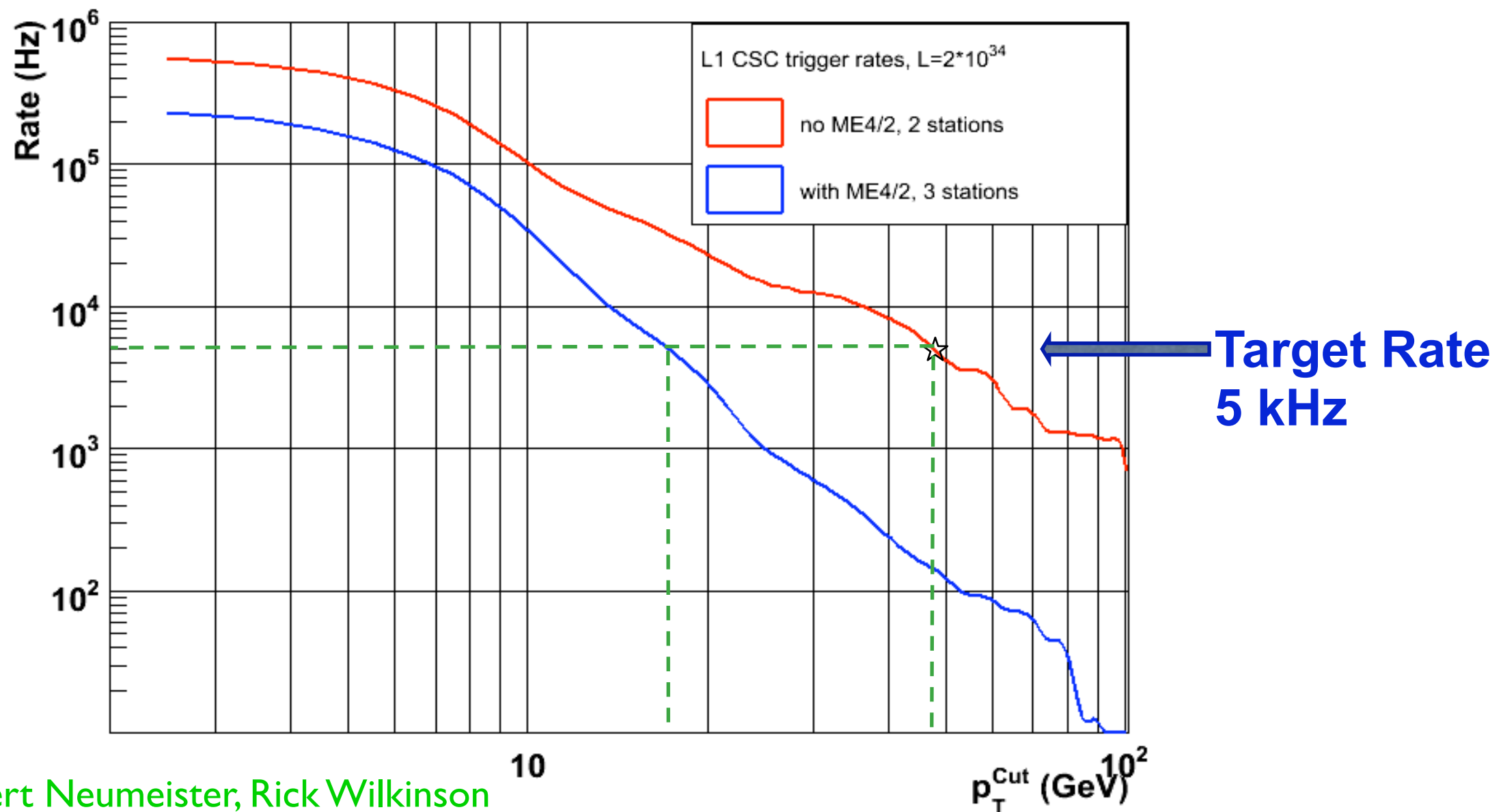
(Vadim Khotilovich, Alexei Safonov)

- Efficiency gaps for good quality TF tracks disappear with addition of ME4/2
- ME4/2 will be included by default in 31X
- Back-porting to 22X took a considerable amount of effort
- Thanks to the experts: Rick Wilkinson, Tim Cox, Oana Boeriu and Slava Valuev!



ME4/2 upgrade motivation

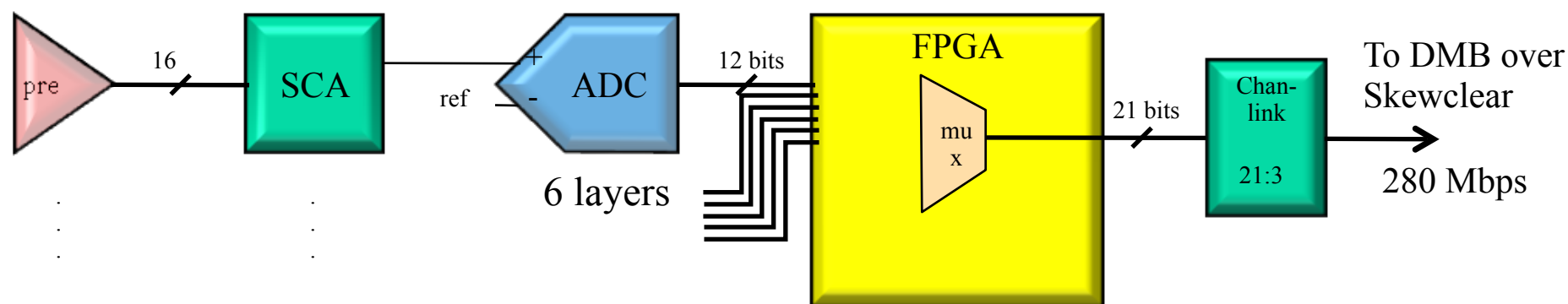
- Triggering with & without the ME4/2 upgrade:
 - The high-luminosity Level 1 trigger threshold is reduced from 48 \rightarrow 18 GeV/c



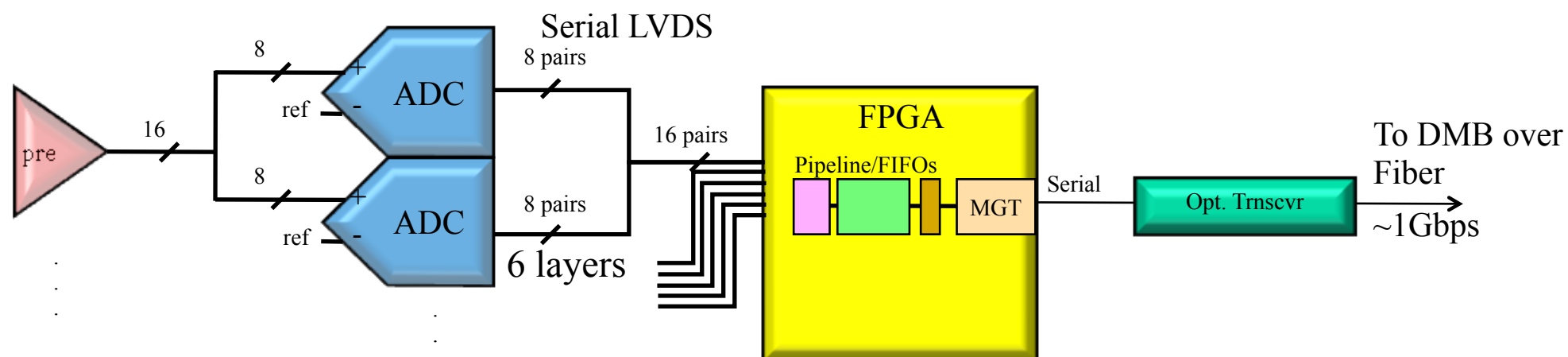


“Digital CFEB” cathode board

- **CSC principle: digitize cathode charges to ~1%, interpolate for fine position**
- **Current CFEB: the ADC is multiplexed 16:1**
 - Requires analog charge storage ASIC (SCA)
 - Serial digitization after L1A



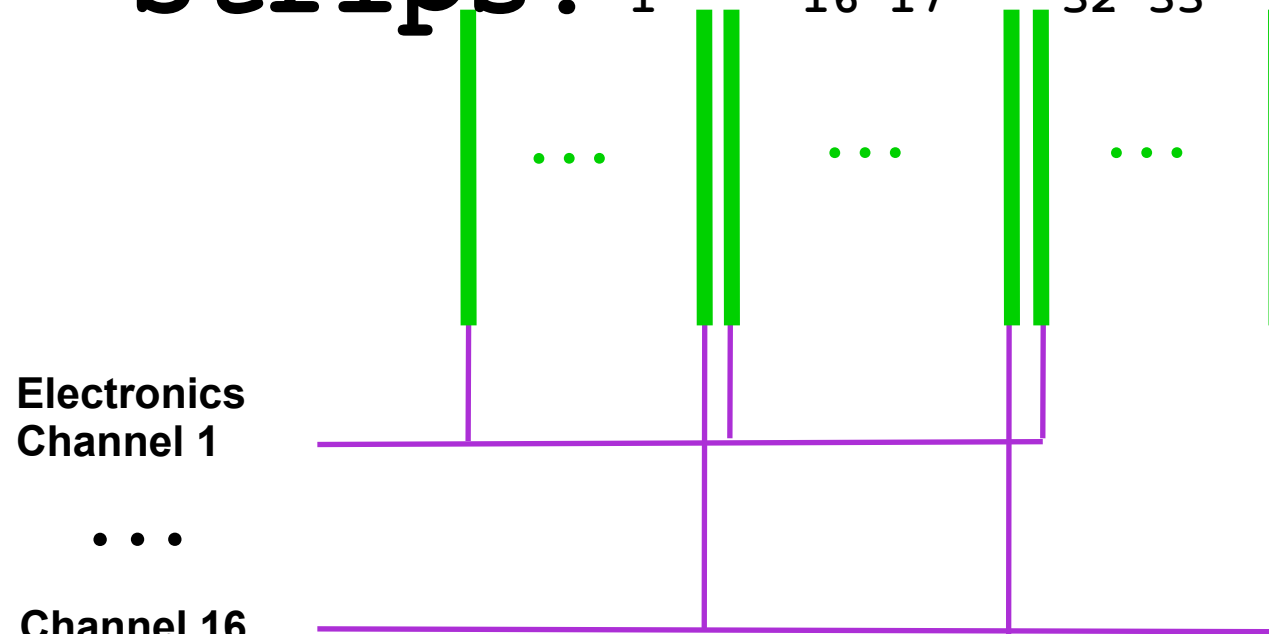
- **Digital CFEB uses Flash ADCs:**
 - Continuous and deadtimeless digitization



MEI/I Restoring η 2.1-2.4

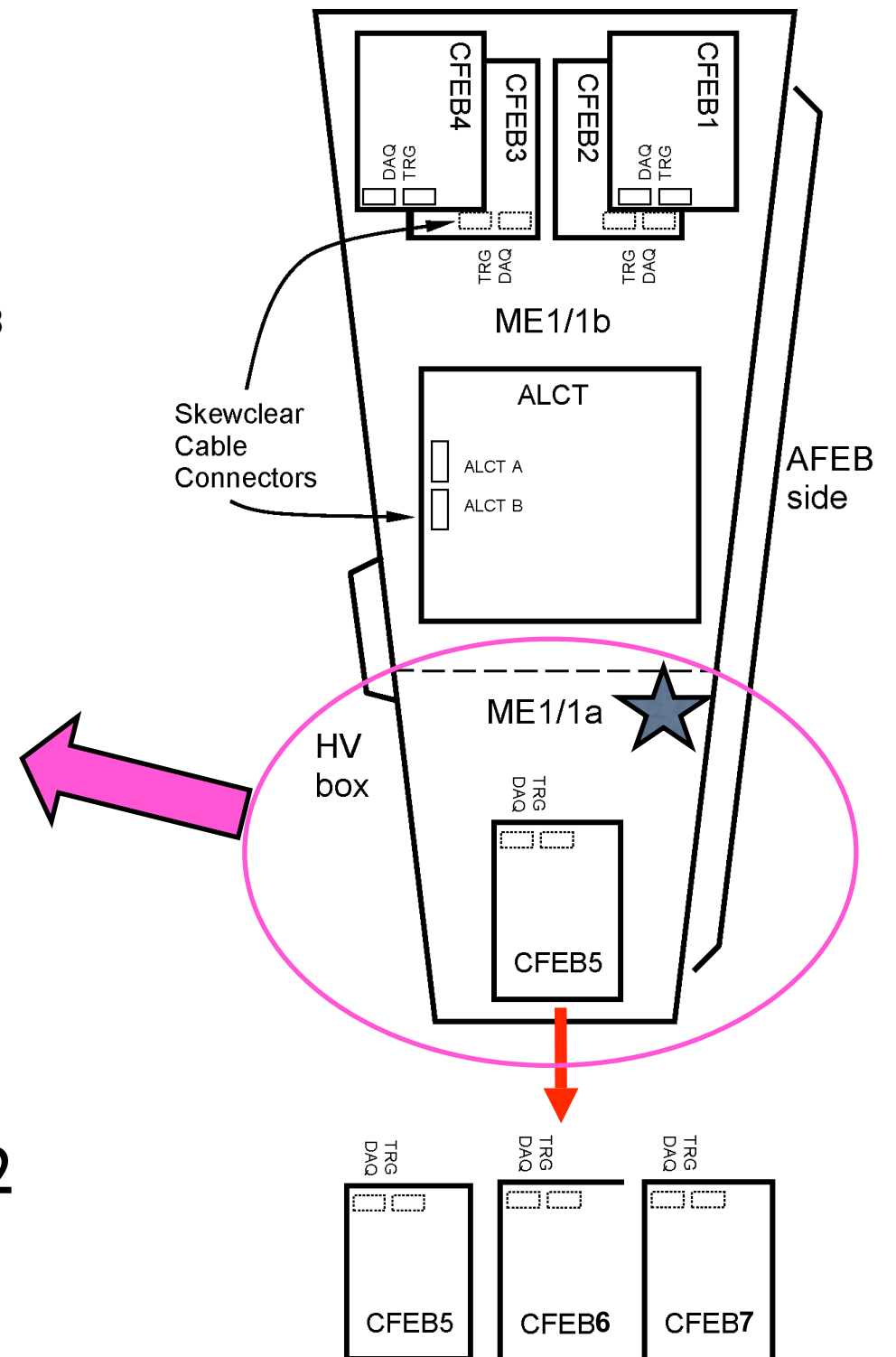
- High- η section of MEI/I
- Cathode strips are currently ganged 3:1

Strips: 1 16 17 32 33 48

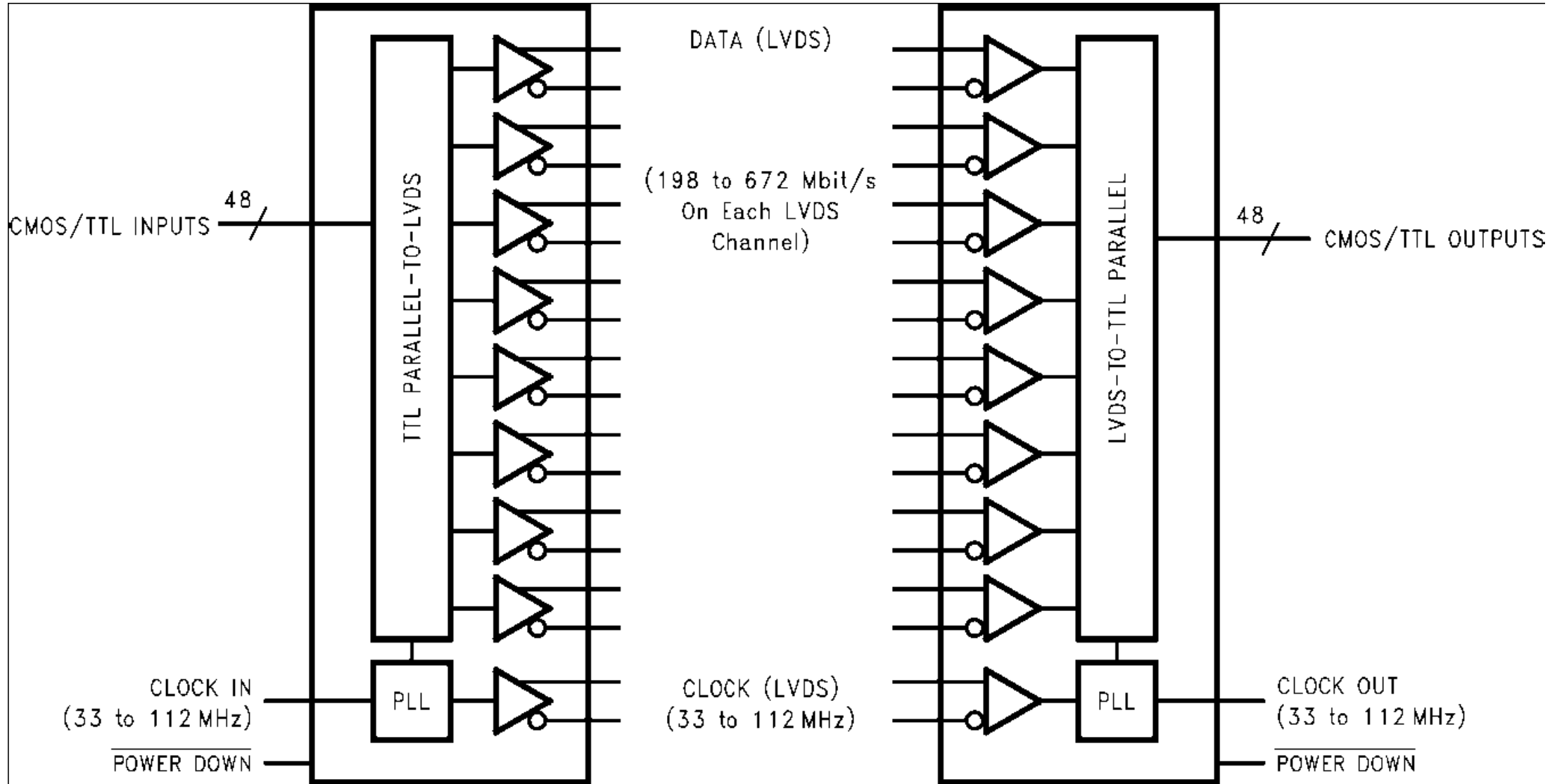


- **Plan:**

- Install DCFEB boards on MEI/I
- Move existing CFEBs from MEI/I to ME4/2
- Takes ~2.5 months per endcap
- **72 new TMB and DMB boards needed to accommodate additional inputs, optolinks**

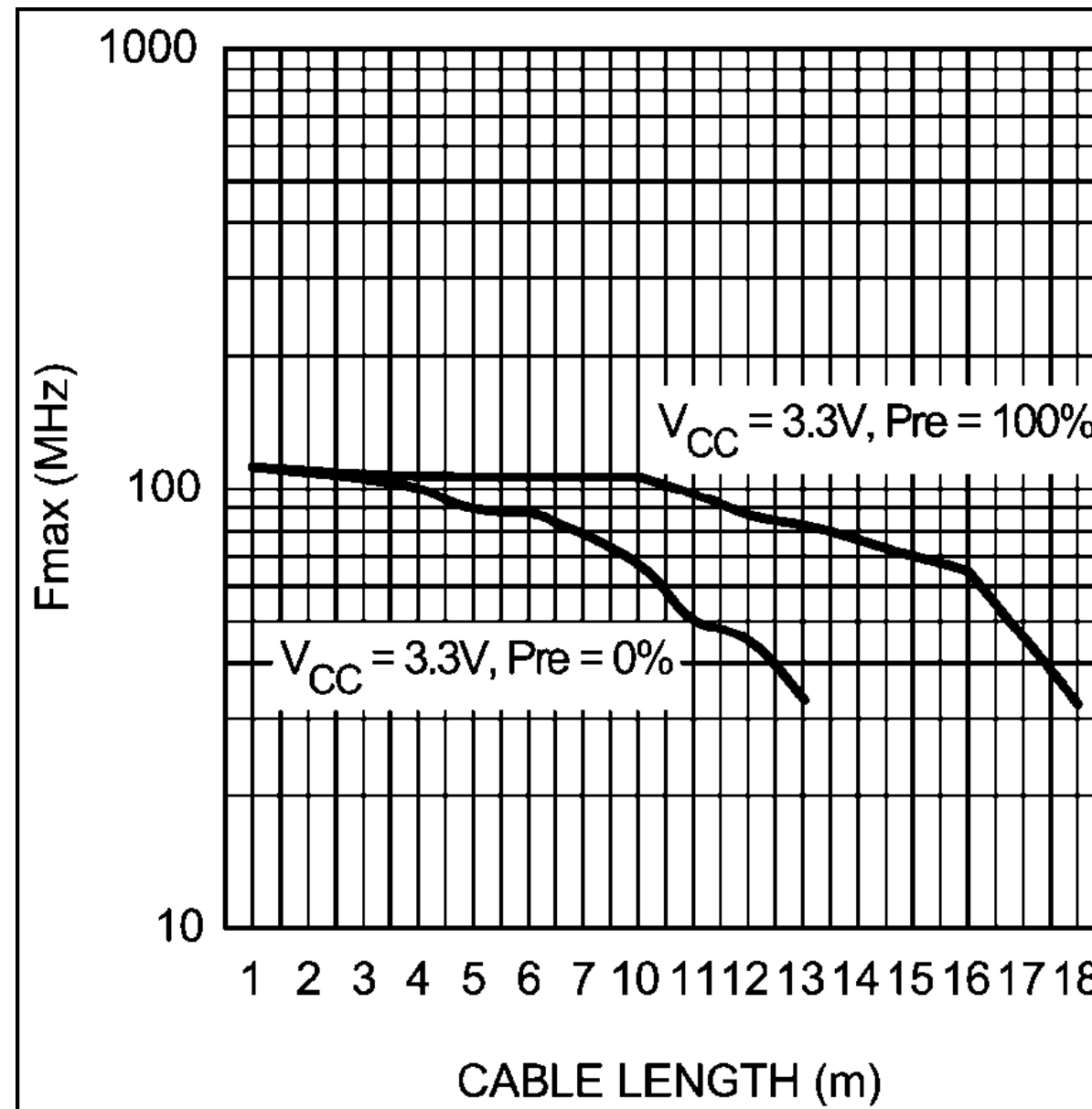


Comparator dCFEB-to-TMB option



- Channel Link: **DS90CR483/484A**
- 48-8 bit Ser/Deser, requires **19 conductors** per CFEB
 - Use 20th conductor as “cable detect” to control Power-Down
- Has options for **pre-emphasis and DC balancing**
 - Provides for reliable operation, even on our longest cables
- **Adds ~3 BX to the trigger latency (~same as Fiber options)**

Channel Link Performance Spec



- Performance exceeds our needs: 14 m cable @40 MHz
- Use the same 50-pin SkewClear, 5 cables to TMB!
 - Each cable can carry one OR two CFEB's comparator bits
 - Two-CFEB case gets appropriate fan-out at MEI/I Patch Panel

TMB-to-MPC

For MEI/I the rates are very high...

- How to send 4 LCTs per BX to MPC?
 - Efficiency will suffer if we don't do this
- Review Virtex-5 capabilities: SelectIO
 - Up to 800 Mb/sec on single ended lines
 - Up to 1250 Mb/sec on differential lines

Using current backplane resources, what can we do?

- Consider differential signals at 320 Mb/sec, FPGA-to-FPGA:
 - Must go from one mezzanine connection to the other...
 - ...through two backplane connectors!
 - This will double the bandwidth, allows 4 LCTs per BX
 - Requires much “proof-of-concept” testing
 - Is it reliable? Should we abandon the mezzanine?
 - Signal distance is only ~0.5 m: Can it work?

Port Cards

- Current design is adequate for LHC luminosity
 - 2 LCTs (di-muon signal) + 1 (background) = **3 LCTs per Port Card per BX**
- With luminosity upgrade, we expect **~7 LCTs per Port Card per BX.**
 - Preliminary simulated data, no measurements so far
 - Reality could be **worse**
- Port Card becomes a **bottleneck**
- Solution:
 - Keep 2 Trigger Primitives per chamber
 - Bring all LCTs to SP (**18 per Port Card per BX**), no filtering
 - May keep the filtering option in Port Cards, in case it's needed
- Port Cards have to be redesigned and replaced system-wide
 - Faster data links evaluated.

Trig. Primitives → Coordinates

- Presently, conversion is done using large LUTs
 - 4MB per primitive
- For upgrade:
 - Using large LUTs impossible: too much memory
 - Make conversion inside FPGA
 - Combine LUTs and logic to reduce memory size
 - Use θ instead of η
 - Using θ allows for uniform angular extrapolation windows, no need to adjust them depending on θ

Track reconstruction logic: Expanding Current design

| Module | % in current design | increase factor | % upgraded |
|---|---------------------|-----------------|--------------|
| Multiple Bunch Crossing Analysis (BXA) | 8% | 36 | 282% |
| Extrapolation units (EU) | 23% | 11 | 262% |
| Track assembly (TAU) | 1% | 4.5 | 4% |
| Track parameters assignment (PAU) | 13% | 4.5 | 57% |
| Sorting, ghost cancellation (FSU) | 51% | 20 | 1012% |
| Output Multiplexor (MUX) | 2% | 4.5 | 9% |
| BX adjustment to 2 nd trig. primitive (BXCORR) | 2% | 1 | 2% |
| Total | 100% | | 1628% |

Total upgraded design size relative to current: about 16 x bigger

Main contributors: FSU, BXA, EU

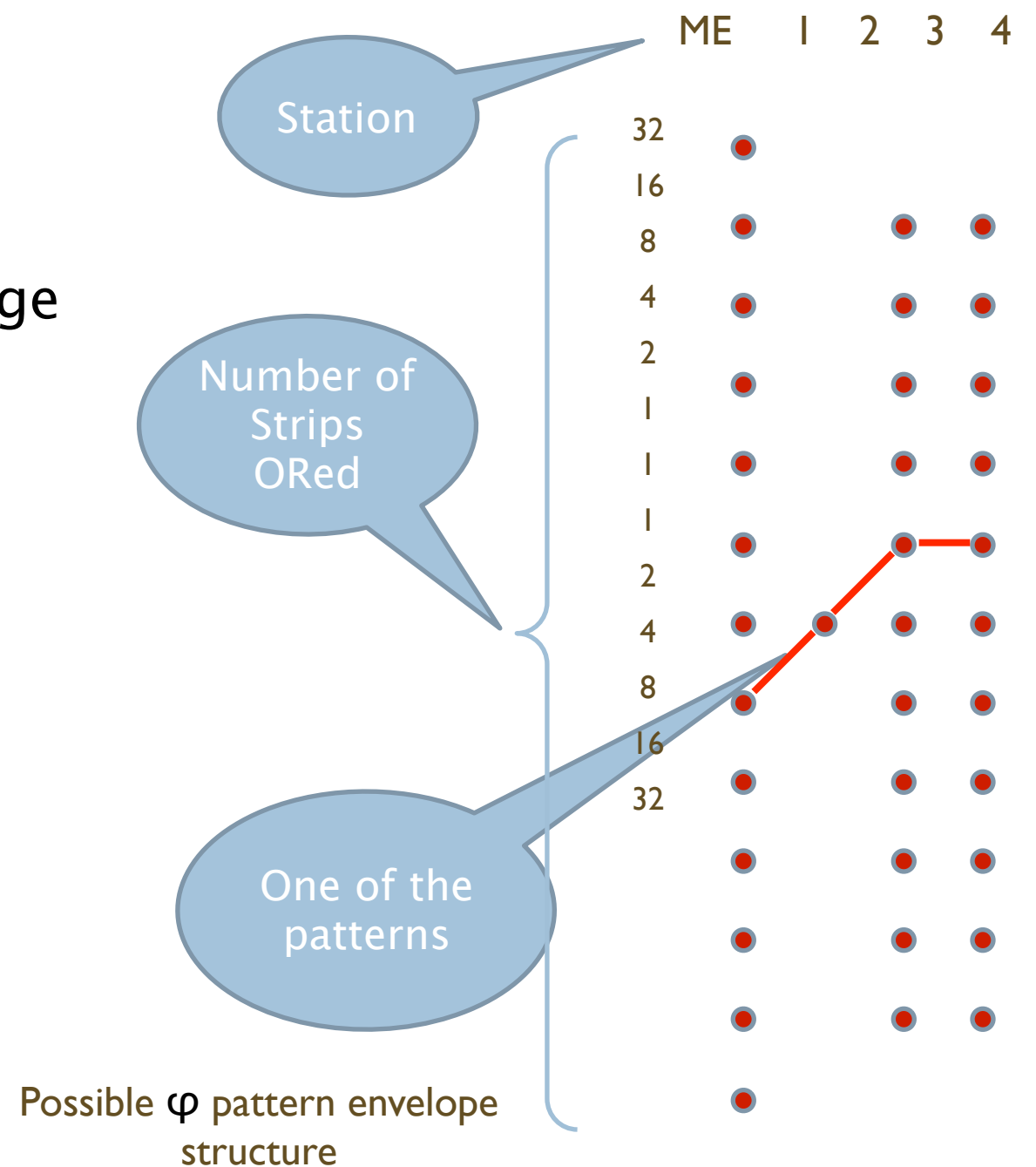
That's too big, may not find suitable FPGA for reasonable cost.

Pattern-based TF

- Investigating another approach:
 - Pattern-based detection
 - Separately in φ and θ
 - Once the patterns are detected, merge them into complete 3-D tracks

- **Benefits:**

- Logic size reduction
- Certain processing steps become “natural”, logic for them is greatly simplified or removed
 - Multiple Bunch Crossing Analysis
 - Ghost Cancellation
 - Automatic track timing on 2nd trig. primitive



Pattern-based finding

Raw hit reconstruction

φ and θ pattern search

φ and θ pattern match

Sorting

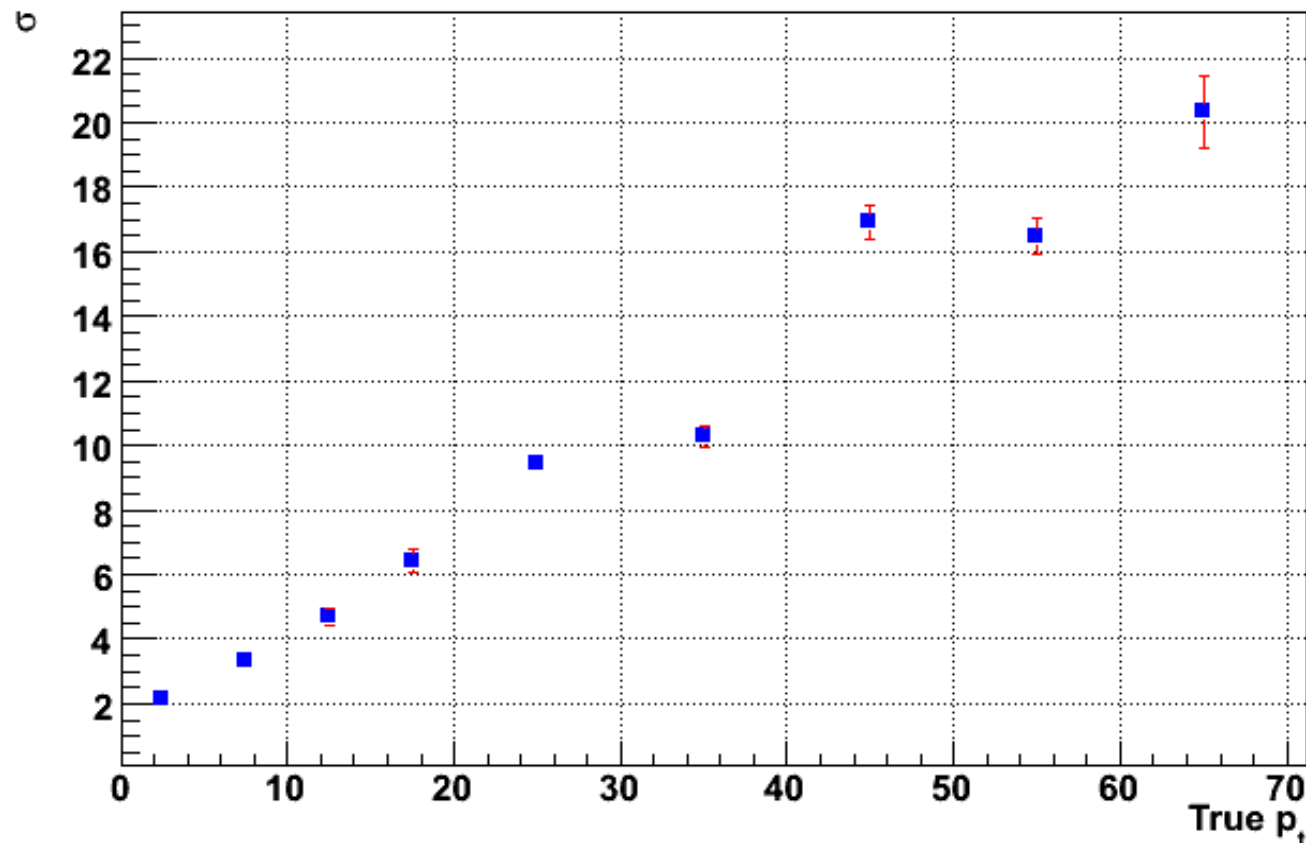
Trigger primitive matching

Precise parameter
assignment

- Similar to pattern search logic in front-end boards (ALCT)
- Sector is split to 5 φ zones and 6 θ zones defined by chamber coverage
- Patterns detected independently in each zone
- Best φ and θ patterns matched together to make 12 track candidates
- Best three are selected by sorting logic
- Corresponding trig. primitives found, precise parameters assigned.

CSC TF Resolutions

Widths from Δp_t fits (Q=3)



- p_T resolution of TF:
current LUT's - 40%
- better LUT's developed, not deployed yet - 30%
[E. Berry (Princeton), A. Kropivnitskaya (UF)]
- design predictions - 20-30% below 30 GeV/c

Further Improvements

- There is unused information in the TF fit:
 - phi information is truncated in fit
 - ignore track direction in chambers
 - ignore staggering in Z of chambers
 - eta information truncated to 4 bits in fit
 - segment quality ignored
- room for further improvement of CSC standalone track finding
- follow up with simulation work to estimate impact

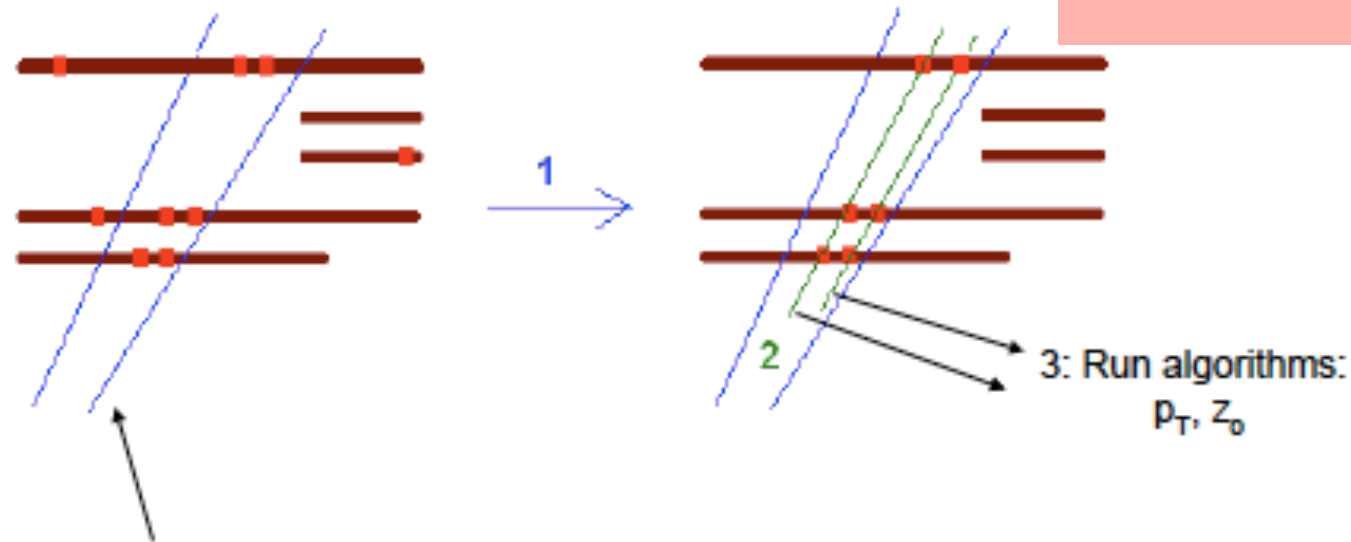
Phase I Summary:

- Detector electronics upgrades deal with increased internal rates and occupancy
- ME 4/2 increases high quality track coverage
- Track Finder expects significant I/O and processing challenge due to increased occupancy
- investigating pattern based approach as solution
- TF fit can incorporate more information to improve momentum resolution measurement
- follow up with simulations to evaluate impact
- Phase II studies found resolution important for track seeding window width, efficiency
- upgrade needs to incorporate both increased volume and better resolution - next major push

Phase II: CSC + Tracker Trigger

More details: talk by
B. Scurlock, Muon
Phase II session

Illustration



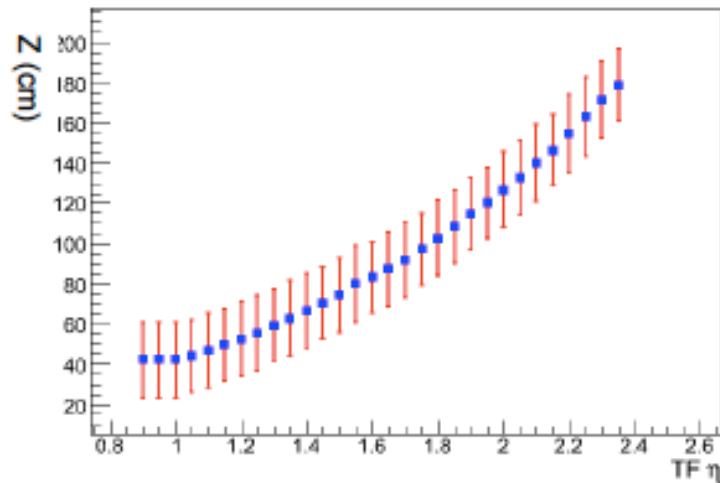
- Step 1: Use matching windows to cut stubs based on $\text{Trackfinder}_{z,\varphi} - \text{Tracker}_{z,\varphi}$
- Step 2: Only keep stubs that are correlated in $\Delta\varphi$ & $\Delta\cot\theta$ (ie $\varphi_{\text{dstack}2} - \varphi_{\text{dstack}0}$)
- Step 3: Apply r-z algorithm $\rightarrow \cot(\theta)$ & z_0 and r- φ algorithm $\rightarrow p_T$



CSC+Trigger Matching Windows

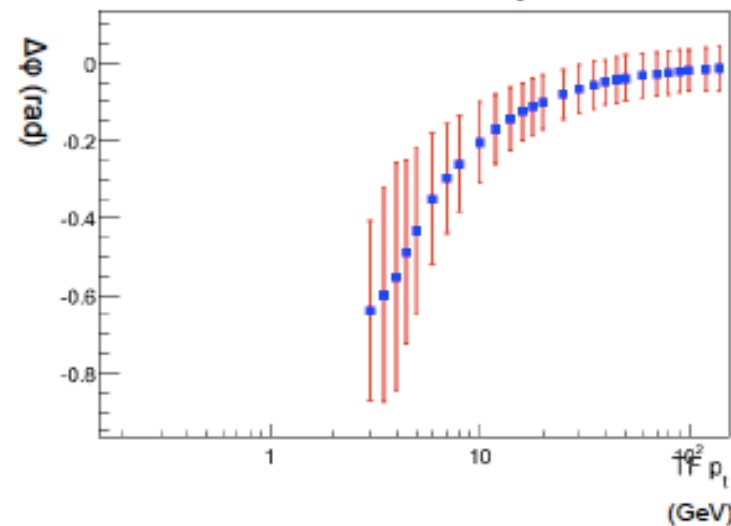
Examples of For Double Stack 0 :

Matching $Z_{tf}-Z_{tracker}$ Windows
For Double Stack 0



Widths ~ 6 cm

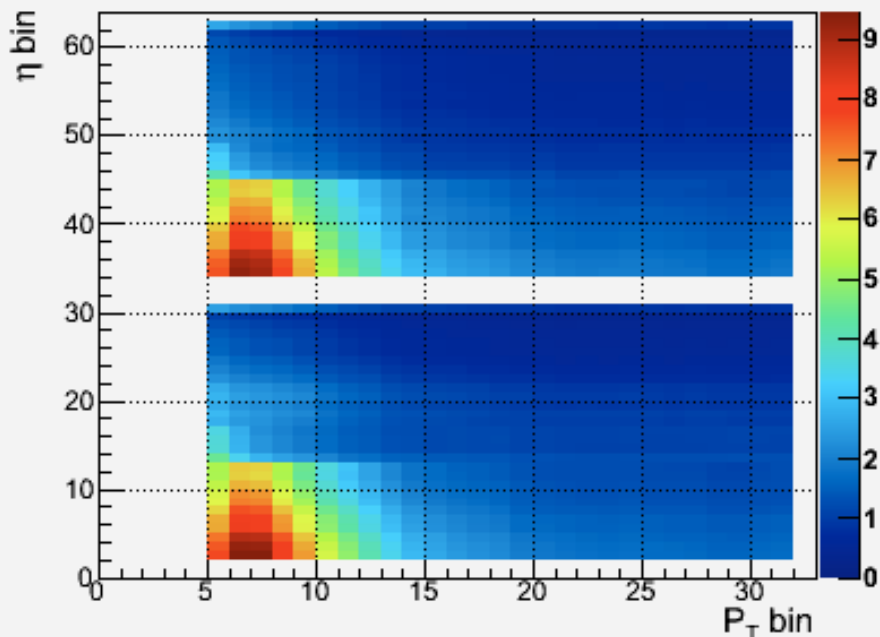
Matching $\phi_{tf}-\phi_{tracker}$ Windows
For Double Stack 0 $\eta < 1.5$



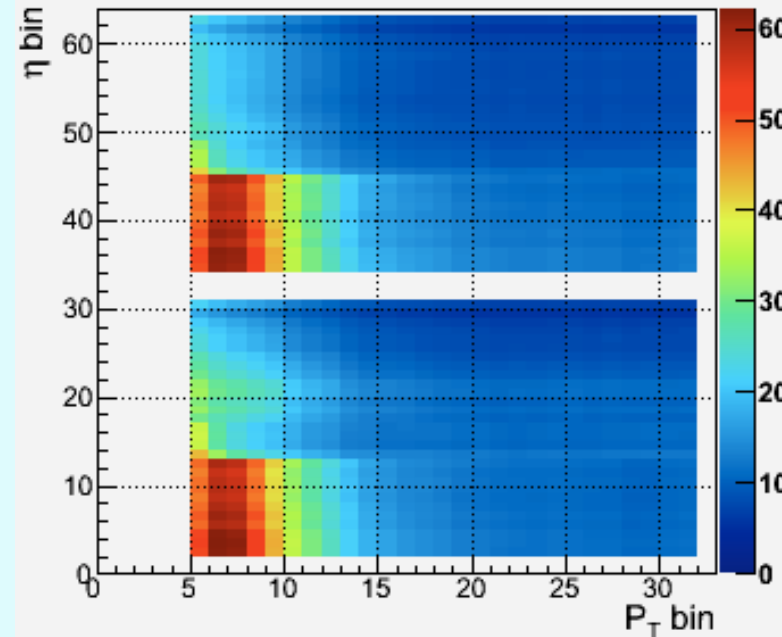
Widths = $O(\sim 0.1) - O(\sim 0.01)$ rad
 η dependence low p_T due to inhom. B-field
Can be tightened if necessary

Matching windows are defined for all possible CSCTF- P_T (5 bits) and CSCTF- η (5 bits per endcap) values. Average match-window-occupancy plots shown below are a function of these CSCTF bins and were made with min bias events (200 PU).

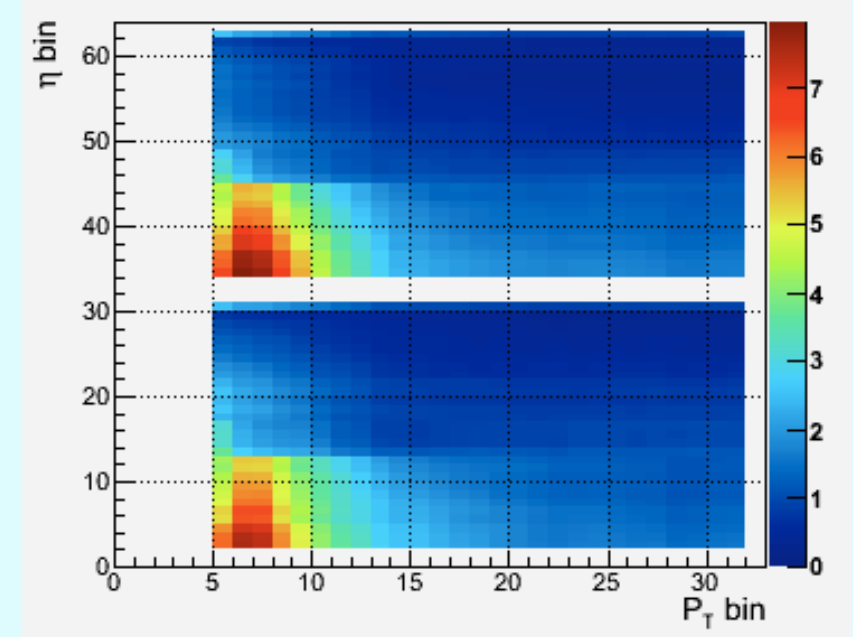
Stubs from simHits



Stubs from unclustered PixelDigs



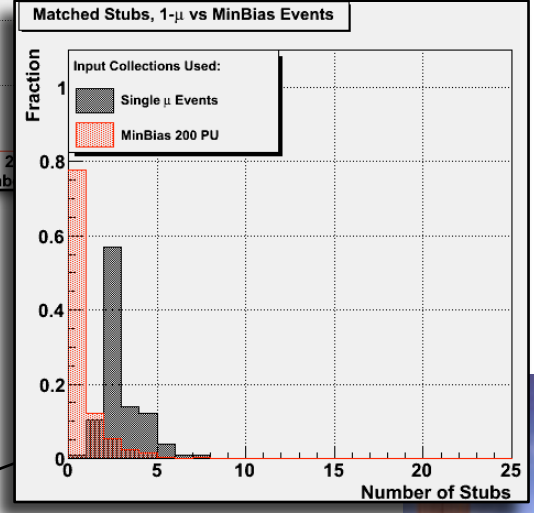
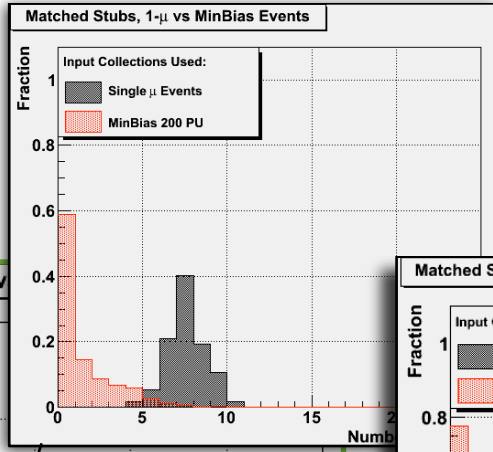
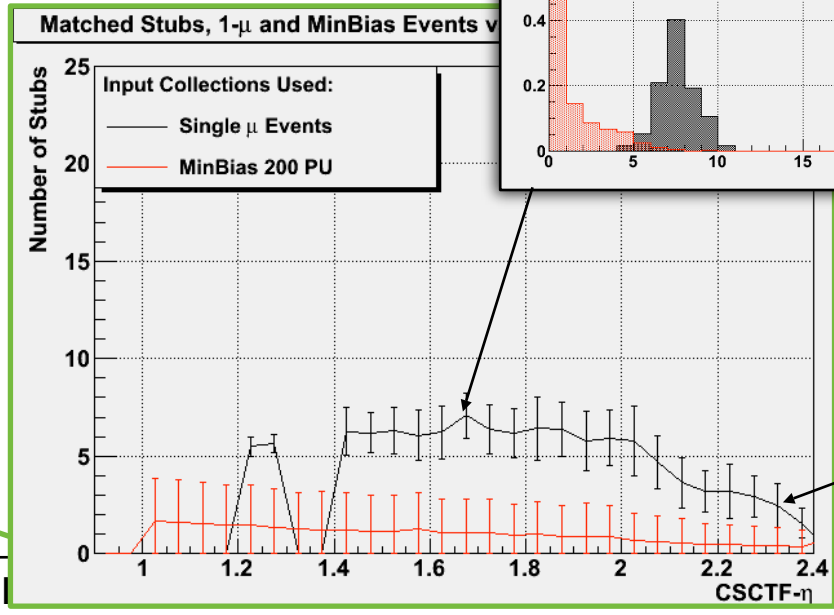
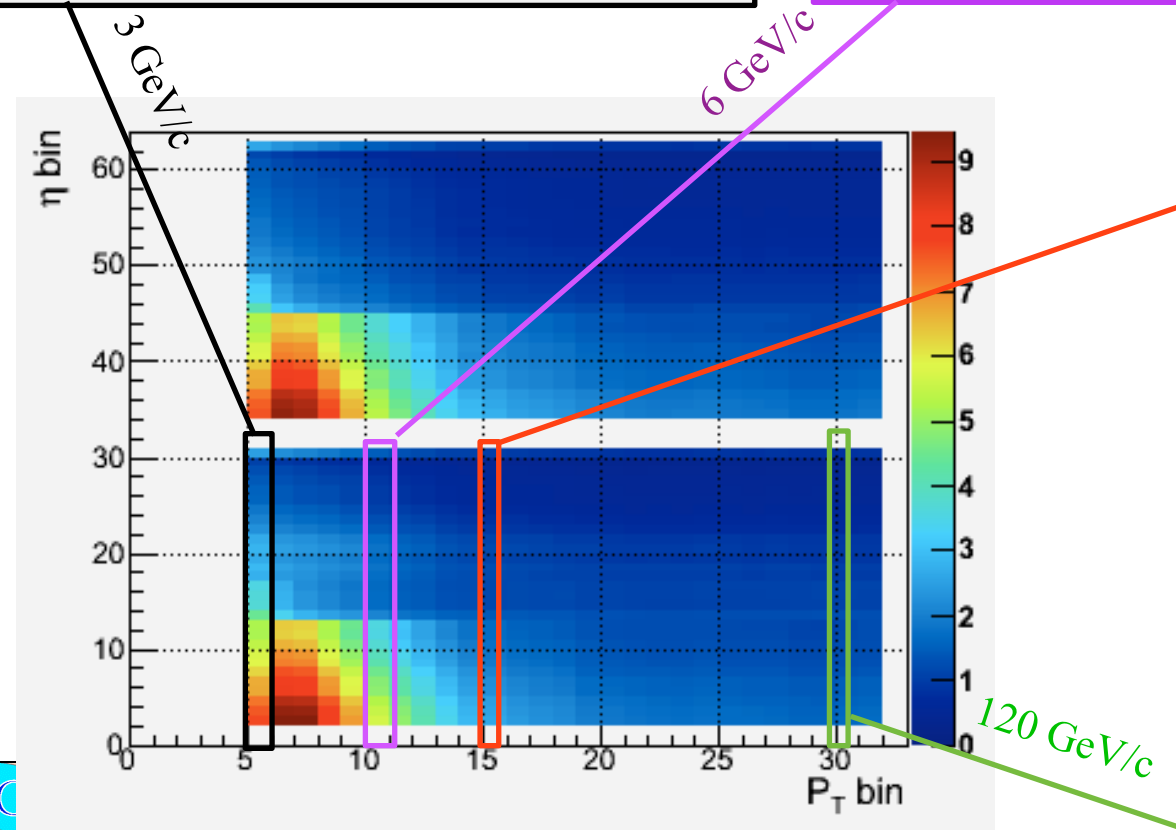
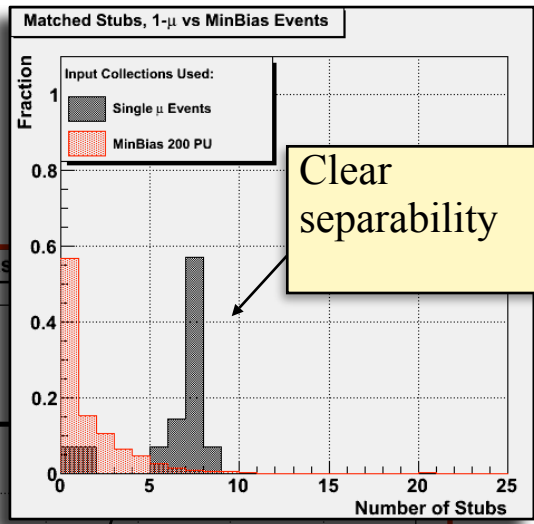
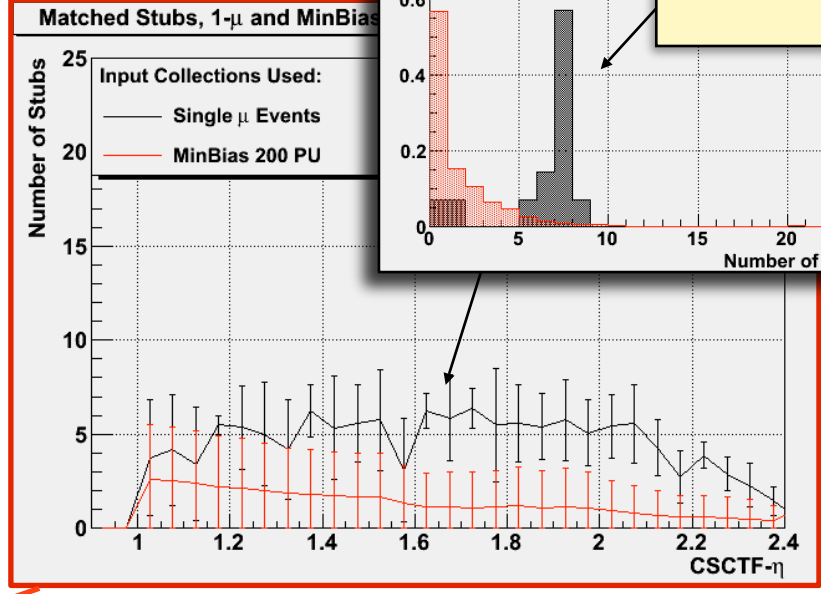
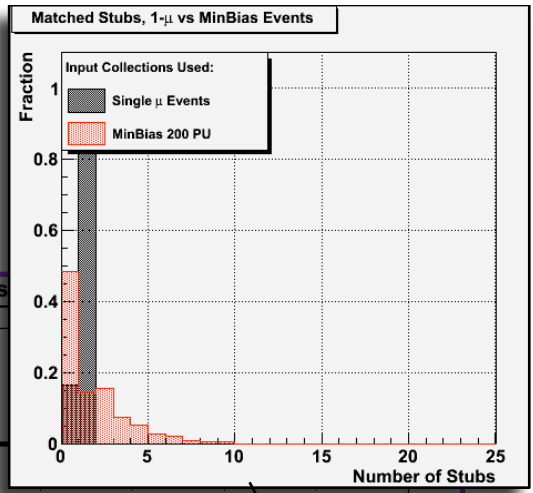
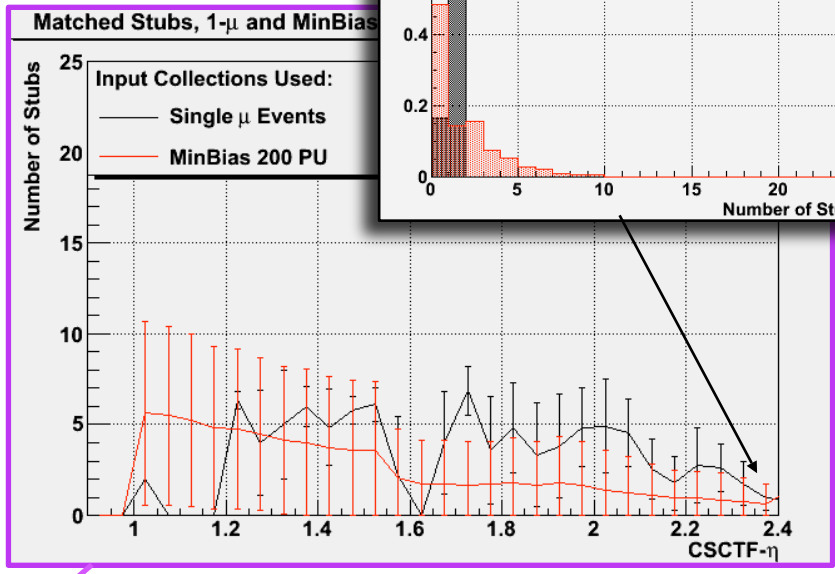
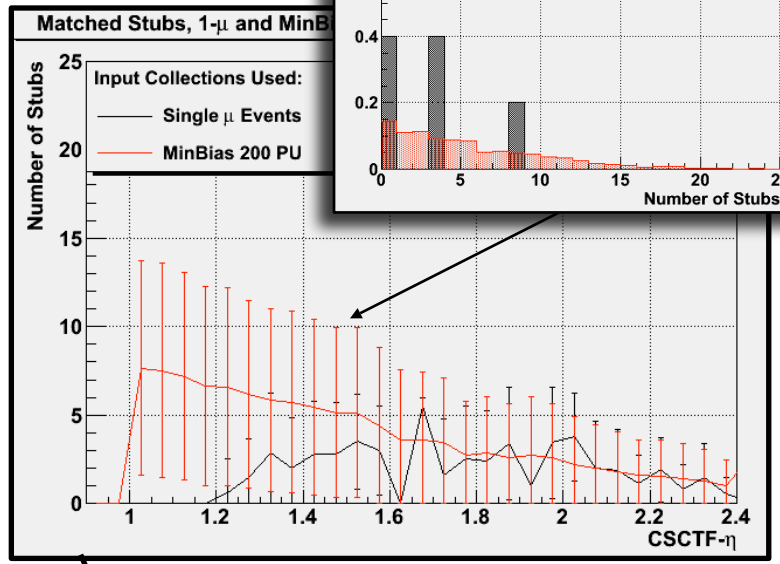
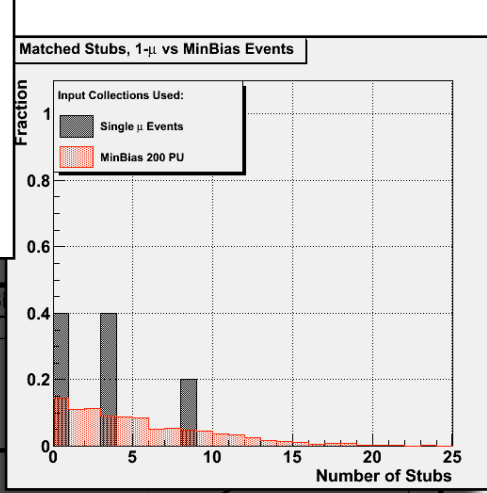
Stubs from clustered PixelDigs



Matching Windows: Signal versus Background

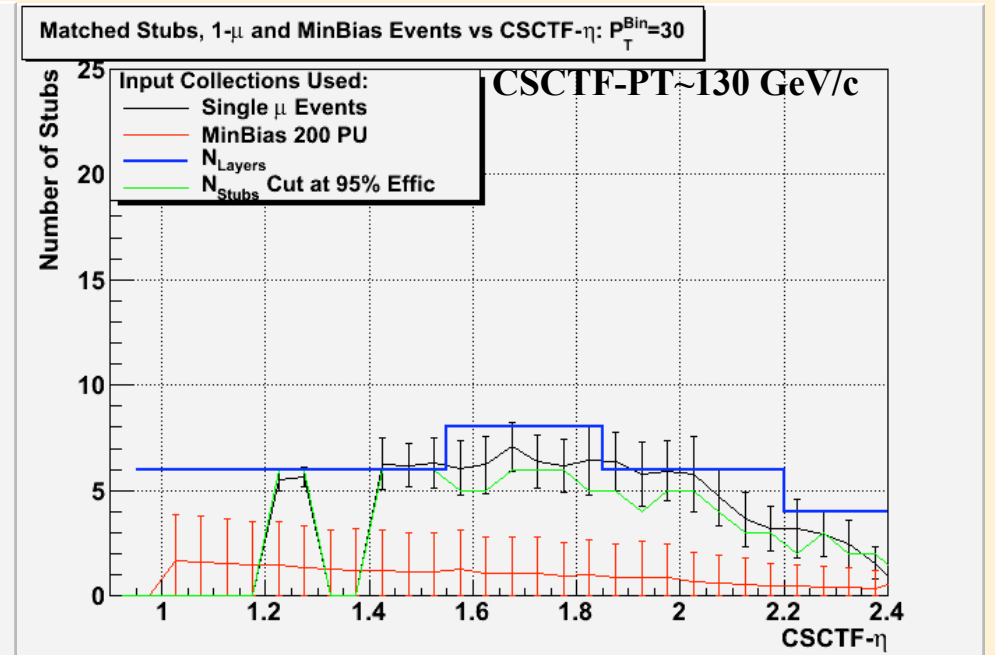
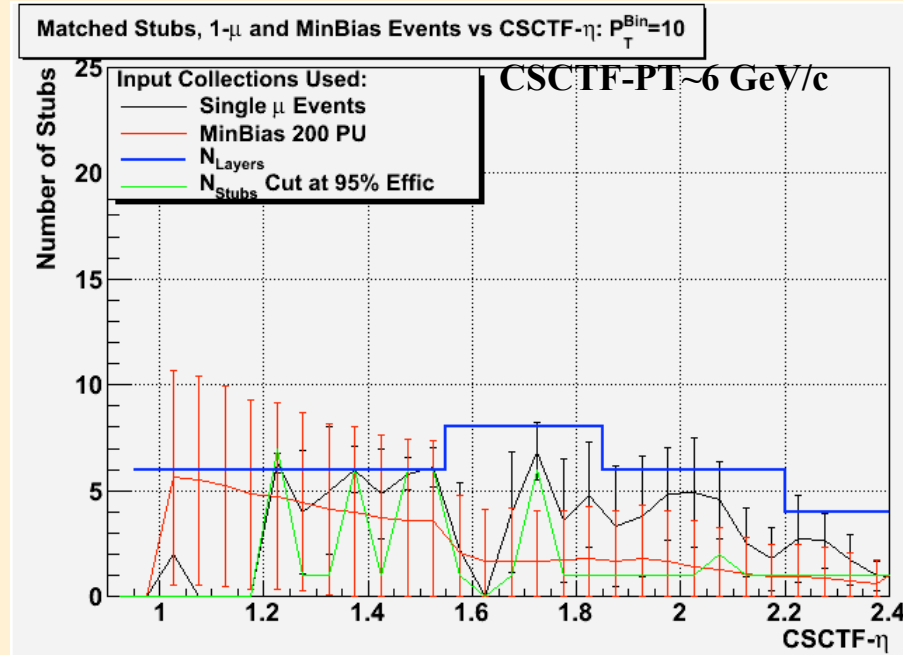
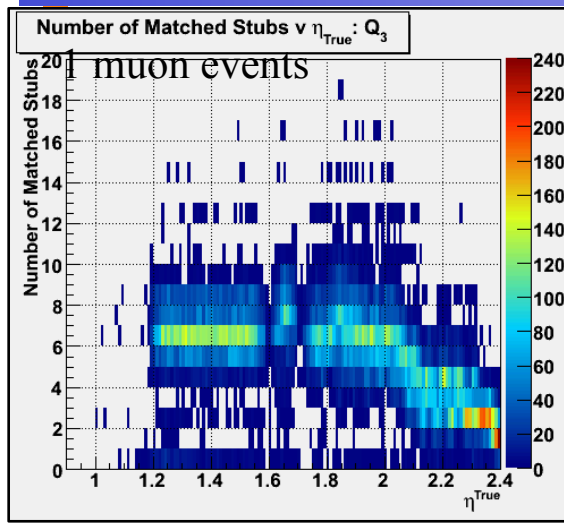
Single muon events

MinBias 200 PU
(randomly sampled
matching windows)



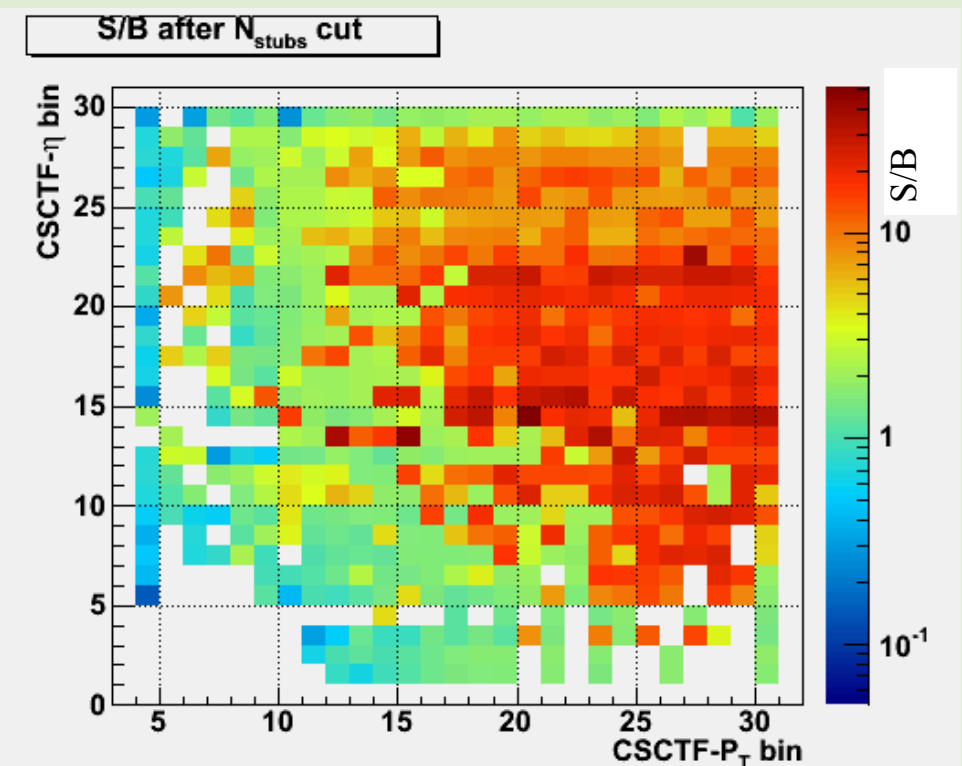
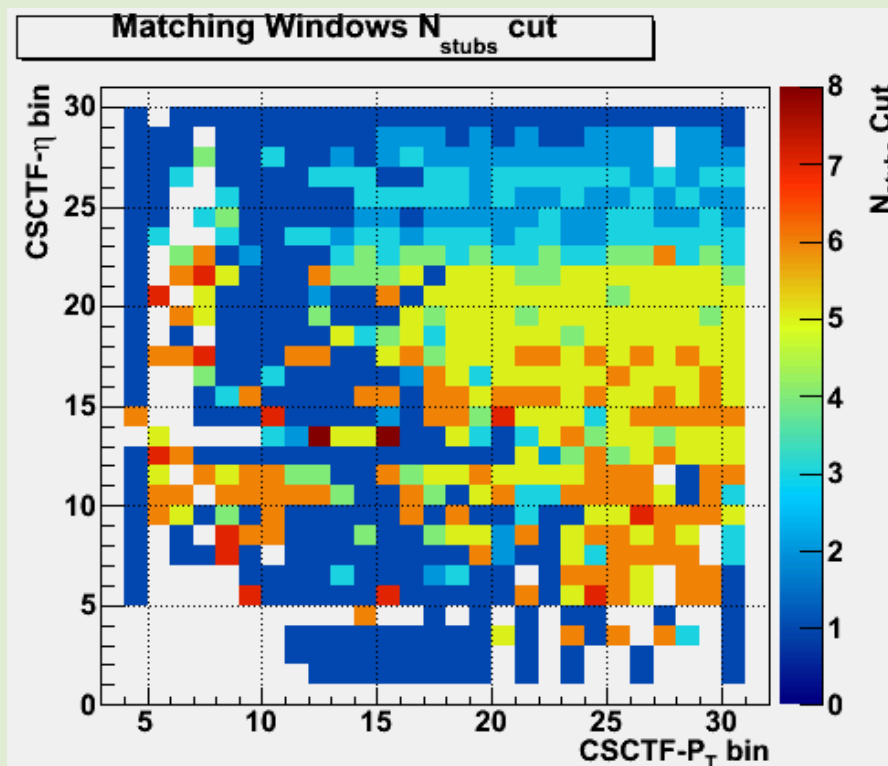
Matching Windows: Separating Signal from Background

Signal and Background vs CSCTF- η

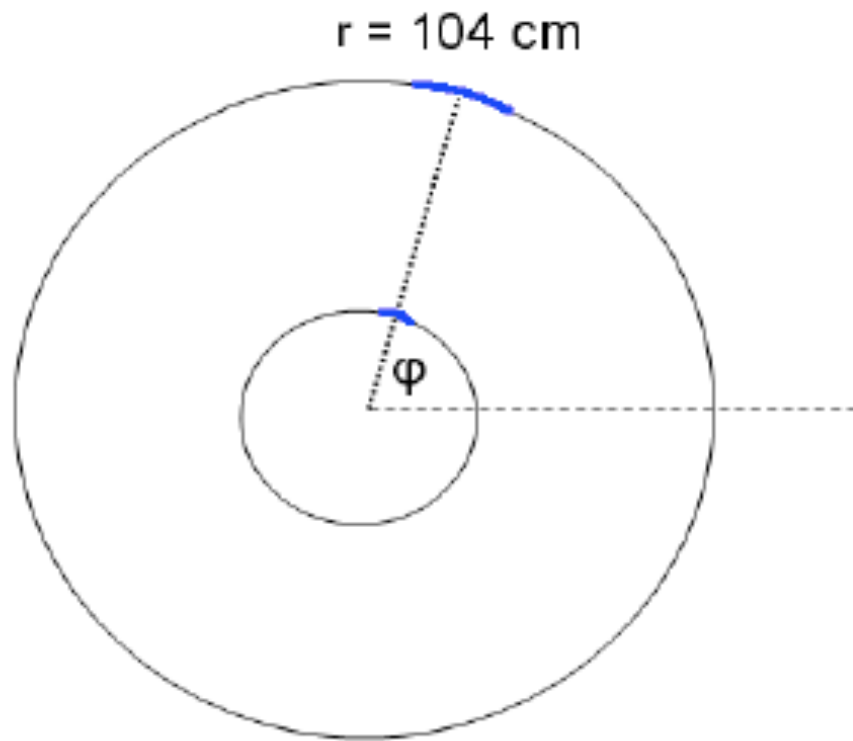


Once matching windows are re-tuned, expect that counting can provide a powerful handle for rate reduction from noise and CSCTF mis-measurement.

Example exercise: tune matching window bin-by-bin N_{stubs} threshold to accept 95% of signal stubs. Cuts and S/B versus bin seen on right \rightarrow



P_T Estimate 1: Using $\Delta\phi$



Circle Fit Approximation:

$$\phi = \phi_0 + \arcsin(\zeta R / p_T)$$

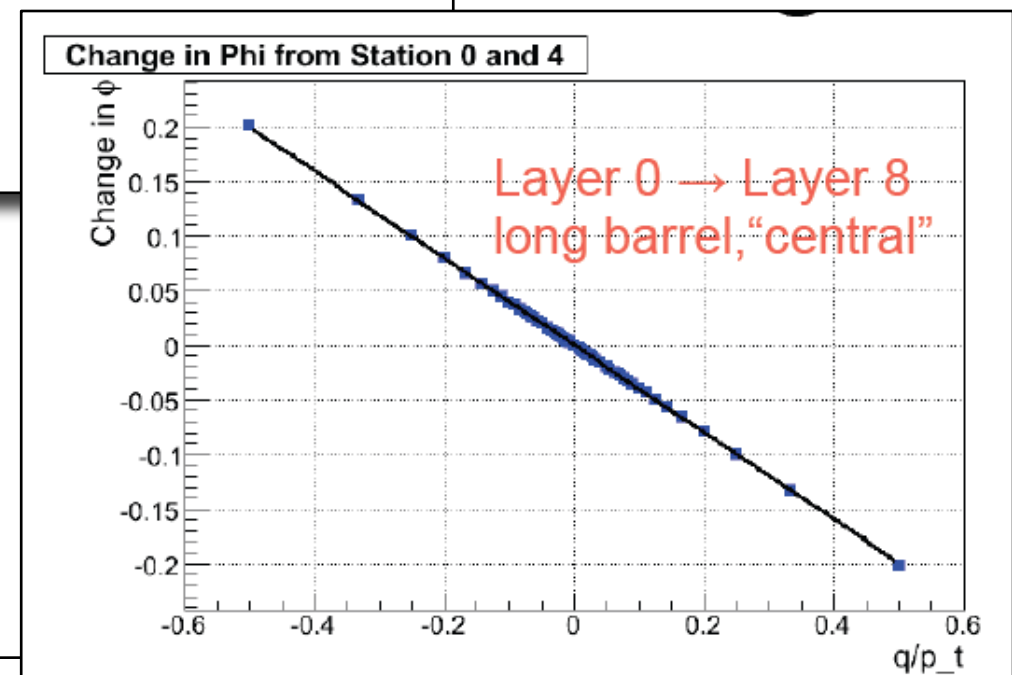
linear approximation:

$$\Delta\phi \sim 1/p_T$$

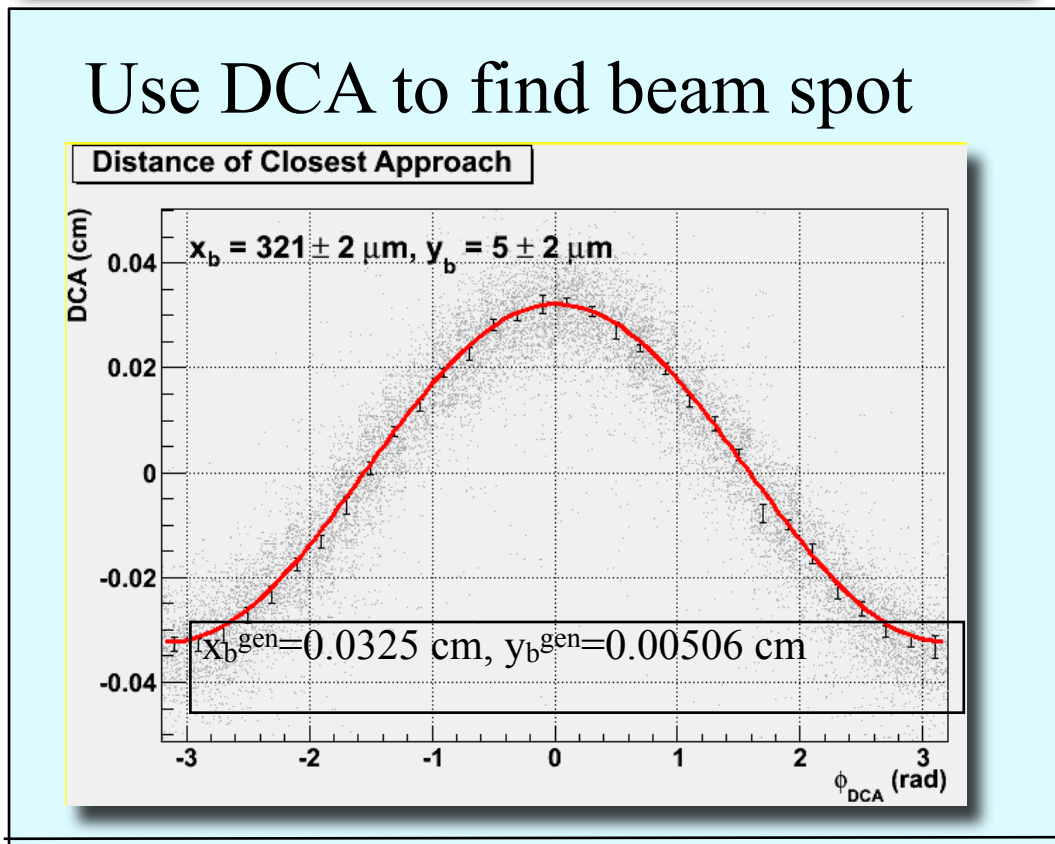
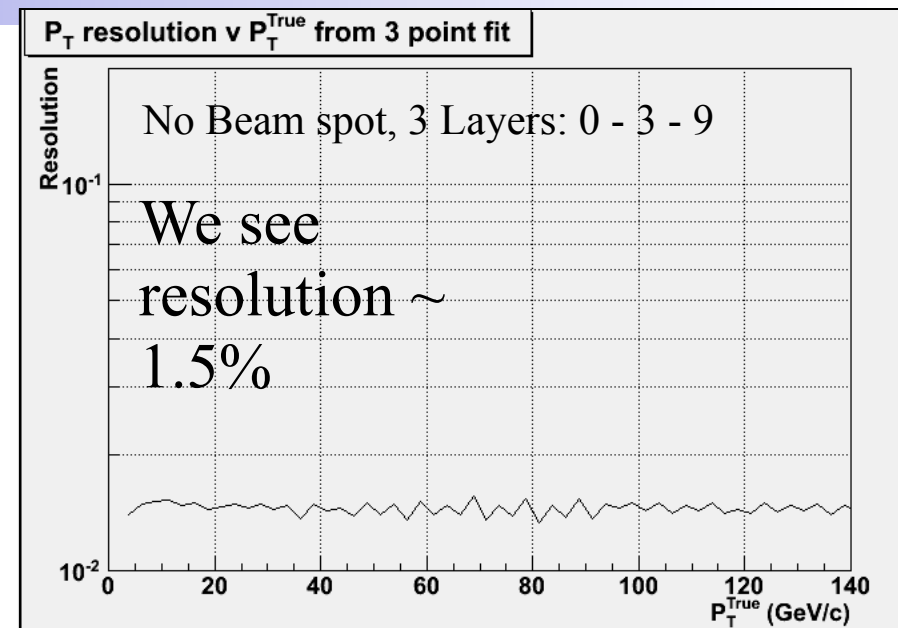
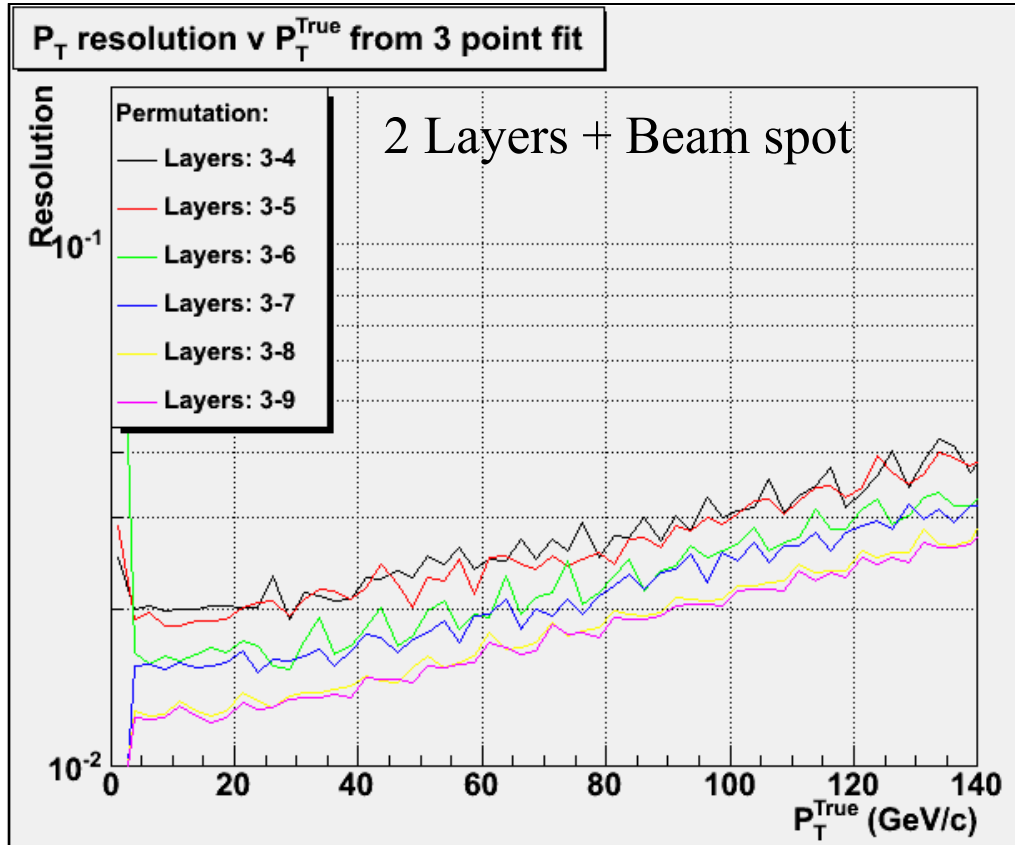
$$\Delta\phi \sim \Delta R$$

- sensors report local coordinate \rightarrow global ϕ
- measure ϕ in $100 \mu\text{m}$ units of arc length at 104 cm
- $\Delta\phi_{09} = \Delta\phi_{ij} \cdot \Delta R_{09} / \Delta R_{ij}$
- $\Delta\phi_{09} \rightarrow 1/p_T \rightarrow p_T$

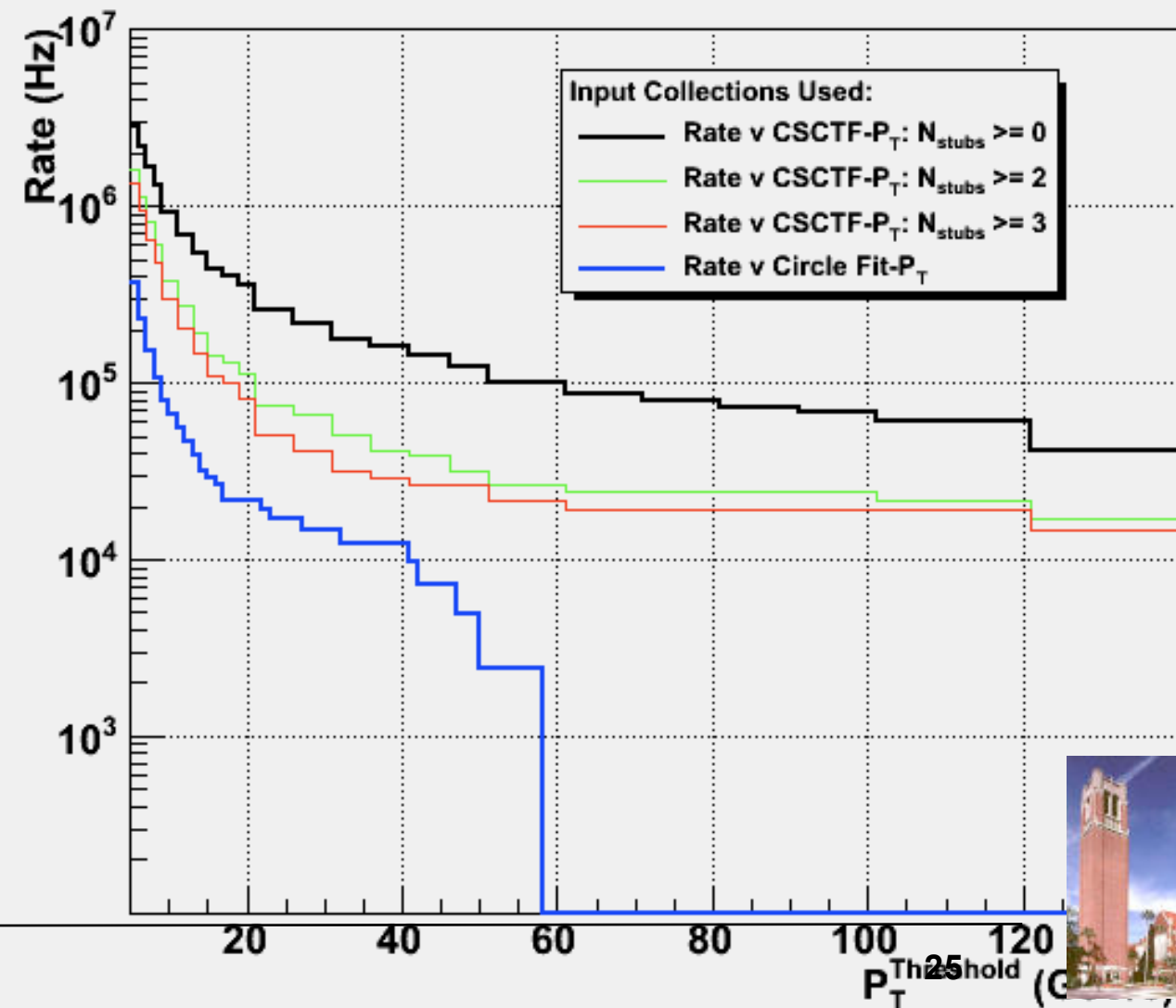
Approach demonstrated to achieve 2% P_T resolution



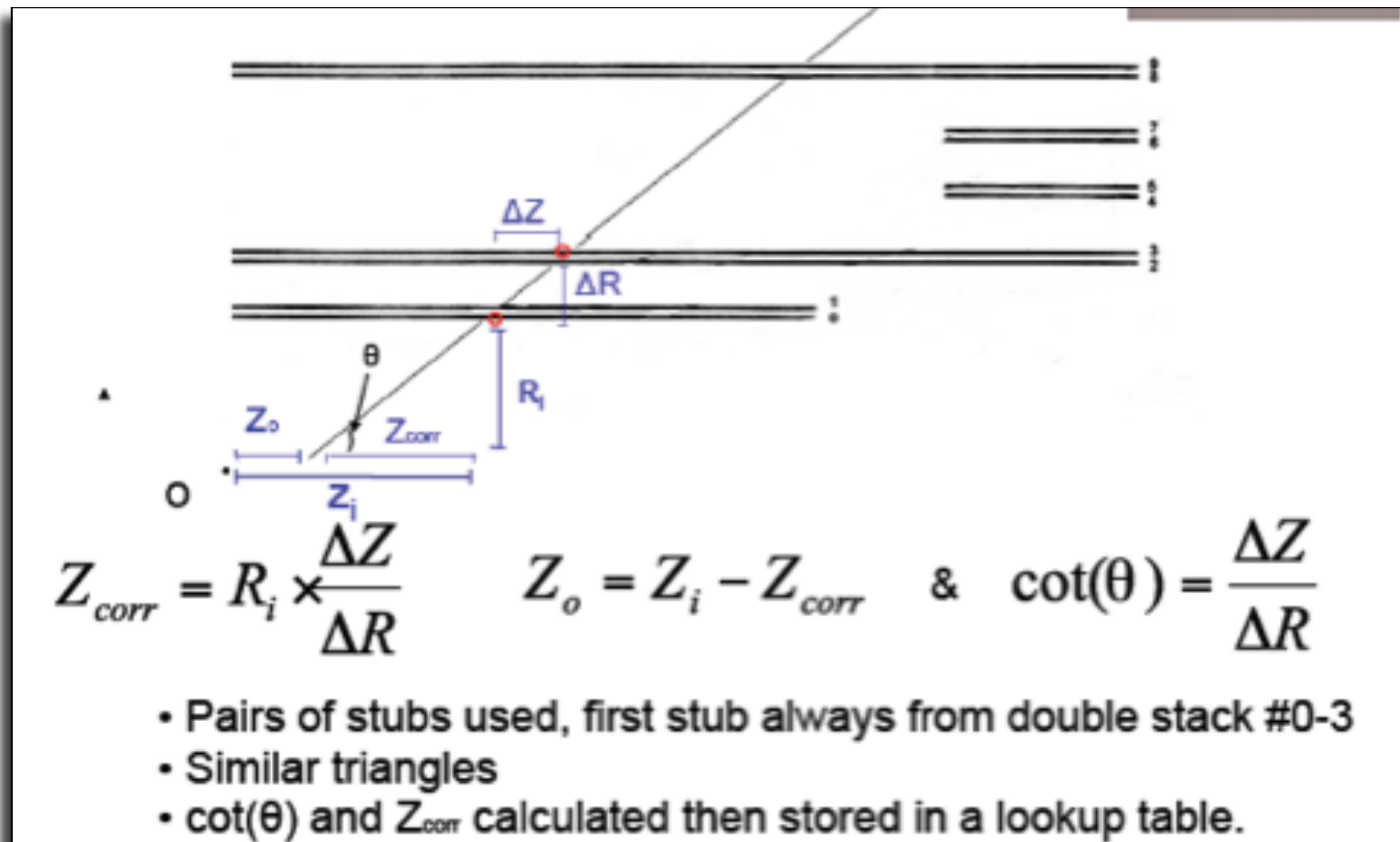
P_T Estimate 2: Circle-Fit Resolutions



Trigger Rate vs CSCTF- P_T : Quality > 1



cot(θ) & Z_0



CSTT model has been demonstrated to achieve z_0 resolution 640 μm and $\cot(\theta)$ resolution 0.002



Phase II Status:

- New manpower: B. Scurlock (UF)
- reviewed and integrated code used in summer studies, validated internal consistency
- results reported in July still stand, further developed
- new studies:
 - counting tracker stubs in matching window rejects background. **More tracker layers** in trigger lead to **more reliable** trigger **output**
 - **3 layers** of tracker in trigger allow for **beam spot independent pt measurement** and beam spot estimation on line (**track beam position in real time**)

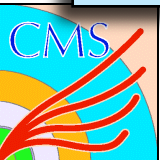
Conclusions:

- CSC electronics upgrades will increase internal data throughput for high luminosity running
- CSC TF Phase II studies with LB geometry converged.
- Recently full CVS permissions, committing code in the upcoming few days
- CSC TF Phase I challenge: increased multiplicity + better resolution, both at the same time

Supporting Material

Phase II: CSCTT Algorithm

- Define regions of interest to help pre-sparsify tracker readout
- Assume stub information is read out from tracker
- Define narrow roads in ϕ , z to further filter tracker readout
- Tracker stubs have excellent positional resolution – utilize internal correlations
- Attempt fit using tracker-only information (best measurement at low momenta)
- **Current CSCTT model developed in context of the Long barrel geometry**
- **CSCTT code is now in CVS**



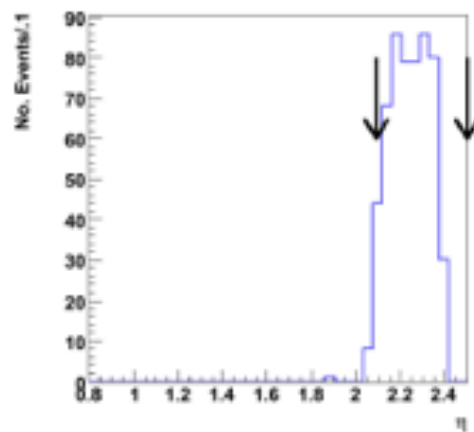
Expected Eta Coverage (Longbarrel)

Geometry Validation: Eta Coverage

Arrows show range of η covered by tracker stations

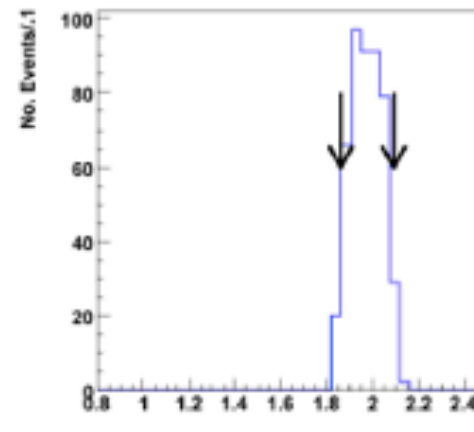
0-1

Etas for hit combination: 0-1
Expect: $\langle N_{stubs} \rangle \sim 4$



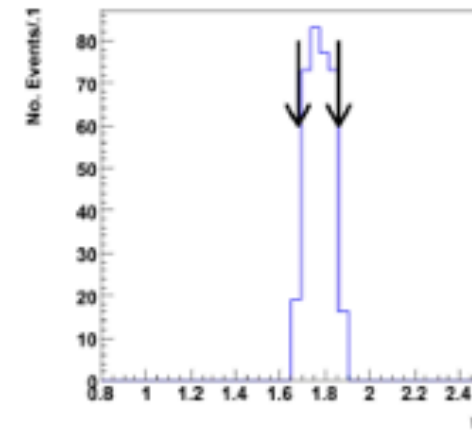
0-1-2

Etas for hit combination: 0-1-2
Expect: $\langle N_{stubs} \rangle \sim 6$



0-1-3

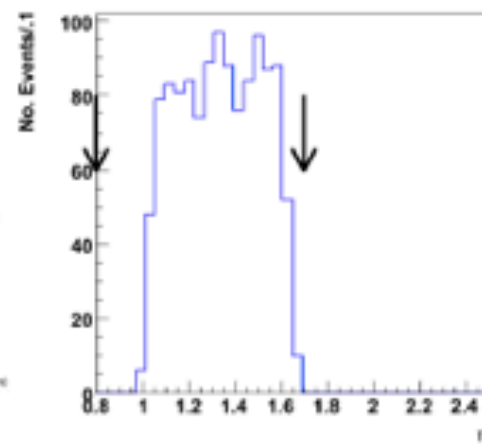
Etas for hit combination: 0-1-3
Expect: $\langle N_{stubs} \rangle \sim 6$



*These combinations of hits are very rare

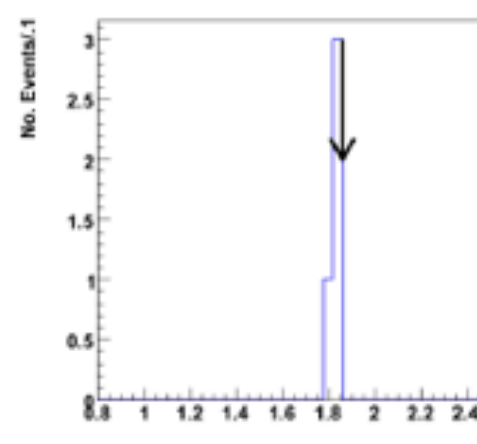
0-1-4

Etas for hit combination: 0-1-4
Expect: $\langle N_{stubs} \rangle \sim 6$



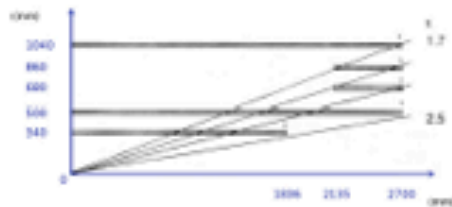
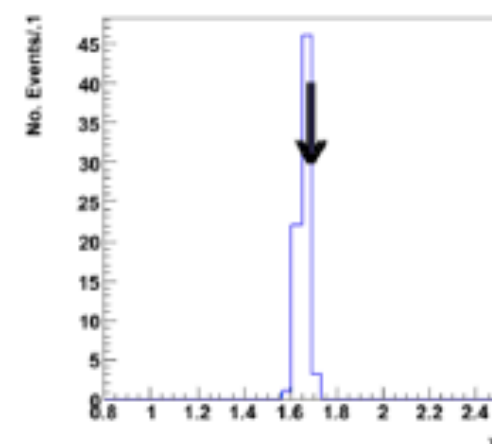
*0-1-2-3

Etas for hit combination: 0-1-2-3
Expect: $\langle N_{stubs} \rangle \sim 8$

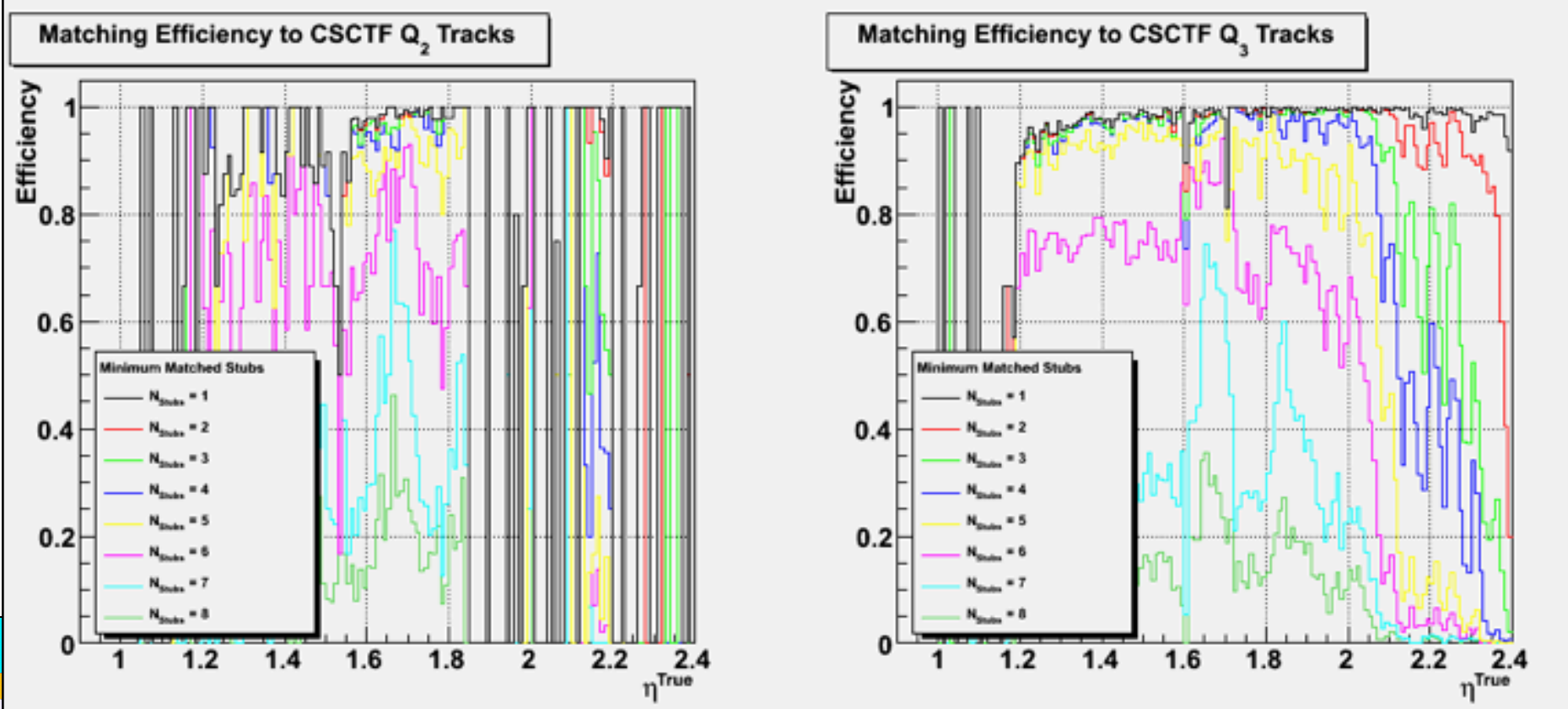
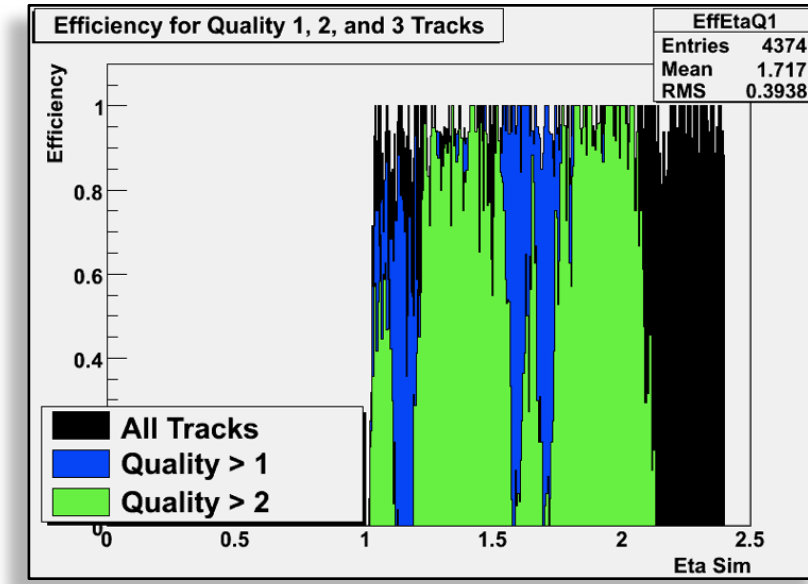
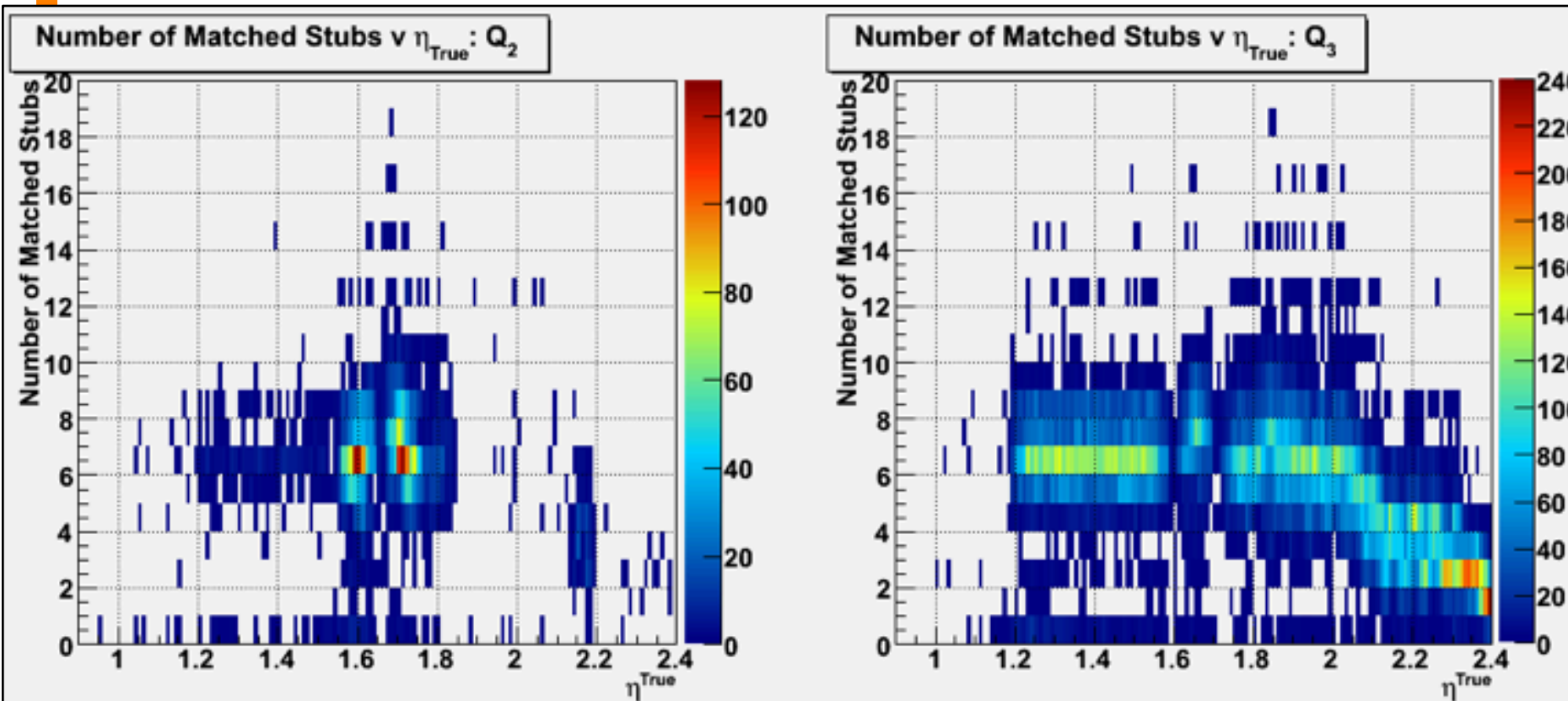


*0-1-3-4

Etas for hit combination: 0-1-3-4
Expect: $\langle N_{stubs} \rangle \sim 8$



Matching Windows Efficiency (room for fine-tuning)

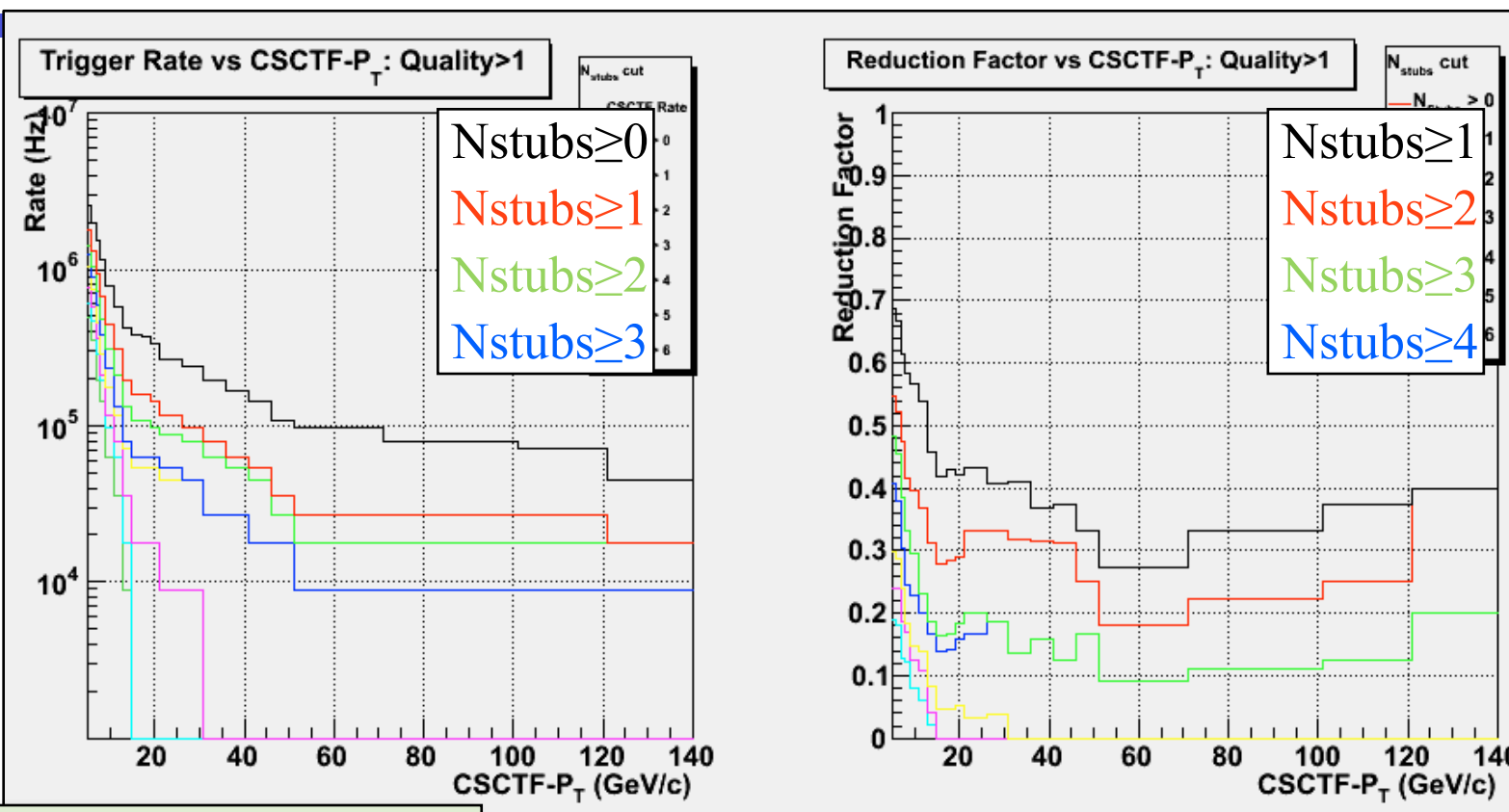


Here we see origin of inefficiency caused by Nstubs cut.

(1) $|\text{Eta}| > 2.1$ Nstubs is seen to drop to ~ 2 (expect 4)

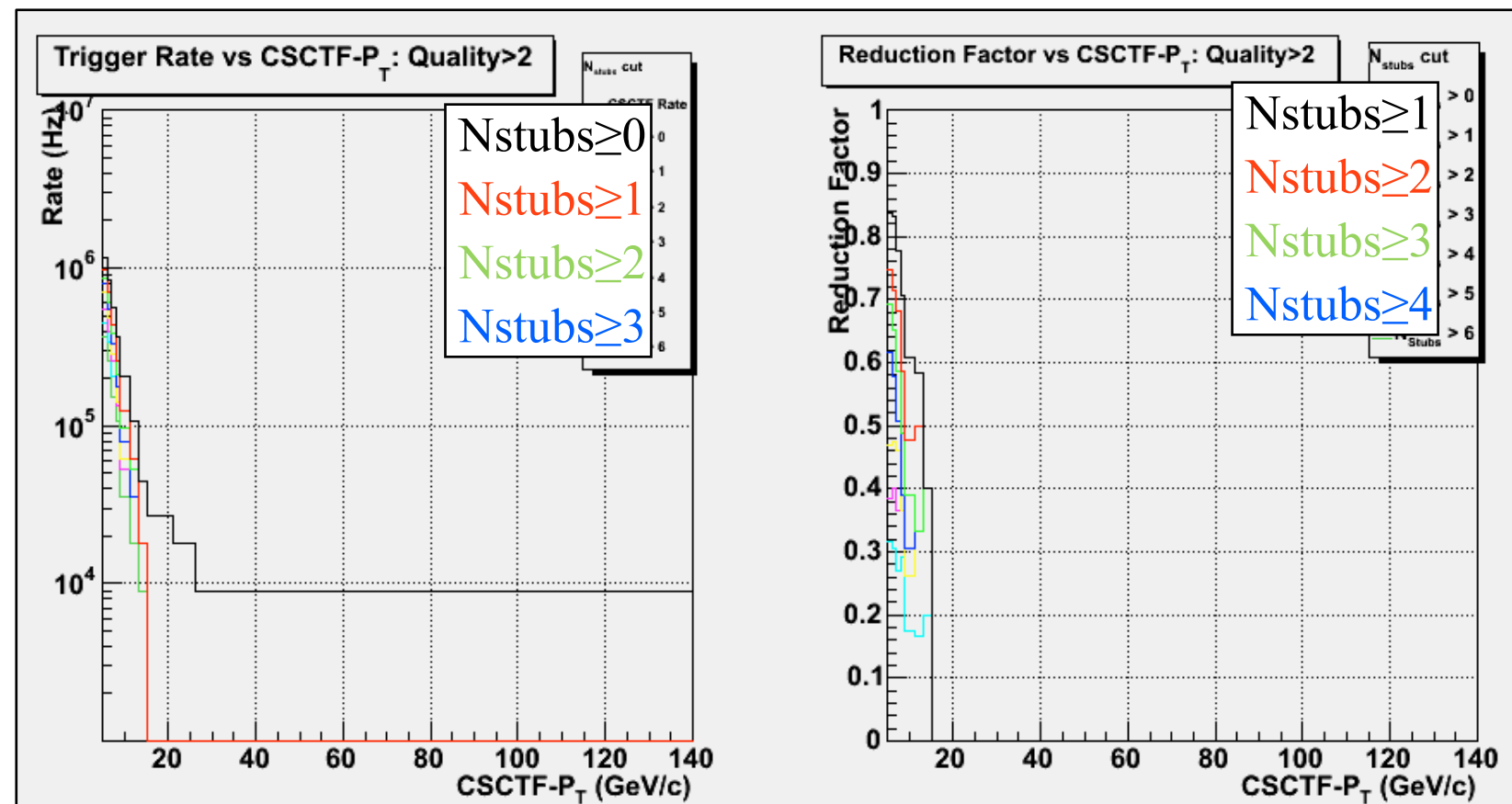
(2) Eta dependent switch in CSCTF-track quality assignment due to gap between inner and outer rings of ME2 and ME3 (matching windows are tuned for Q3 tracks).
 $Q_3:Q_2 \sim 8:1$ for 1 mu events (cf $Q_3:Q_2 \sim 2:1$ for MinBias)

Rate Reduction from stubs



Rate and relative reduction contours with Quality>1 CSCTF Tracks (versus Nstubs matching window cuts)

Rate with Quality>2 CSCTF Tracks



Rate reduction power is mostly related to CSCTF Quality. Improperly seeded windows miss underlying stubs. This can be a powerful weapon against CSCTF mis-measurement!



P_T with Beam spot drift

- Current algorithm takes filtered stub candidates and assigns P_T by finding effective $\Delta\phi_{09}$ between tracker Layers
 - Uses linear fit between $1/P_T$ and $\Delta\phi_{09}$, with (0,0,0) beamspot
 - This algorithm can be re-tuned to accommodate off-center (not investigated yet)
- Can we use the CSCTT model framework to accommodate beam spot drift?
 - Take filtered stub candidates and use a 3-point circle fit to find P_T
 - Algorithm 1: Assume a known beam spot and use stubs available from two tracker Layers
 - Algorithm 2: Assume unknown beam spot and use stubs available from three tracker Layers
 - Can then use DCA to provide beam spot location
 - Both algorithms fit two lines: $L1 = \text{Point}_i$ to Point_{i+1} and $L2 = \text{Point}_{i+1}$ to Point_{i+2} (points increasing in radius). Solve for the intersection of the two orthogonal lines which bisect $L1$ and $L2$
 - Working with engineer to understand how we can implement algorithm in HW