Track Trigger Designs for Phase II

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geometry

assume long barrel design for tracker



BUT:

many ideas also apply to geometries with less layers and to different low pT hit rejection schemes (e.g. cluster width)

doublet formation

- reject hits from low p_T tracks on detector
- cluster adjacent pixels with hits
 - reject clusters >2 pixels wide
- require coincidences between clusters in two closely spaced modules in a stack
 - reject single clusters
 - reject doublets from soft tracks



 $r-\phi$ view of rod structure

rates

MC simulation (Laura Fields, Cornell U, track trigger session tomorrow)

- Cluster rate
 - max 2 pixels wide

R = 35 cm	R = 55 cm	R = 110 cm	@ z=0
≈4	≈1.6	≈0.2	MHz/cm ²
≈10	≈4	≈0.5	/xing/module



Odoublet rate

- 1 mm stack separation
- 2 GeV threshold

R = 35 cm	R = 55 cm	R = 110 cm	@ z=0
≈0.3	≈0.13	≈0.025	MHz/cm ²
≈0.7	≈0.3	≈0.06	/xing/module



number of fibers

- average rate over length of rod $\approx^1/_2$ max rate @ z=0
- safety factor of ≈ 10
- →1.5 MHz/cm² in inner layer
- 42 modules in z
- 20 bits/doublet
- \rightarrow 250 Gb/s per sector per station (2 stacks)
- bandwidth of fiber links = 3.6 Gb/s
- \rightarrow 70 GBT per sector per station
- \rightarrow ≈5000 GBT for entire tracker

basic idea

represent every possible hit combination by a logic "equation":

 $S_{1i} \cap S_{1o} \cap S_{2i} \cap S_{2o} \cap S_{3i} \cap S_{3o}$

- create a table of all possible equations in FPGAs
- feed all hits for an event into the FPGAs
- evaluate all equations simultaneously.
- the equations which are satisfied correspond to the reconstructed tracks
- timing dominated by time needed to load hits into FPGAs
- problem
 - too many equations
 - too many inputs
 - need to factor problem

sector structure

- trigger logic handles inputs from sectors n-1, n, n+1
- active area of module \approx 95 mm (ϕ) x 100 mm (z)
- sector size determines min p_T for full acceptance



minimum p_T

what is the minimum p_T we need to trigger on?

min p _T	sector opening angle	
2 GeV	18º	requires more/wider modules
2.5 GeV	15º	←lots of inputs but geometry easier
5 GeV	7.5°	←less inputs – makes trigger easier

built into the hardware design
need to decide soon

→ here assume 15° sectors

tracklet formation

- combine doublets from the two stacks in each station to form tracklets
 - \bigcirc drop in rate by about factor 4 (but need \approx 40 bits/tracklet)
 - for each stack in inner layer need to process data from two adjacent stacks in z in outer layer



equation count

- assume azimuthal position resolution ≈ 0.1 mm
- number of ϕ positions per sector:
 - \bigcirc \approx 2900 in outer station
 - $\odot \approx$ 1450 in middle station (for each outer station position)
- number of equations
 - $\bigcirc \approx 2900 * 1450 = 4,200,000$
 - \odot too many equations for single chip ightarrow
- number of fibers
 - O 210 fibers from each sector
 - too many inputs for single chip n-1
- divide outer station into 12 sub-sectors
 - route tracklets from inner and middle stations to subsectors using interaction point and p_T

n+1

sector processor

sector processor

outer station

- Ono pT information required for sorting
- Ono need to form tracklets in outer station
- Orobust against inefficient sensors
- Onumber of equations in each sector
 - ≈ 4,200,000/12 ≈ 350,000
- middle and inner stations
 - Oloose entire station if there is an inefficient sensor

solution

 in parallel sort into 12 subsectors anchored in middle layer and into 12 subsectors anchored in inner layer

orobust against inefficient sensors in any layer

sector processor

for each trigger specify number of tracklets and doublets

Oaccept tracks with

3 tracklets

2 tracklets and 0 or 1 doublets

I tracklet and 0 or 1 doublets

do r-\u00f6 tracks satisfy track equations in z?
 remove duplicate tracks

summary

- 3 trigger stations provide full coverage for tracks with $p_T>2.5$ GeV in 15° sectors
- hits collected in real time, sent off-detector on ≈5000 optical fibers at 3 Gb/s
- all possible track equations for each sector evaluated in parallel using FPGAs in USC to produce inputs for L1
- total of ~2000 large FPGAs needed to build this using current technology

next steps

- © robust against hardware failures
- © very powerful pattern recognition
- ⊗ large channel count, power, mass
- need MC simulations implementing specific algorithms
- verify rate estimates with LHC data
- → do we really need 6 trigger layers?
- What is the smallest number of trigger layers needed?