SLHC Regional Calorimeter Trigger System Design and Prototypes

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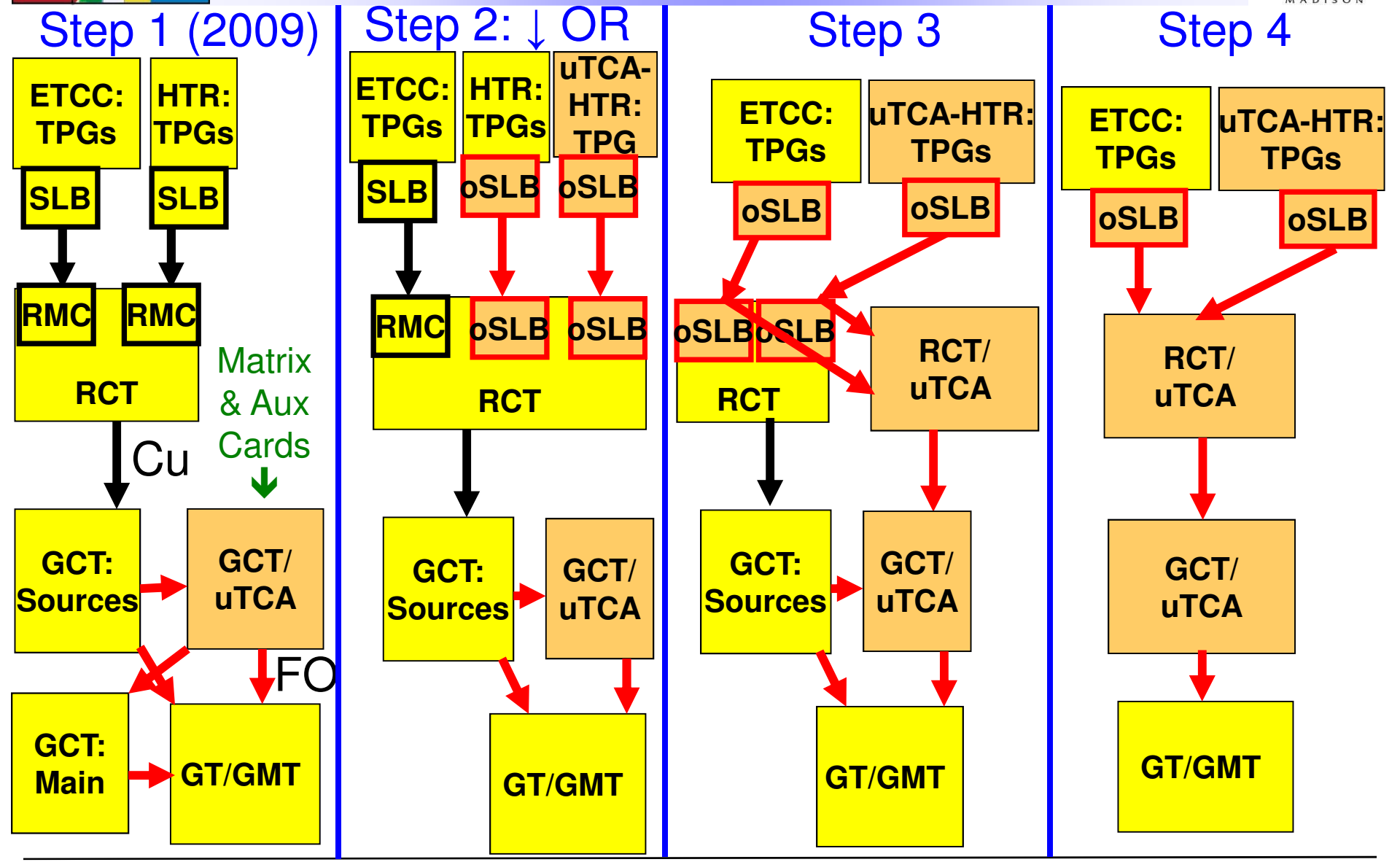
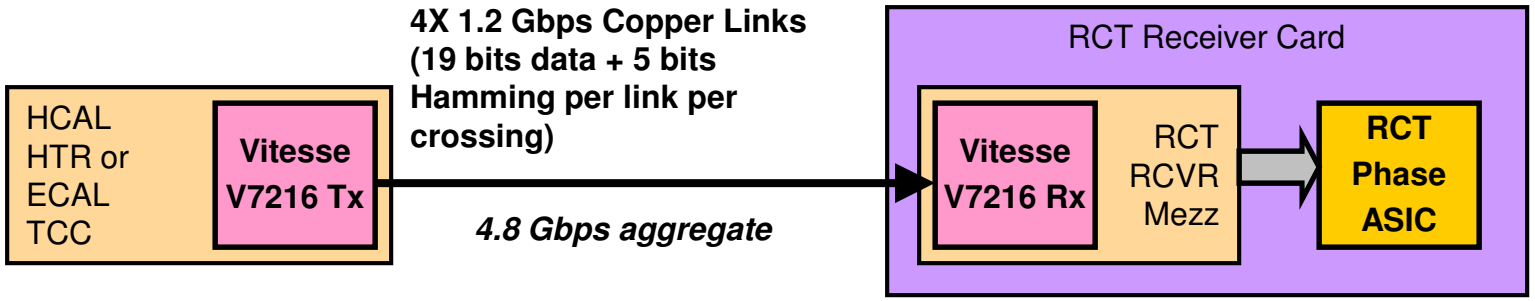
Calorimeter Trigger Evolution

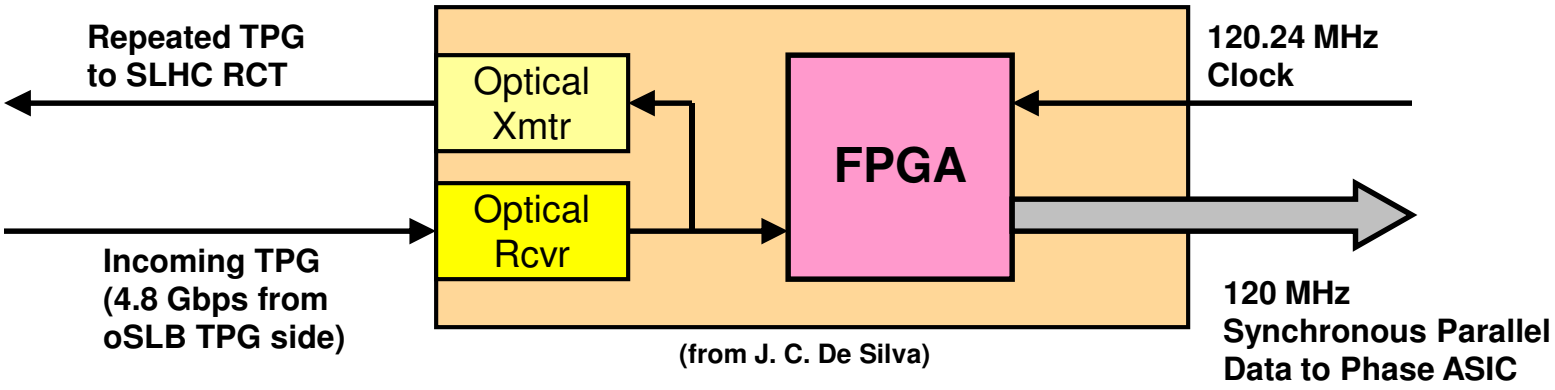


Review: Current HCAL/ECAL to RCT Link



- Intersection of 4,032 links at common destination (RCT)
- Link Xmt & Rcv Clks are 3X the LHC Clock (~120 MHz)—use of common clock means no long term drift issues and minimal buffering between subsystems
- Elastic buffers in V7216 Rx chips to manage short term clk jitter
- RCT Phase ASIC provides channel bonding function, hamming code check, and buffering for 4X RCT processing pipeline (~160 MHz) in about 3 crossings
- 120 MHz Link Clock skew tolerances: ±6ns @ Tx, ±1ns @ Rx
- Scheme is stable, reliable, and has low latency

oSLB RCT side (LIP Development)

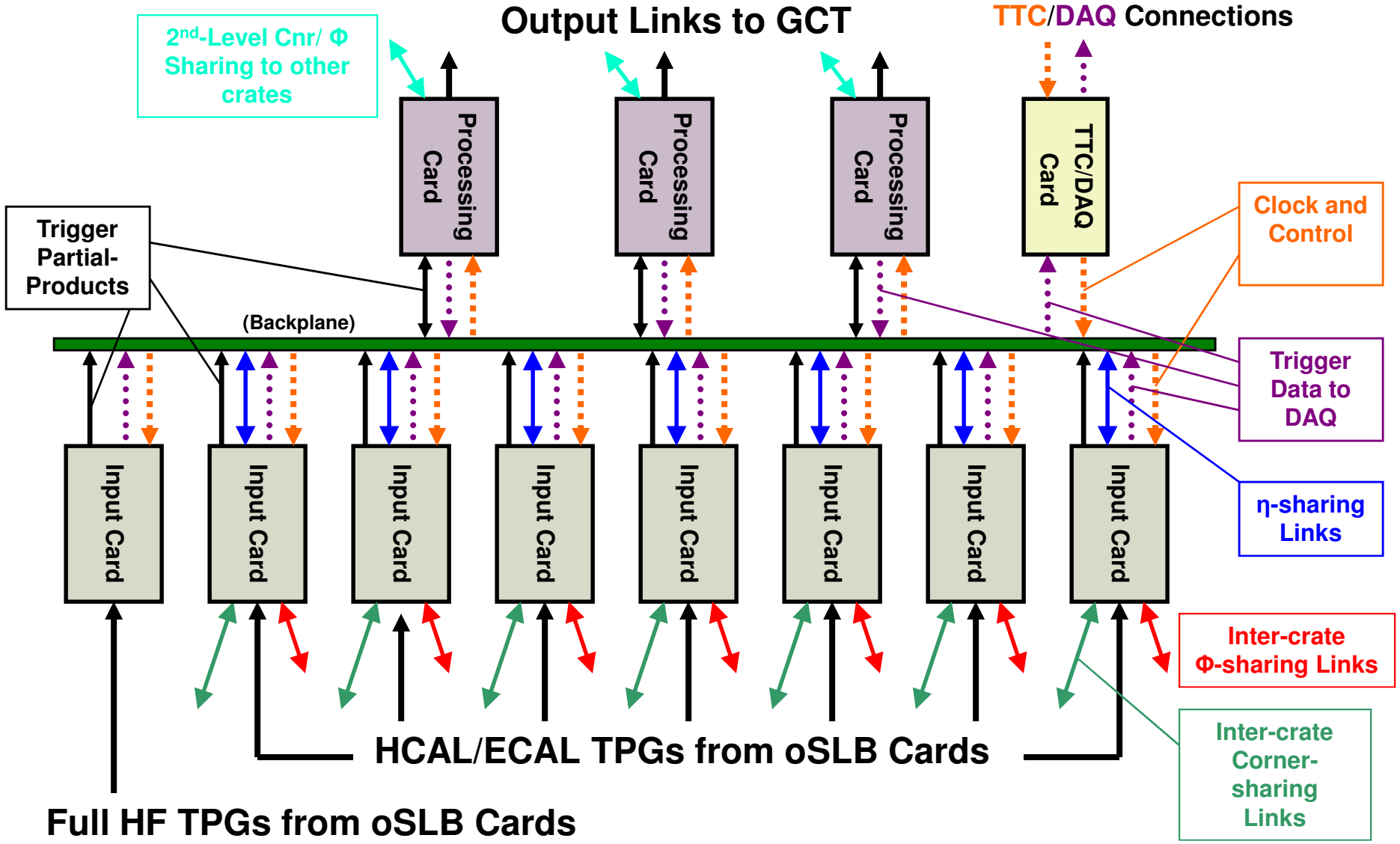


Latency for Current 7216-based Link:

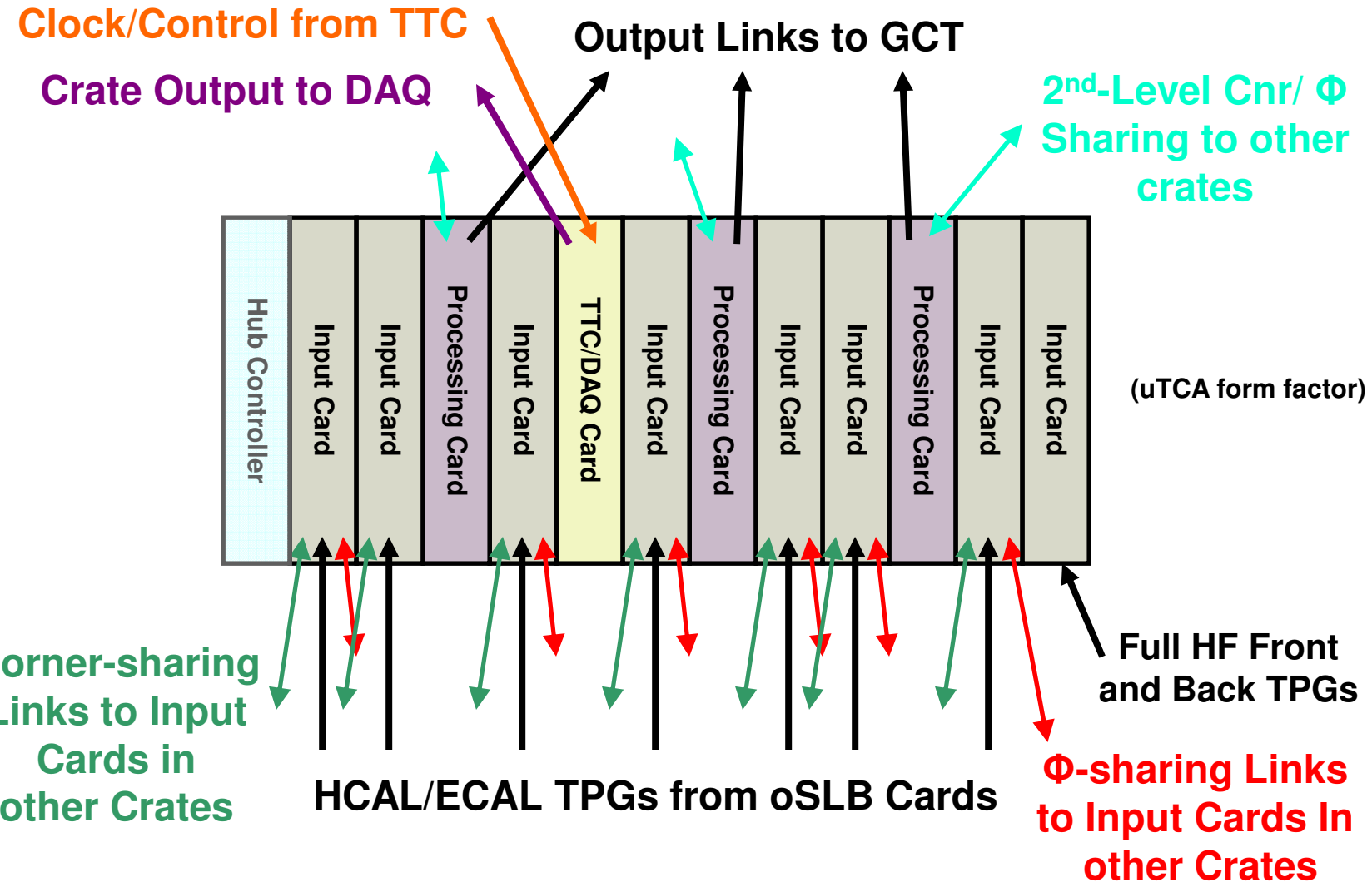
- 3.4 bunch crossings for cable (85ns)
- 0.8 bunch crossings for 7216 Tx (19ns)
- 2.5 bunch crossings for 7216 Rx (62ns)
- TOTAL: 6.6 bunch crossings (166ns)

- Based on what we know so far about Rocket I/O, the budget may need to be increased by 1 or 2 crossings

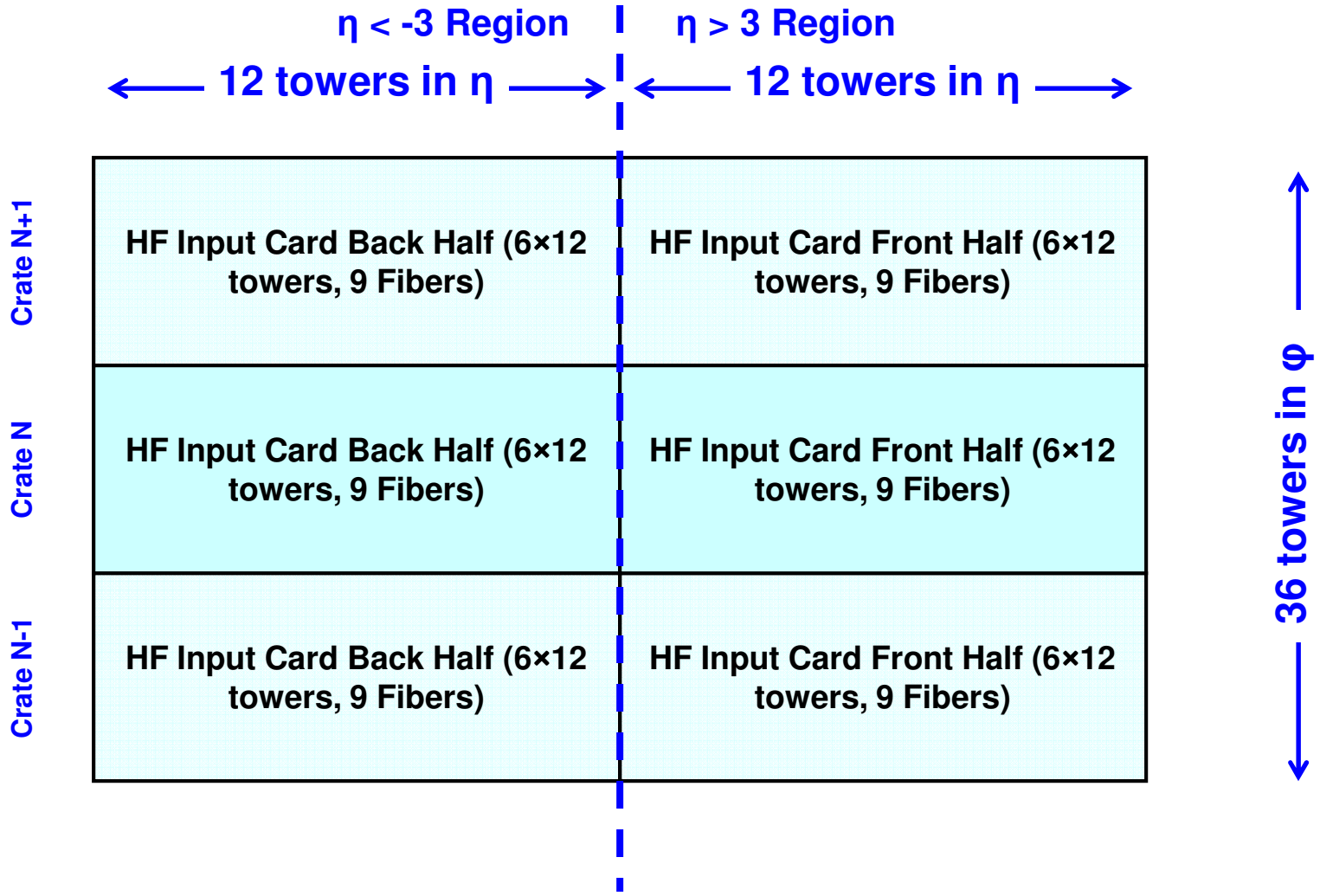
SLHC RCT Block Diagram
(56η×12φ B/E slice + 24η×12φ Full HF Slice)



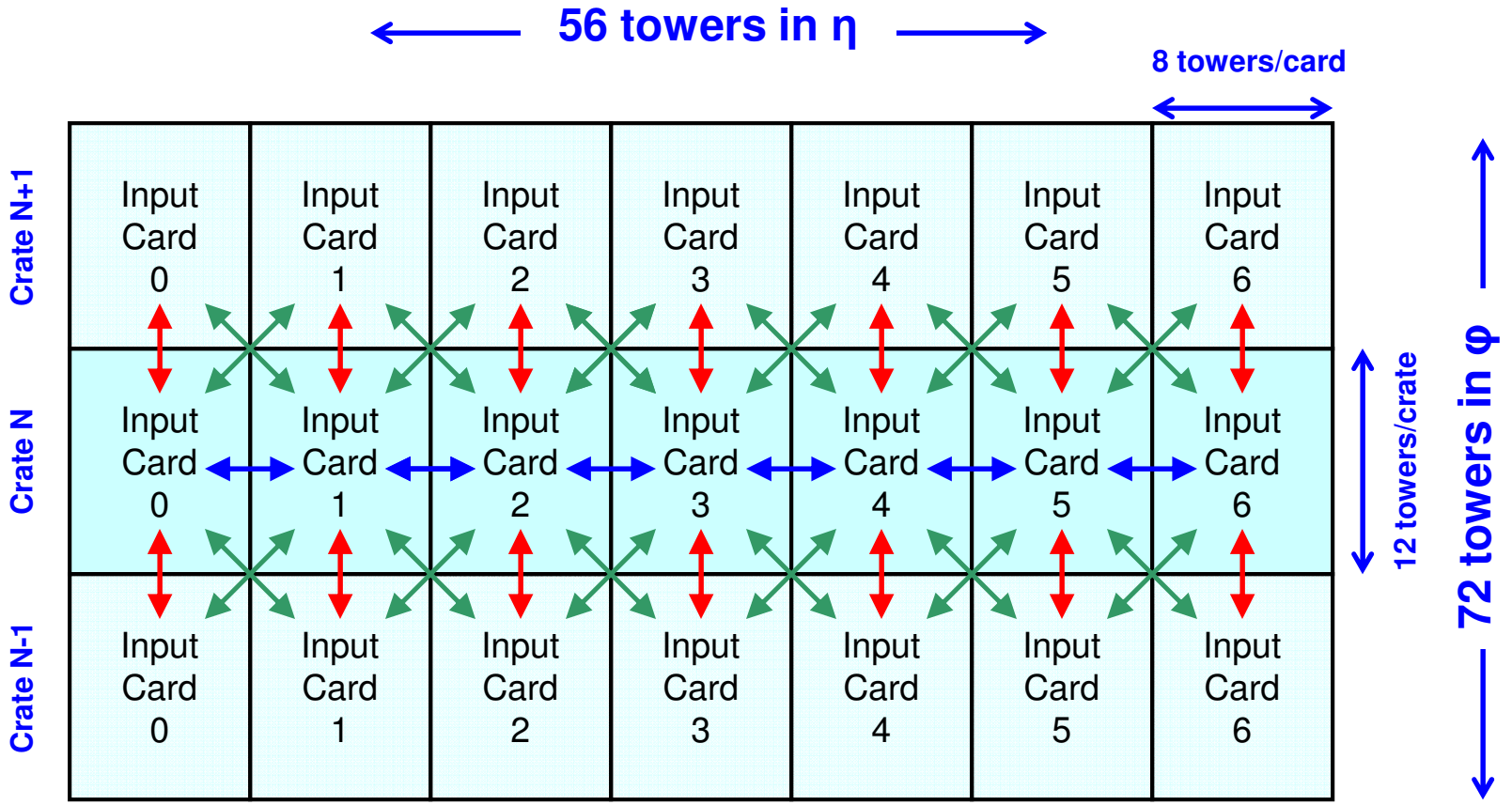
SLHC RCT Crate—1 of 6 (Barrel+Endcap+Full HF)



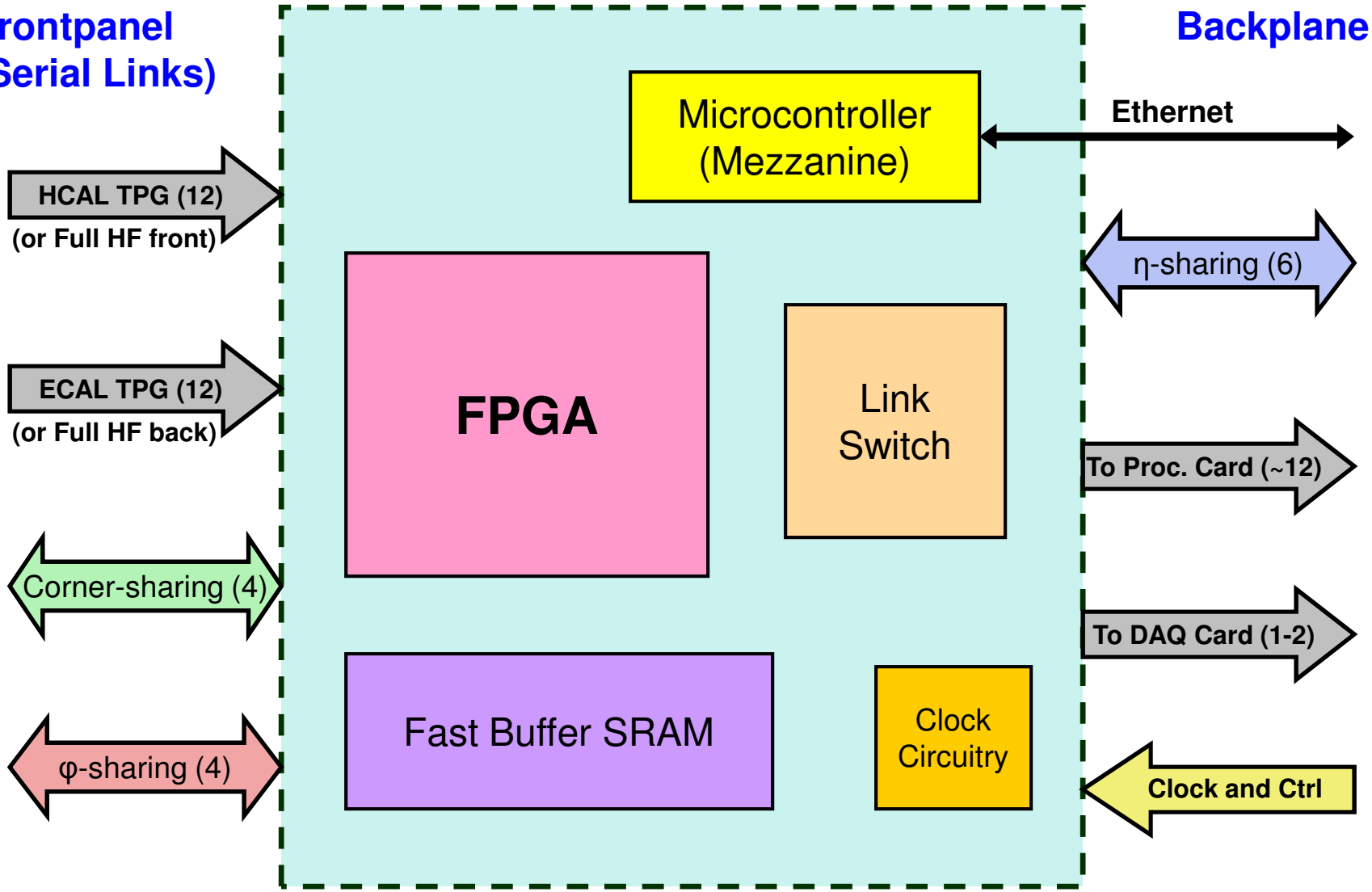
Full HF Input Card Coverage



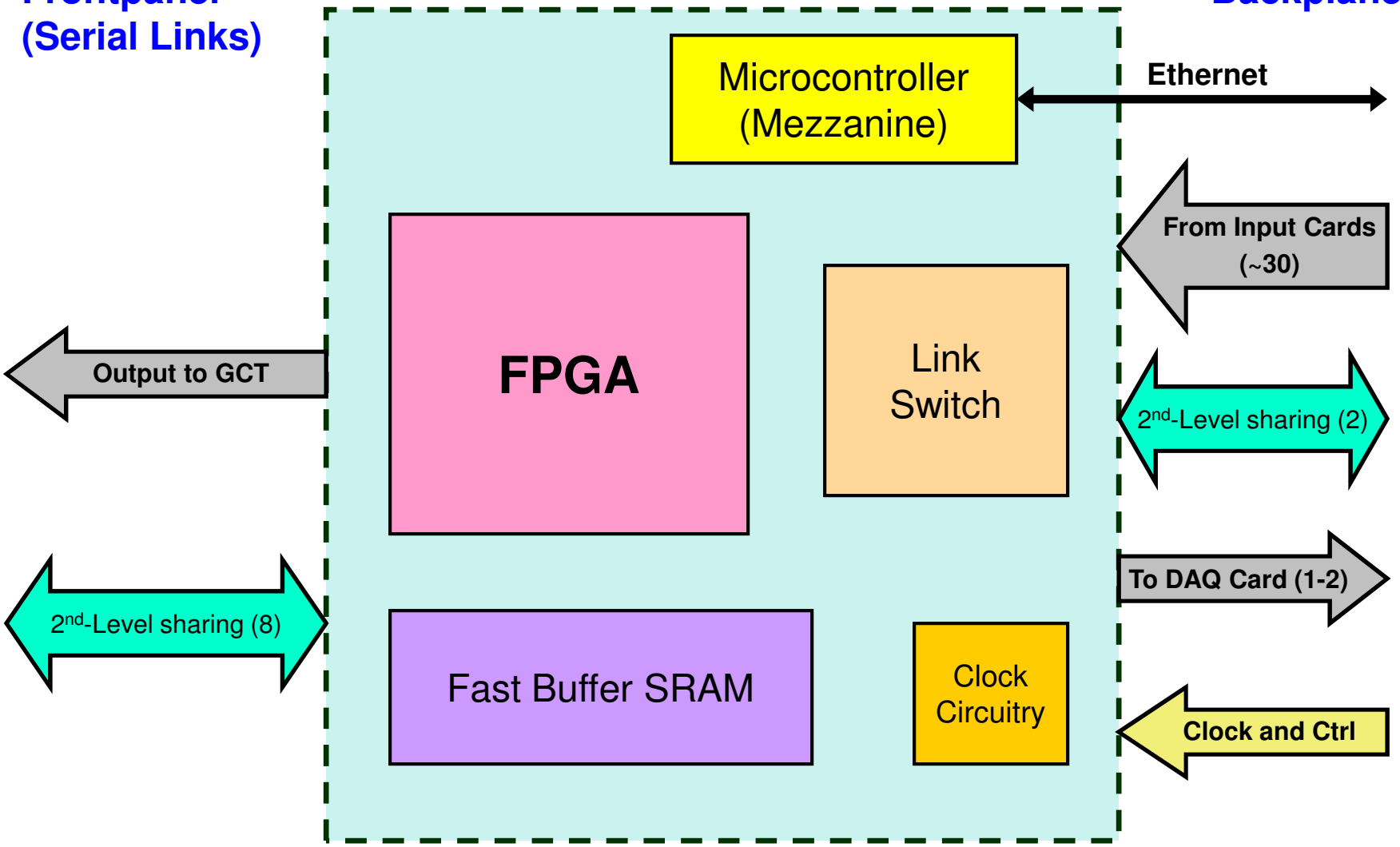
Input Card Barrel/Endcap Coverage/Sharing



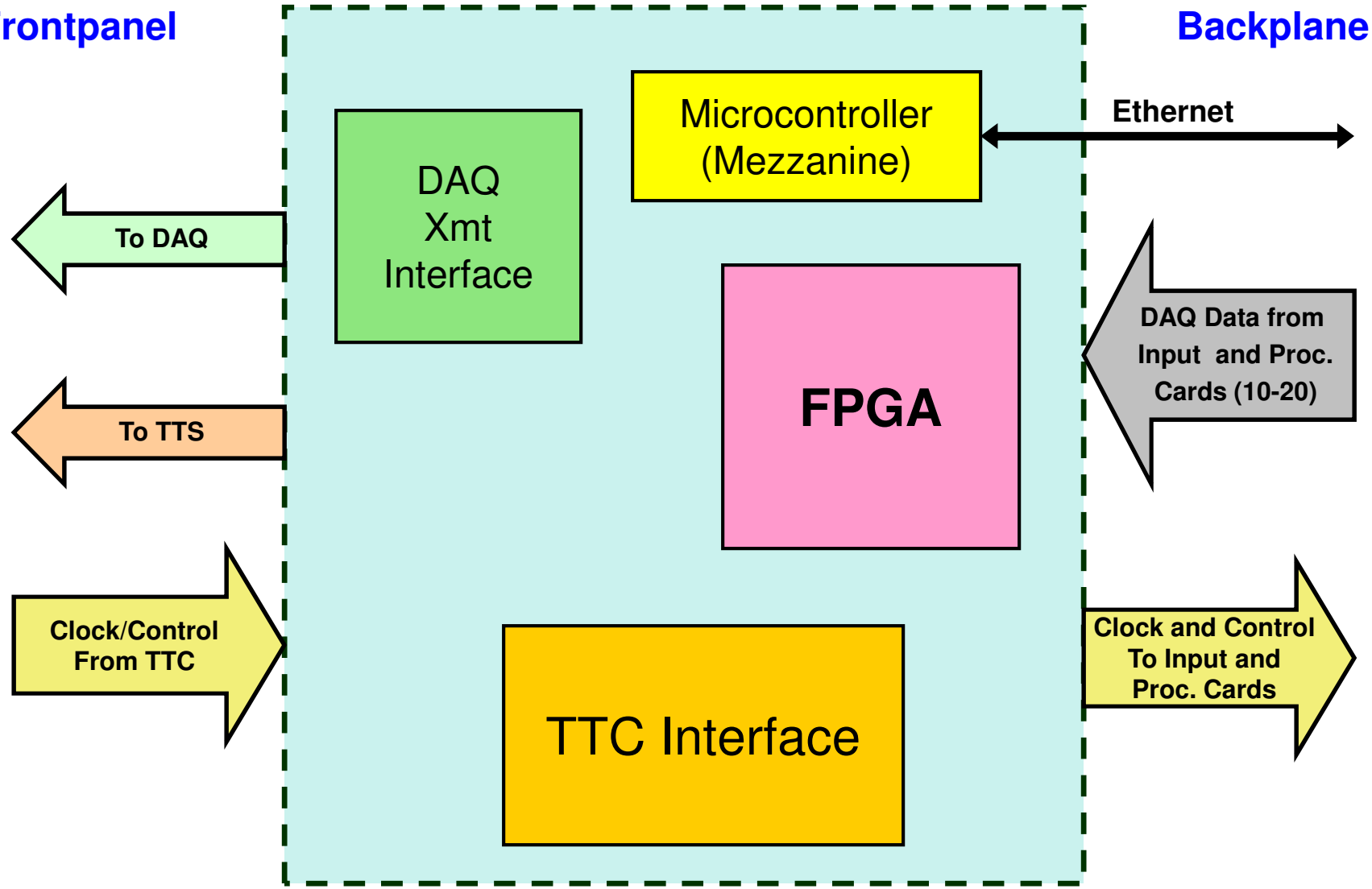
SLHC RCT Input Card (12η × 8φ)



SLHC RCT Processing Card
(~20η × 12φ)



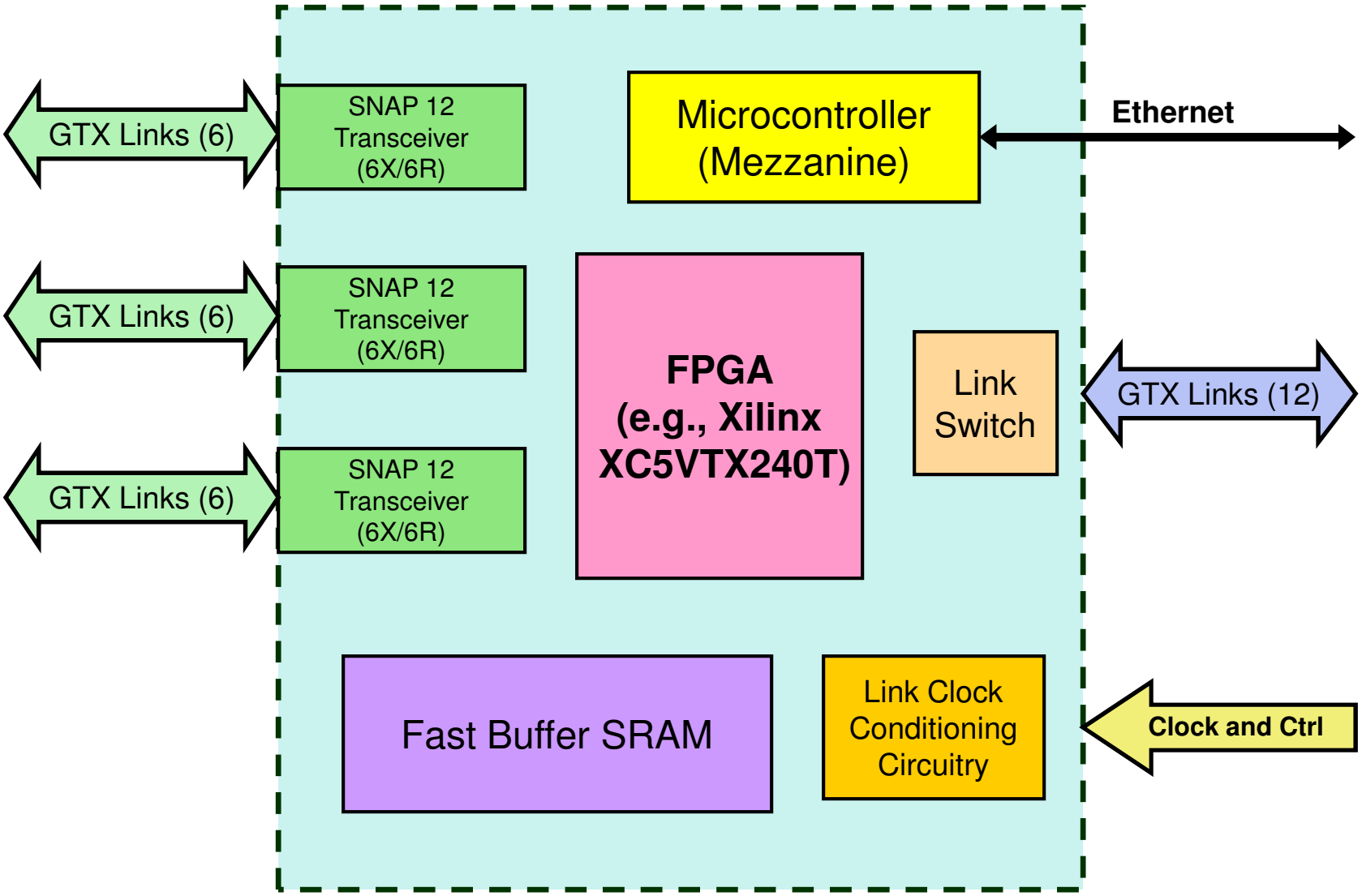
SLHC RCT "TTC"/DAQ Card
(Evolution of UW GCT Aux Card)



SLHC RCT Key Points:

- Double-width AMC-style (uTCA) modules (148.8mm height, 181.5mm deep)
- 3 Card Types: Input Card, Processing Card, TTC/DAQ Card (evolution of UW GCT aux card, possibly common card)
  - Input Card receives HCAL/ECAL/HF TPGs, performs inter-region data sharing needed by algorithms (8 cards/crate)
  - Processing card receives partial products from Input Cards, performs 2nd level of sharing to complete regional processing, delivers output to GCT (~3 cards/crate)
  - TTC/DAQ card interfaces crate to the TTC and DAQ systems (1/crate)
- Single Crate Encompasses Full η Width, including full HF granularity
- Card microcontroller implemented as a Mezzanine
  - Can perform uTCA arbitration if needed
  - High-performance I/O interface to card for Trigger Supervision functions
  - Single hardware/firmware implementation
- Backplane contains combination of passive and switched interconnections
  - Passive good choice for η-sharing
  - Switches for some routing between Input and Processing cards
- TPG Inputs are fundamentally compatible with the envisioned upgrade path
  - Affects link and pipeline clock frequency choices
- Goal is to have a single firmware image for each card type, and to configure individual cards via RAM

SLHC Cal. Trig Prototype (R&D Platform for Conceptual Design)



SLHC Cal. Trig Prototype

- **R&D Hardware Platform**
  - **Prove layout/PCB fabrication concepts and principal technologies for Input and Processing cards**
  - **Circuit Prototypes:**
    - Microcontroller Mezzanine Concept
    - Link/Pipeline Clock Conditioning
    - External SRAM/FPGA Interface
- **Double-size AMC module (149mm x 182mm)**
- **Suitable for trigger algorithm development**
- **Capable of supporting hardware/firmware/system R&D for multiple years**