CMS Upgrade Workshop – Fermilab, 28th of October, 2009

DC-DC Conversion for the Pixel System at Phase I

Lutz Feld, Rüdiger Jussen, Waclaw Karpinski,
Katja Klein, Jennifer Merz, Jan Sammet

I. Physikalisches Institut B – RWTH Aachen University

Federal Ministry of Education and Research

SLHC-PP
PREPARATORY PHASE 2008 • 2011
LARGE HADRON COLLIDER UPGRADE

RWTH AACHEN UNIVERSITY

Outline

- Plans for Phase I pixel upgrade
- DC-DC Powering Scheme for the CMS Tracker

- Challenges
- Timeline
- Test System

- Choise of Converter ASICs
- Aachen Buck Converters with CERN-ASICs

- Efficiency Measurements
- Converter Noise Measurements (EMC)
- Infrared Camera Setup

- Implementation into the CMS pixel detector

- Summary

Phase I – Activities and Plans

Pixels at Phase I: $2 \cdot 10^{34}$ $cm^{-2}s^{-1}$ | ~2014

- Detector will grow: 3 $\rightarrow$ **4 barrel layers**, 2 x 2 $\rightarrow$ **2 x 3 forward disks**

- More read-out chips per cable and PS, **total power consumption will increase**
  $\rightarrow$ Current in the cables to the Tracker will increase

- The upgraded pixel detector for Phase I cannot be powered with (modified) existing power supplies $\Rightarrow$ Massive upgrade of PS would be needed

- DC-DC conversion scheme would allow to power the upgraded pixel detector with existing power supplies and cables

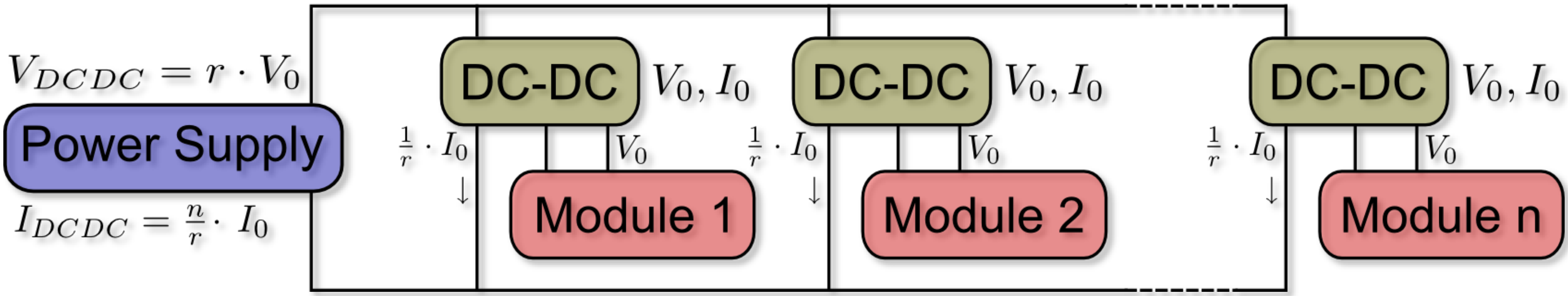
- Buck converters with conversion ratio r = 2 could be combined with light PS upgrade
  $\rightarrow$ First use case of DC-DC converters in the tracker

We will develop / test converters, based on ASICs of CERN group!

DC-DC Powering Scheme for CMS at SLHC

→ A new powering scheme is mandatory: **DC-DC conversion:**

Conversion ratio
r = V_{IN} / V_{OUT} (r>1)



Example for the Tracker:

Cable losses: (r = **2**, Efficiency η = **80%**)

→ without converter: P_{Cable} = 30.0 kW

→ with converter: P_{Cable} = 9.4 kW

- n modules are powered in parallel
- DC-DC Buck Converters:
  - Convert higher input voltage to a lower output voltage
    "Step-down Converter" $U_{in} > U_{out} \rightarrow I_{in} < I_{out}$
  - Losses without DC-DC: $\mathbf{P_{cab} = R \cdot I^2}$
  - Losses with DC-DC Conversion: $\mathbf{P_{cab,DCDC} = R \cdot (n \cdot I_0)^2 \cdot (1/r)^2 = R \cdot I^2 \cdot (1/r)^2}$

Challenges

- **High-voltage tolerant (up to 12V) and radiation-hard ASICs needed:**
  - Up to ~2-3 · 10^{14} n/cm^2 (1MeV neutron equivalent) and ~150kGy
    → **CERN** AMIS2: **Prototype** for radiation hard Converter [F. Faccio, S. Michelis, ...]
- **Efficiency:**
  - $$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out} \cdot I_{out}}{V_{in} \cdot I_{in}}$$ (r ≈ 2 , I < 2.8A)
- **Inductors:**
  - CMS Tracker: B=3.8T
    → Converters have to be magnetic field resistant
  - Ferrite material saturates in a strong magnetic field
    → Use of air-core coils inevitable
- **Converter switching noise (f_{SWITCH} ~ MHz):**
  - Additional source of noise in the system
  - Has to be compatible with PSI46 ROC
- **Material budget:**
  - Material budget of the new CMS pixel detector should decrease, even with converters
- **Space constraints:**
  - Length = 3.2cm ; width = 2cm; height < 1.4cm
- **Specific requirements:**
  - Very fast load variations due to the orbit gaps. Long pixel cables and the CAEN A4603 modules
  - Quantity → 944 pieces required for FPIX + BPIX; 1400 including spares and prototypes

→ Efficiency Measurements

→ Magnetic Field Tests

→ Spectrum Analysis (Converter Noise)
→ System Test Measurements (with pixel detector hardware)
→ Susceptibility Measurements

→ η ≈ 4 ↔ uncritical

→ Piggy-boards with board-to-board connectors

→ Stability Test System w/ switched load

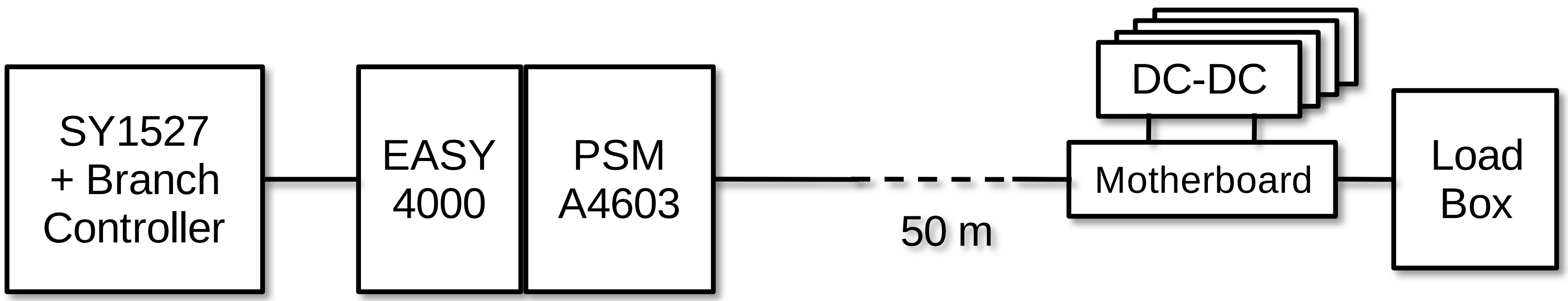
Timeline

1^{st} qrt. 2010	• Development and System Test of a (non rad-hard) converter • Start with commercial converters to commission setup • In time for the Phase I upgrade TDR
1^{st} qrt. 2011	• Development and test of the final rad-hard converter (CERN Group has agreed to develop required ASIC)
1^{st} qrt. 2012	• Pre-production of 100-200 of fully qualified converter boards
1^{st} qrt. 2013	• Delivery of full quantity (1300 pieces) of fully qualified converter boards

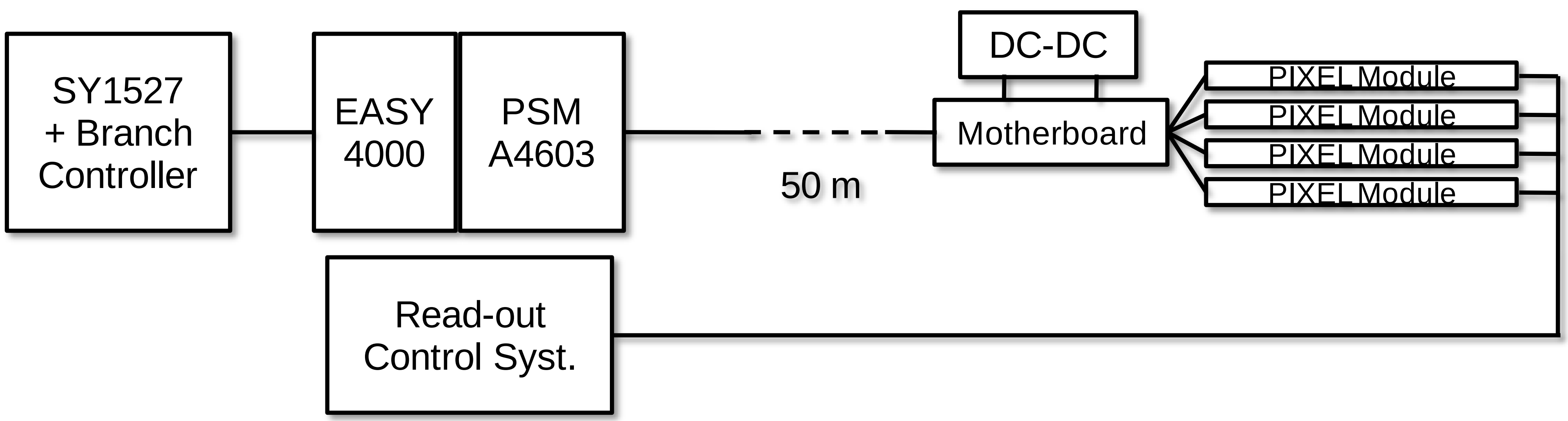
Test System

Stability Test of the whole power supply chain:

Pulsed load that emulates the varying load condition in the pixel digital current due to the orbit gaps (3 µs every 90 µs): $I_{DIG}(L)=1.9A + L \cdot 0.4A / 10^{34} cm^{-2}s^{-1}$ for 4 pixel modules



System Test with several pixel modules to fully qualify the converters



Components for Pixel System Test

Components:	Quantity:	Origin:	Status:
CAEN SY1527 Mainframe	1	CERN Pool	in Aachen
CAEN Branch Controller	1	PSI	at CERN
CAEN EASY 4000 Crate	1	PSI	at CERN
CAEN A4603 PSM	1	PSI	not modified yet
CAEN Backboard	1	PSI	at CERN
48 V AC-DC	1	CERN Pool	in Aachen
50 m LIC Cable	1	PSI	in Aachen
Converter Prototypes with AMIS2 chip	5	Aachen	in Aachen
Motherboard	1	Aachen	under development
Load Box	1	Aachen	under development
Pixel Modules	4	PSI	at CERN
Read-out System	1	PSI	at CERN

Modification of A4603 Power Supply

Modification has to be done by CAEN:

Channel	1	2	3	4
Vset:	1.8 ÷ 3 V	1 ÷ 2.3 V	0 ÷ -600 V	0 ÷- 600 V
Vmax software:	1.8 ÷ 3 V	1 ÷ 2.3 V	0 ÷ -600 V	0 ÷ -600 V
Vset / Vmax sw resolution:	5 mV	5 mV	100 mV	100 mV
Vconn:	Up to 7 V	Up to 5.8V	N.A.	N.A.
Vmon Resolution:	5 mV	5 mV	100 mV	100 mV
Vconn Resolution	5 mV	5 mV	N.A.	N.A.
Iset:	0 ÷ 13 A	0 ÷ 6 A	0 ÷ 20 mA	0 ÷ 20 mA
Iset / Imon Resolution:[1]	10 mA	10 mA	1 μA	1 μA

Increase Vconn to ~10V

Increase Vset to ~8V for sensing at converter input

Adapt regulation to negative impedance load

Modification is organized by W. Bertl:
→ A modified CAEN A4603 Power Supply will be available in December

Choice of Converter ASIC

- Reminder: We started with commercial converters to commission set-up and took reference data

- Developed of radiation hard converters using a custom ASIC developed by F. Faccios group at CERN

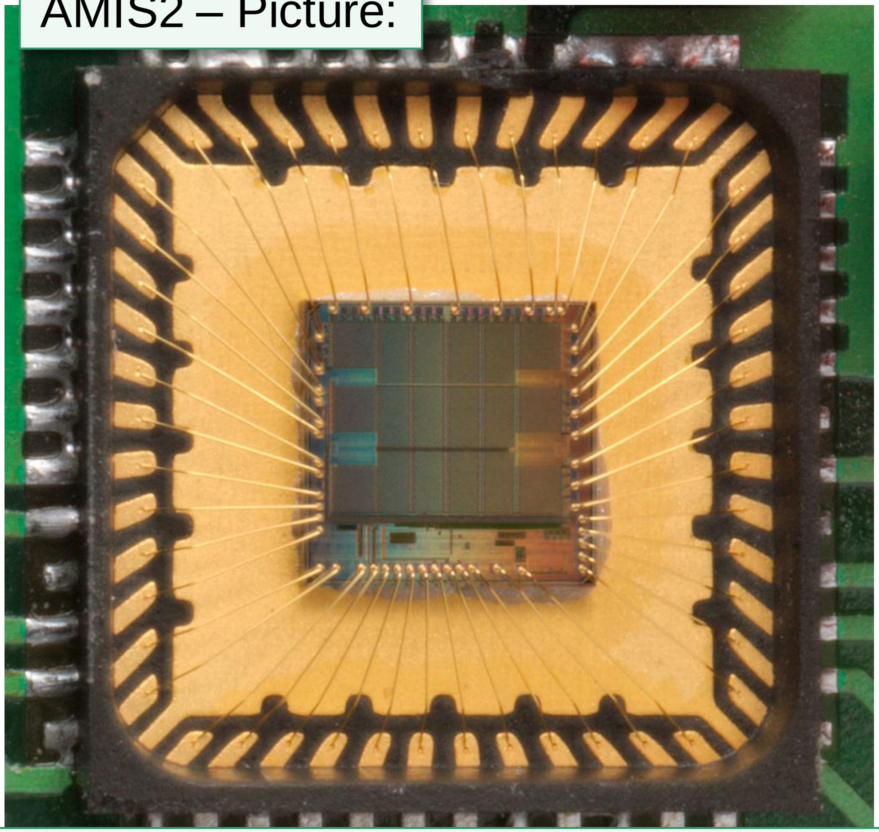
- 2 different rad-hard technologies have been identified by CERN group
  → 3 different ASICs produced:

AMIS I3T80, ON Semiconductor	AMIS1 – 1st submission	→ Tested – low efficiency (understood); system tests showed unsatisfactory EMI behaviour (high noise level)
	AMIS2 – 2nd submission	→ ASICs delivered to CERN and after packaging to Aachen → Converter boards have been produced → Repeat system tests, efficiency measurements,
SGB25V GOD, IHP Frankfurt/Oder	IHP1 – 1st submission	→ Radiation hardness of LDMOS transistors proven (F. Faccio, S. Michelis, ..) → 1st submission: ASICs have been delivered to CERN, (re-)processing problems
	IHP2 – 2nd submission	→ 2nd run will be in January 2010 – Chips available May 2010

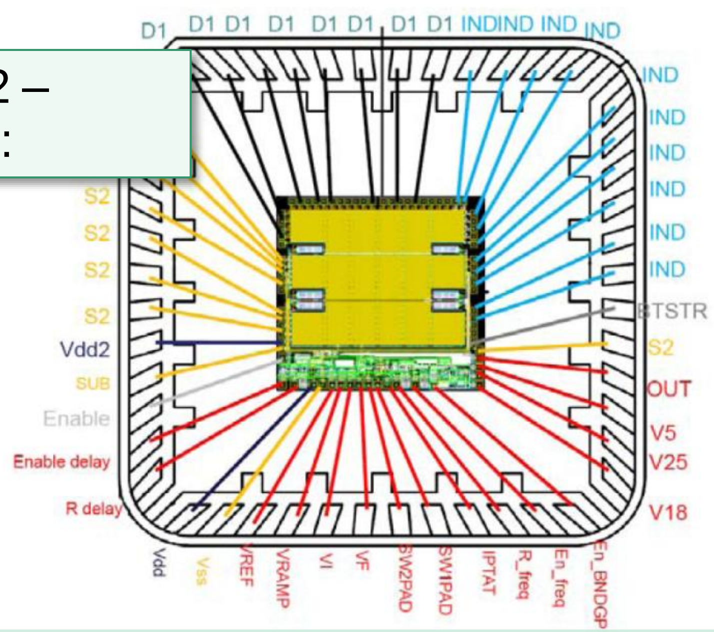
AMIS2 – Chip & Technology

- Package: QFN48 (7mm x 7mm)
- No on-chip protection (over-V, over-I, over-T)
- Tested up to 300 Mrad = 3000 kGy with only 2% efficiency loss (after annealing) (→ backup slides)
- Integrated feedback loop with bandwidth of 20kHz
- Internal voltage reference
- Lateral HV transistors are used as power switches
- Noise and efficiency on upcoming slides

AMIS2 – Picture:



AMIS2 – Pinout:

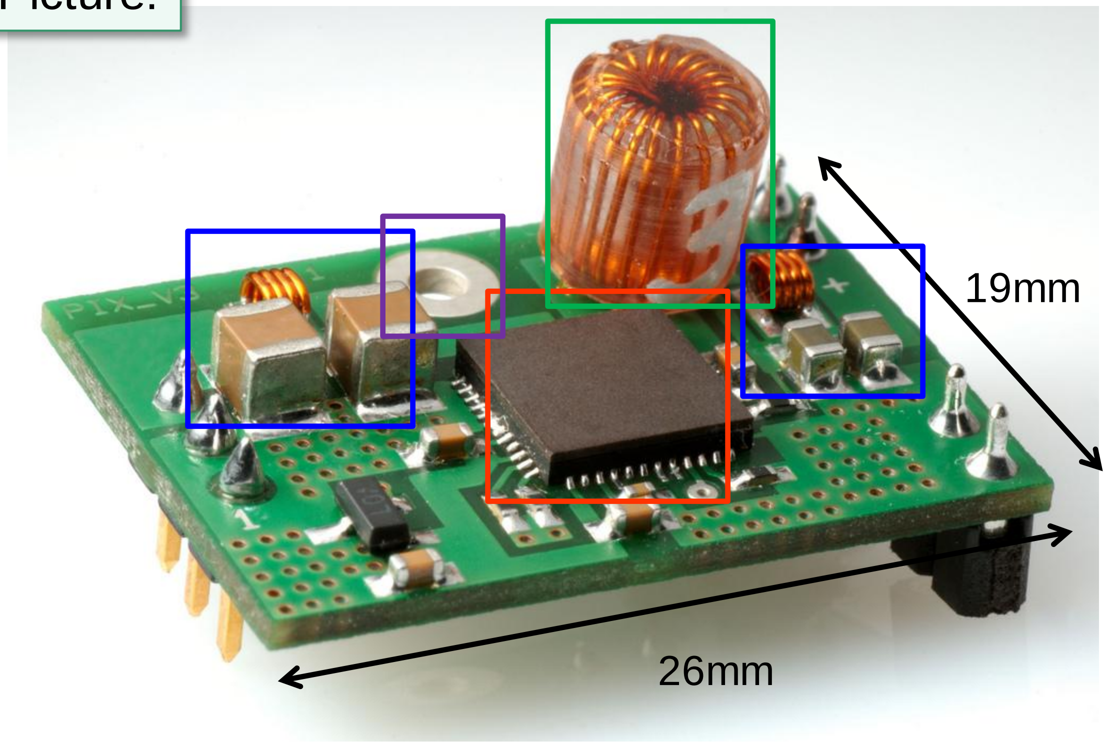


→ Most chips will be delivered with a smaller package: QFN32 (5mm x 5mm)
→ Delivery date not yet known!

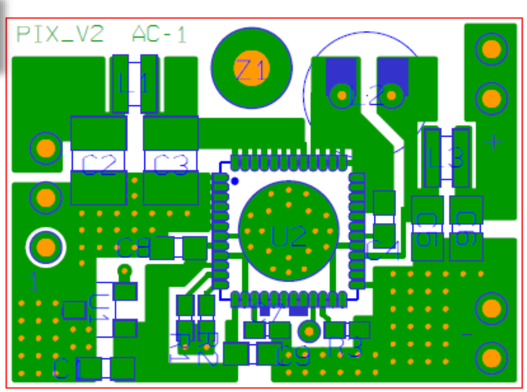
We observed some problems with this chip (thermal instability, regulation problems) so we cannot use this chip for the 1st milestone in 2010

AMIS2 – Converter PCBs

Picture:



Schematic:



PCB:
2 copper layers a 35µm
FR4 1mm
V = 19x30mm^2 x 10mm
m = 2.5g

Chip: AMIS2 by CERN
V_{IN} = 6-11V(rec.) / 12V(max.)
I_{OUT} < 3A
V_{OUT} = 3.3V (but also 1.2V, 1.8V, 2.5V, 5V)
f_S = 600kHz..3MHz

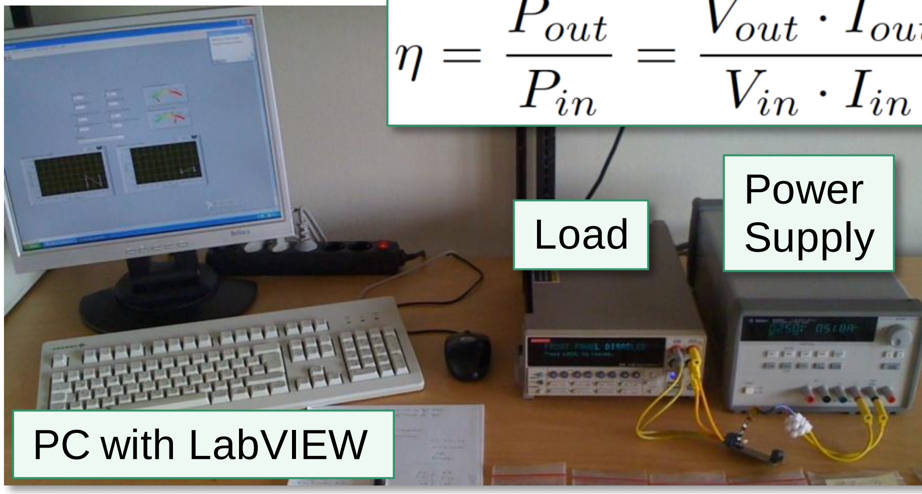
External air-core inductor:
Custom-made toroid, ∅ ≈ 6mm,
height = 7mm, L = 550nH, R = 80mΩ

Input and output π-filters
L = 12.1nH, C = 22µF

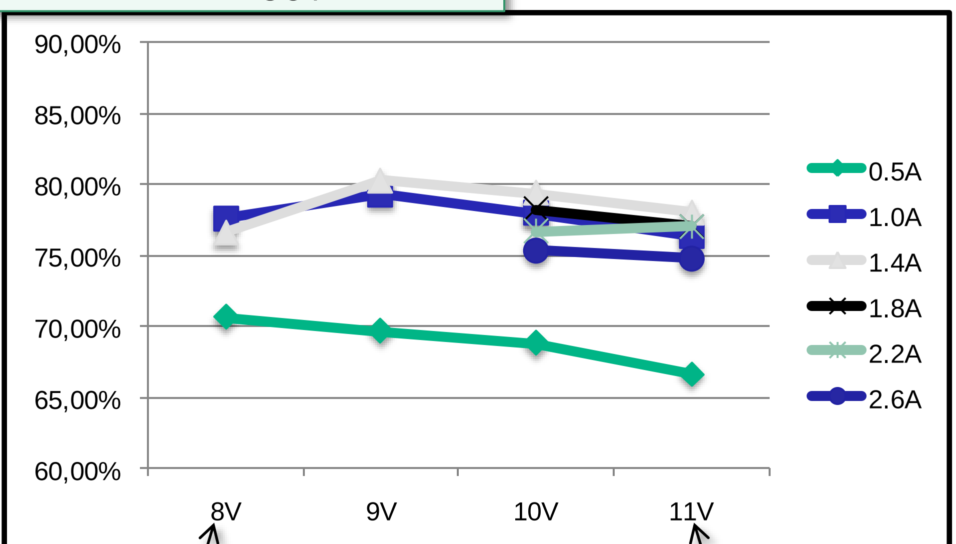
Cooling contact

Efficiency Measurements

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out} \cdot I_{out}}{V_{in} \cdot I_{in}}$$



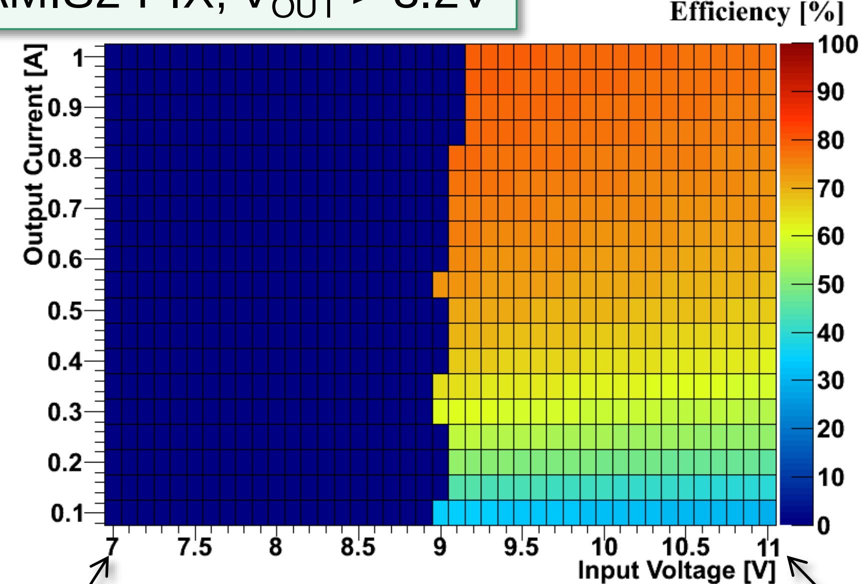
AMIS2-PIX: V_{OUT} = 3.3V



r = 2.4

r = 3.3

AMIS2-PIX; V_{OUT} > 3.2V

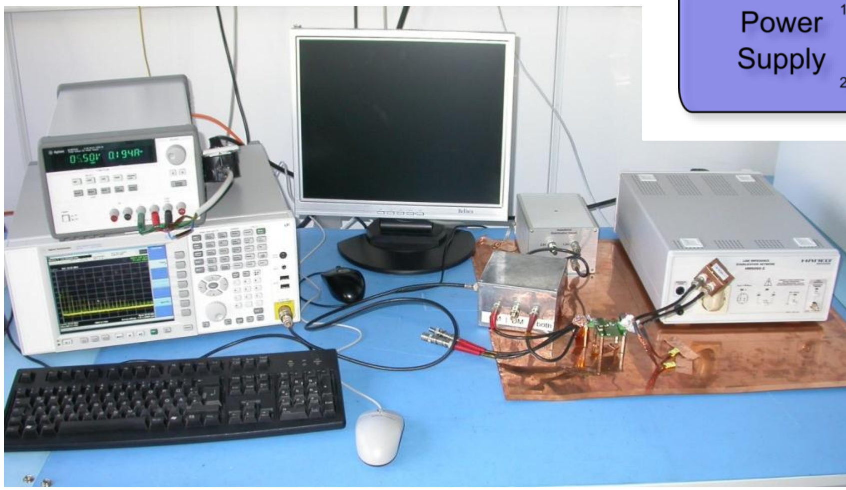


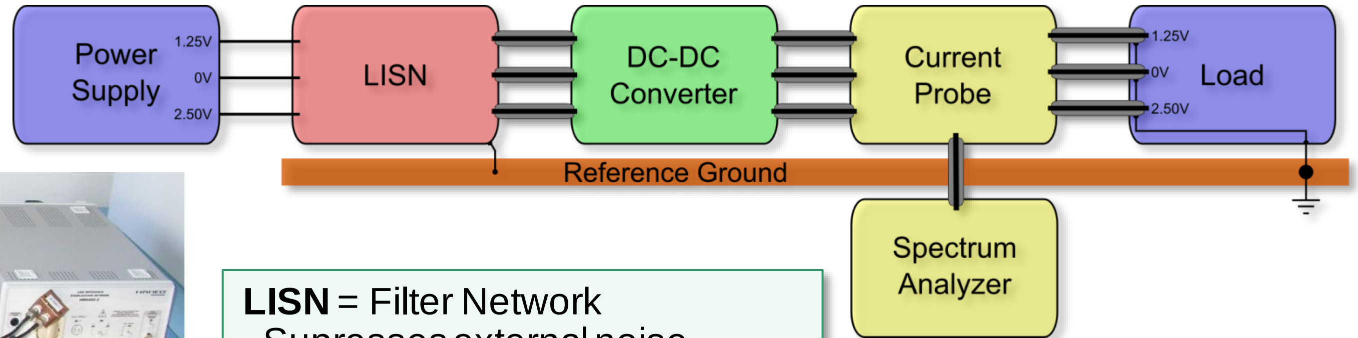
r = 2.1

r = 3.3

- Inductor: Mini Toroid (L = 600nH)
- Efficiency is 75-80% for I_{OUT} > 1A
- Regulation does not work properly for low conversion ratios
- Poor thermal stability (bandgap reference, high I_{OUT})

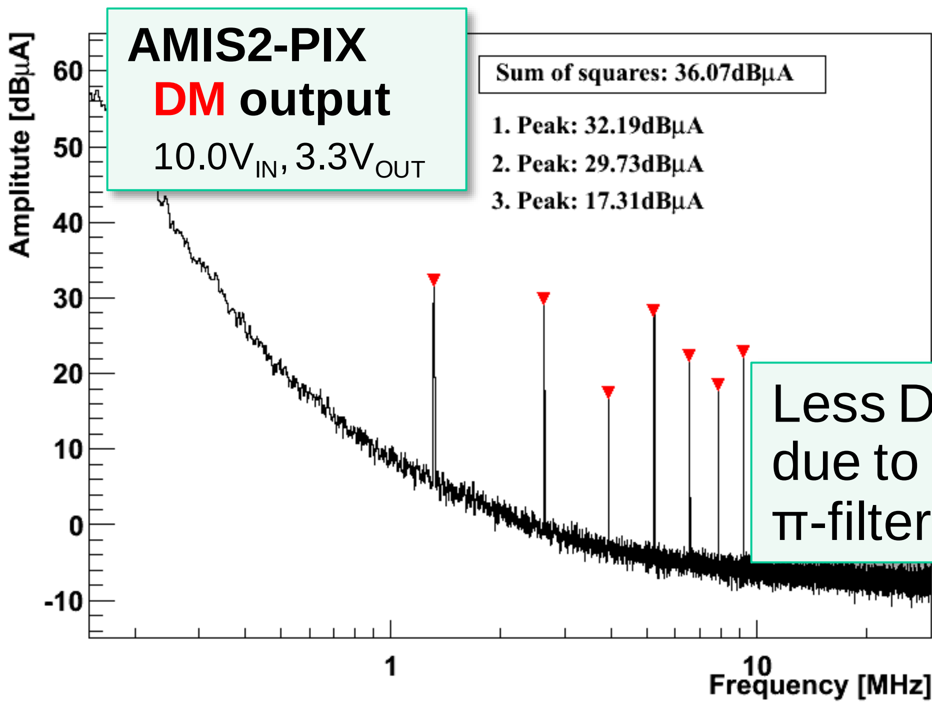
Converter Noise Spectra (EMC Studies)

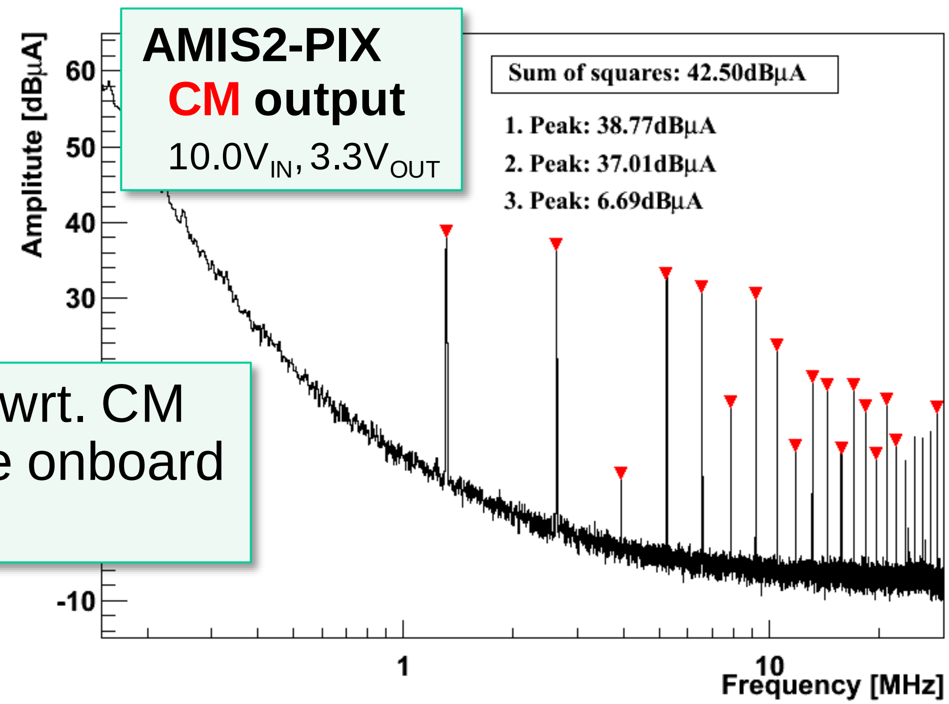




LISN = Filter Network

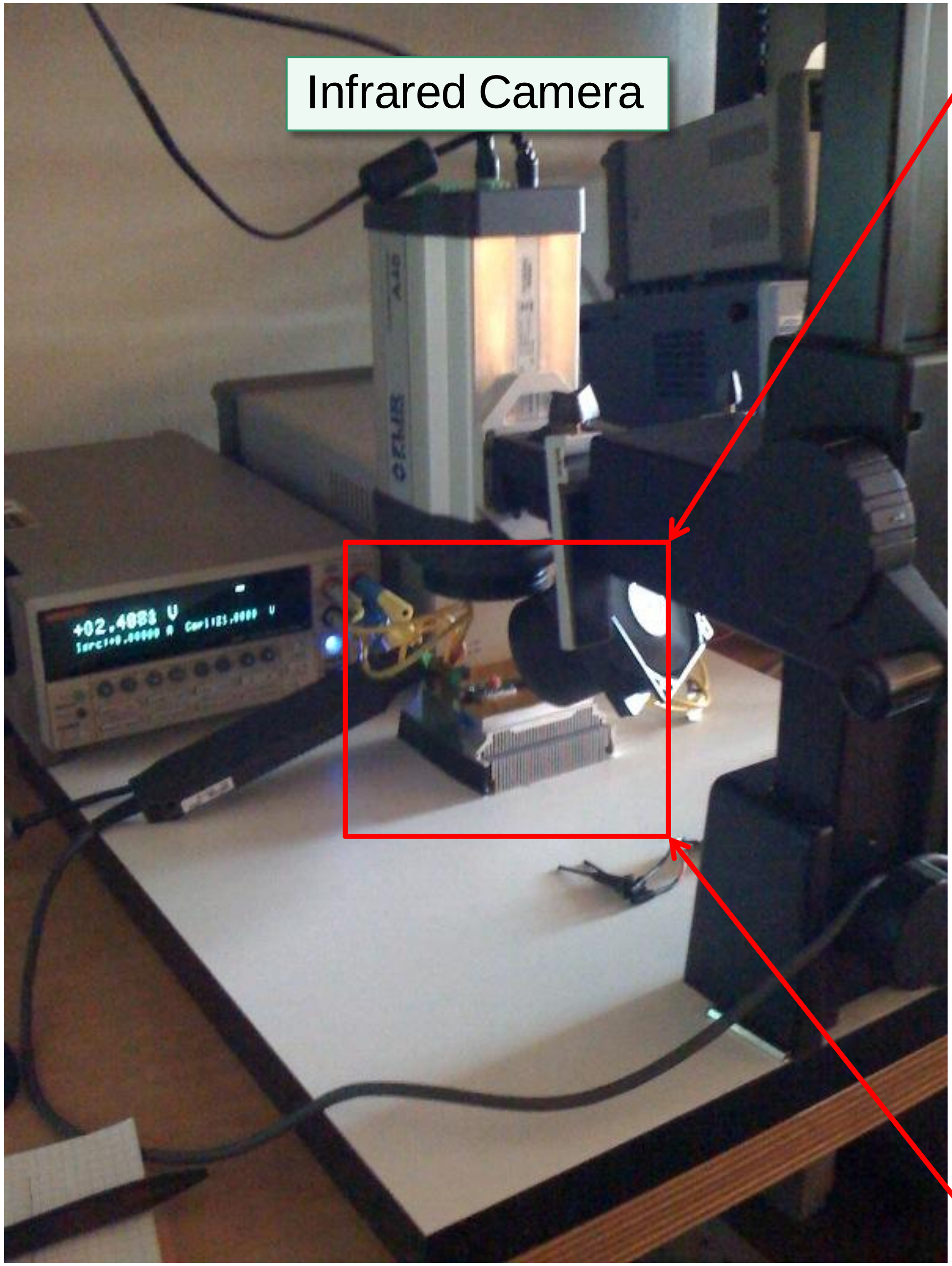
- Supresses external noise
- Avoids reflection of the noise currents inside the test system

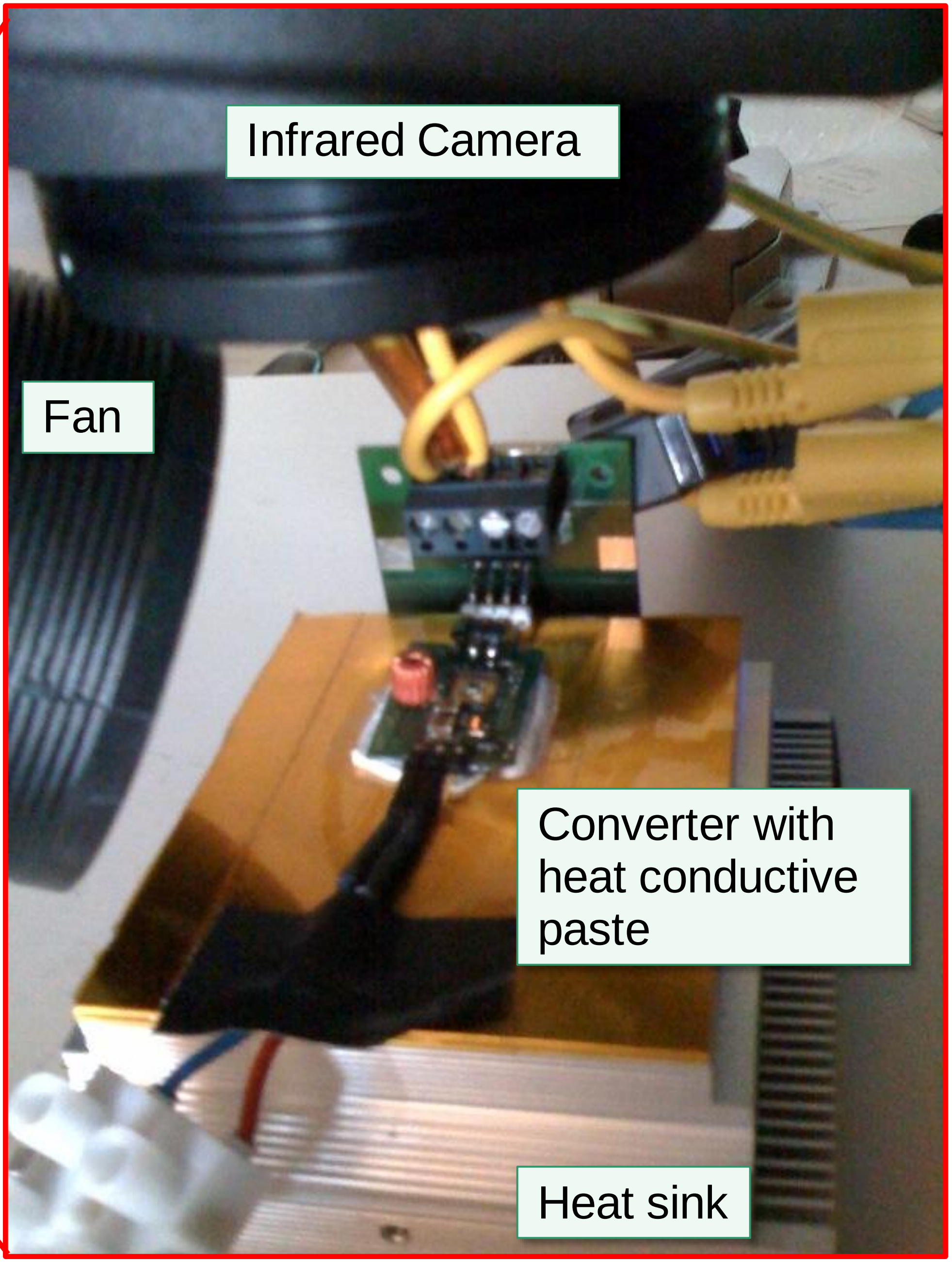




Less DM wrt. CM due to the onboard π-filters

Infrared Camera Setup with Cooling

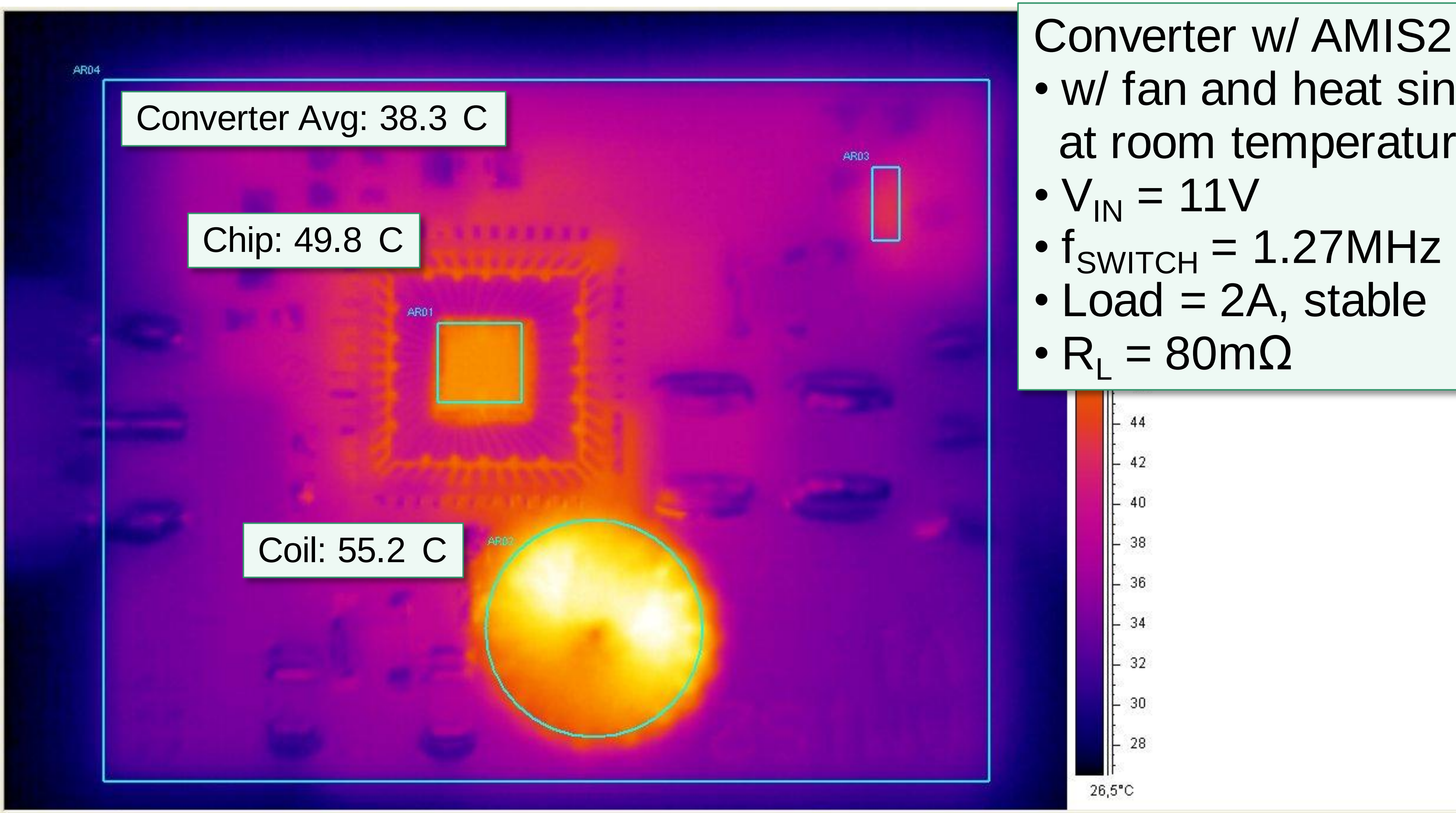




AMIS2 – Chip Temperature

Converter w/ AMIS2:

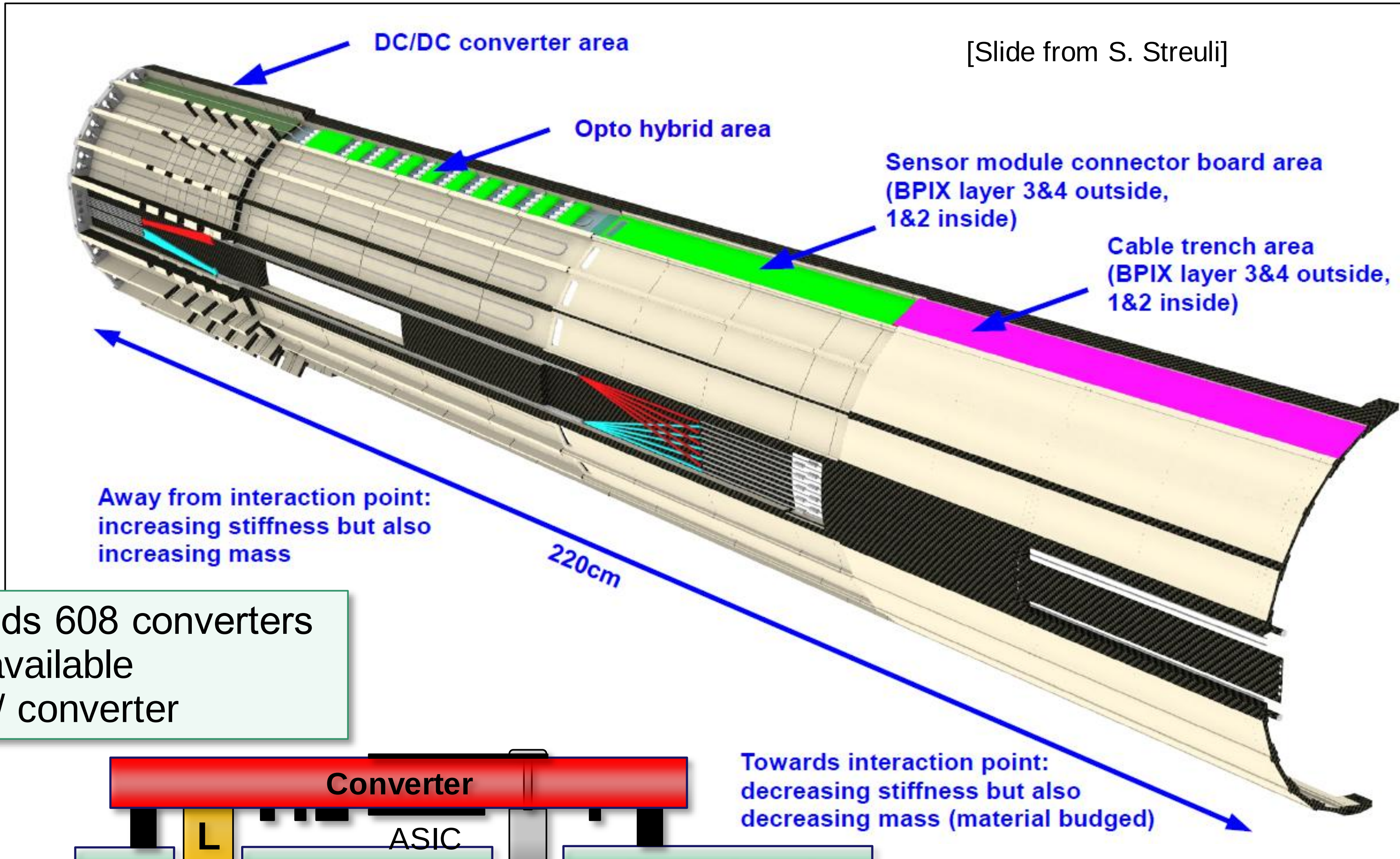
- w/ fan and heat sink at room temperature
- V_{IN} = 11V
- f_{SWITCH} = 1.27MHz
- Load = 2A, stable
- R_L = 80mΩ



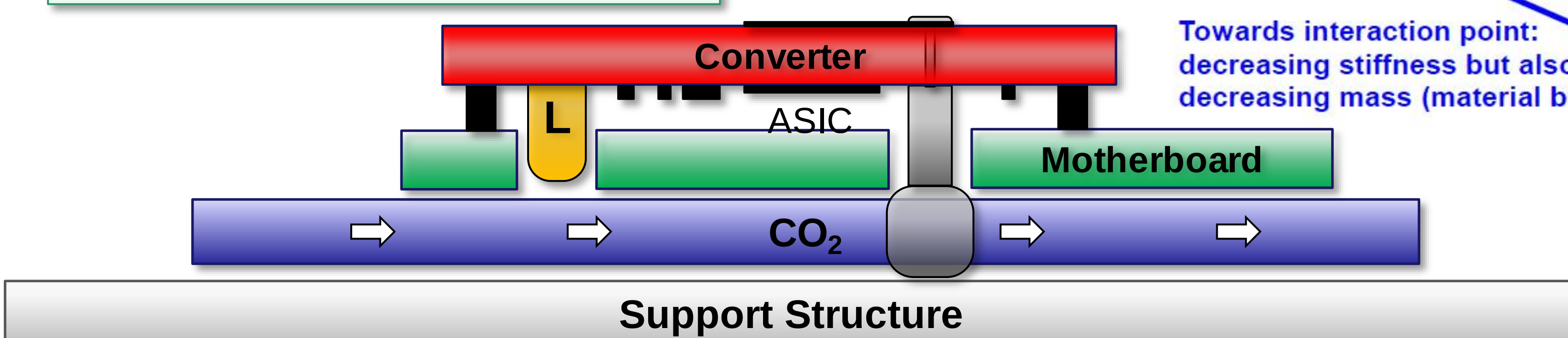
Analysis | Position | Obj. Par | Image | Text comment

Label	Value [°C]	Min	Max	Max - Min	Avg	Stdev	Result	Expression
Image		26,3	62,8	36,5				
AR01		44,0	51,8	7,8	49,8	1,4		
AR02		43,5	62,8	19,3	55,2	4,8		
AR03		39,1	43,0	3,9	41,7	0,9		
AR04		28,8	62,8	34,0	38,3	6,0		

Converter Implementation



→ BPIX needs 608 converters
Volume available
≈ 12cm^3 / converter



Summary and Questions

- The CMS Tracker plans to implement buck converters in the pixel system at Phase I (and in the outer tracker at Phase II)

- System test measurements with current pixel detector hardware will be performed in Aachen. Check converter behaviour under fast load variations and possible inferference with CAEN power supply

- Buck Converters with ASICs from CERN have been developed

- PCBs are equipped with small, low-mass 0.6µH air-core toroids with low R_L and π-filters on the in- and output of the converter

- The efficiency is up to 80%. Impact of emitted noise has to be tested with pixel test system

- We also develop new Converters with commercial Chips (Enpirion 5336QI) for cross checking the test system

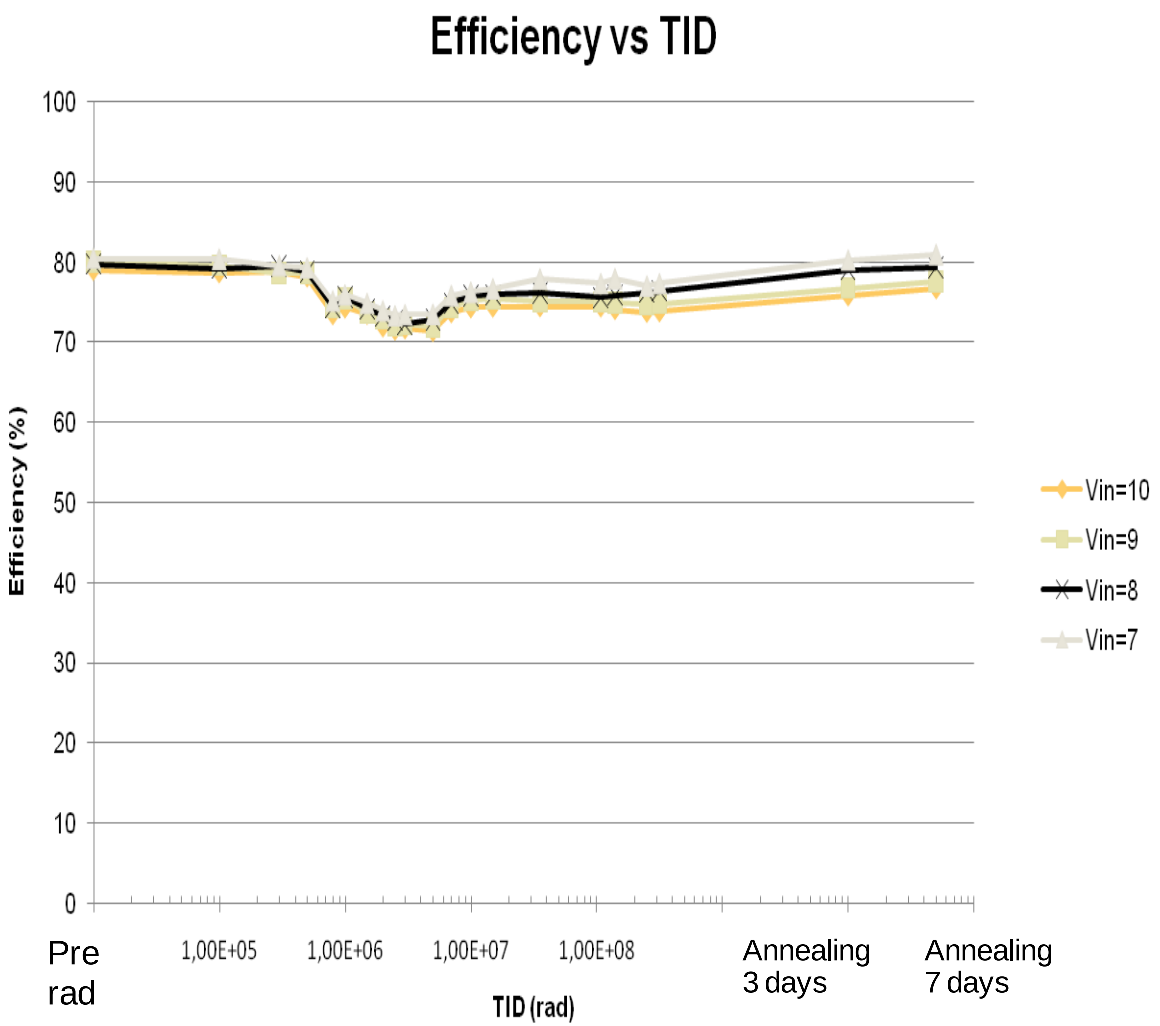
- AMIS2 Chip does not yet fulfill the Phase I specifications (Conversion ratio, thermal instability, ..) so we cannot use this specific chip for the 1st milestone in 2010

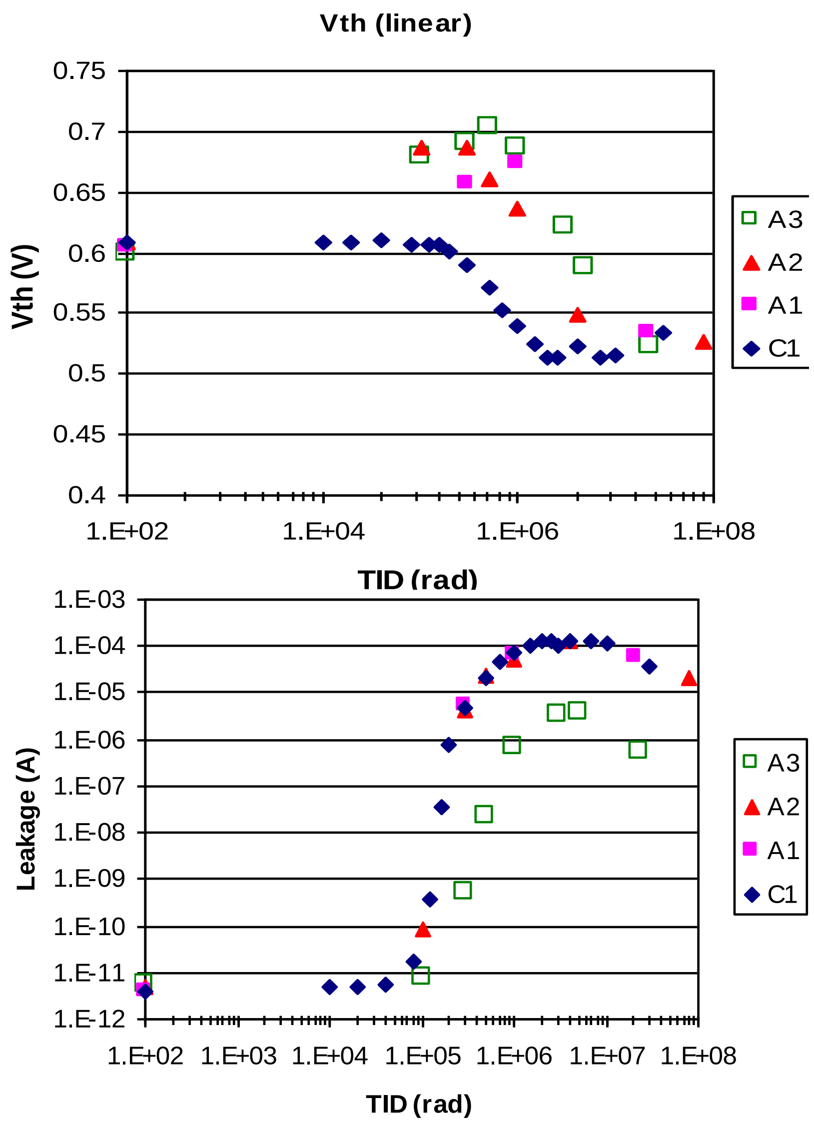
B A C K U P – S L I D E S

Specifications for Pixel DC-DC Converter

Specification	
radiation level	up to 2-3x10^{14} cm^{-2} (fast hadrons) up to 150 kGy (?)
magnetic field	4 T
voltage conversion	6.6 V → 3.3 V (2:1)
current capabilities	< 2.8 A
volume	length = 3.2cm , width = 2cm, height <1.4cm
form factor	piggy-board with board-to-board connectors
material budget	uncritical
output ripple	compatible with PSI46 ROC
specific requirements	• behaviour for very fast load variations due to the orbit gaps • stability of operation together with long pixel cables and the CAEN A4603 modules
quantity	944 pieces required for FPIX + BPIX 1400 including spares and prototypes

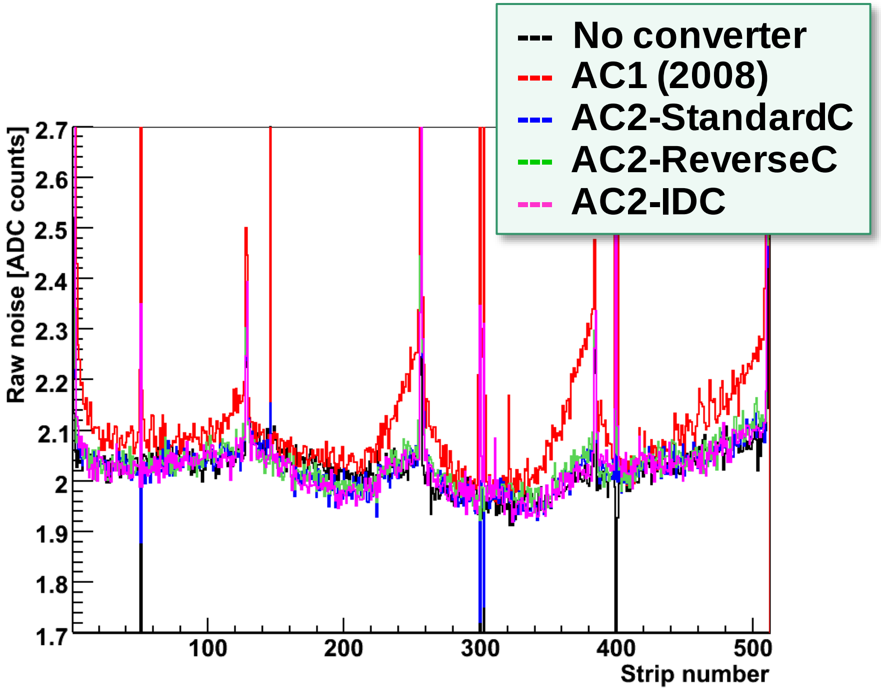
AMIS 2 Irradiation Results [S. Michelis, CERN]





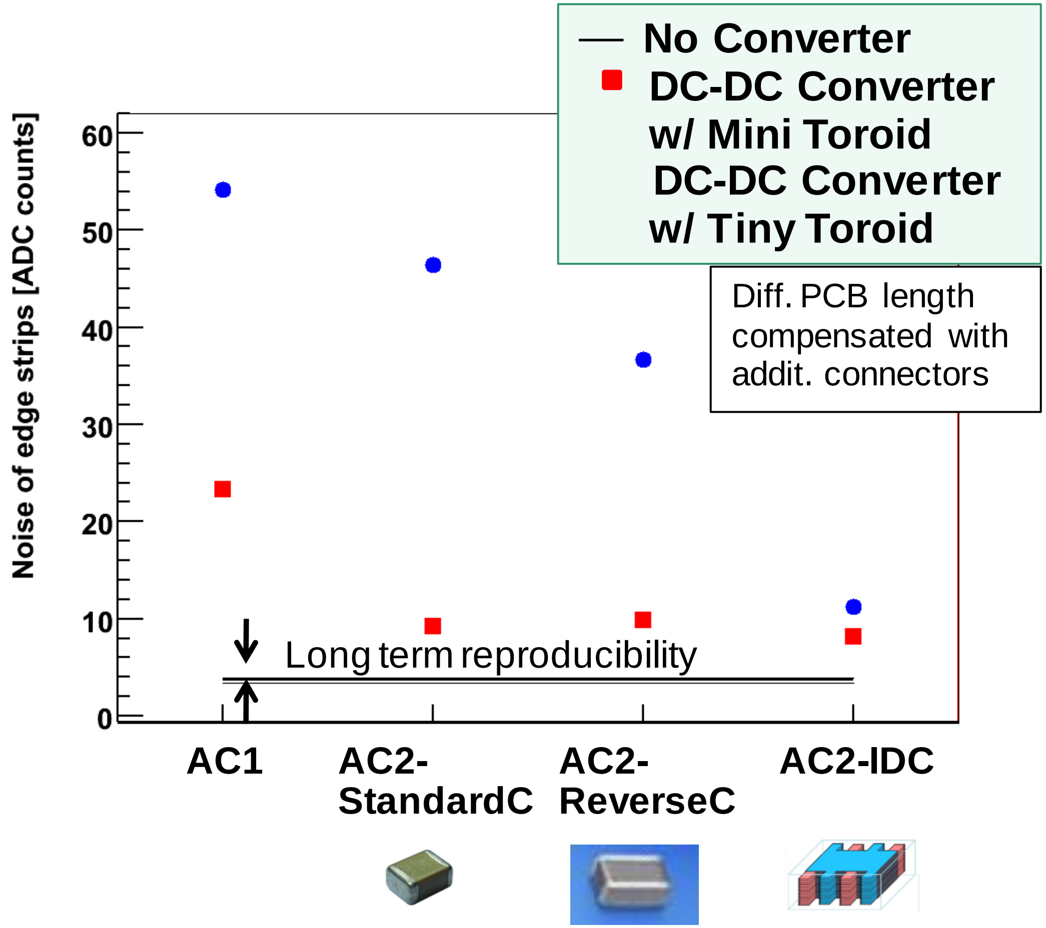
X-ray radiation tests shows a decrease of the efficiency mostly due to the radiation induced leakage current, compensated by the threshold voltage shift

Noise of the Aachen Converters



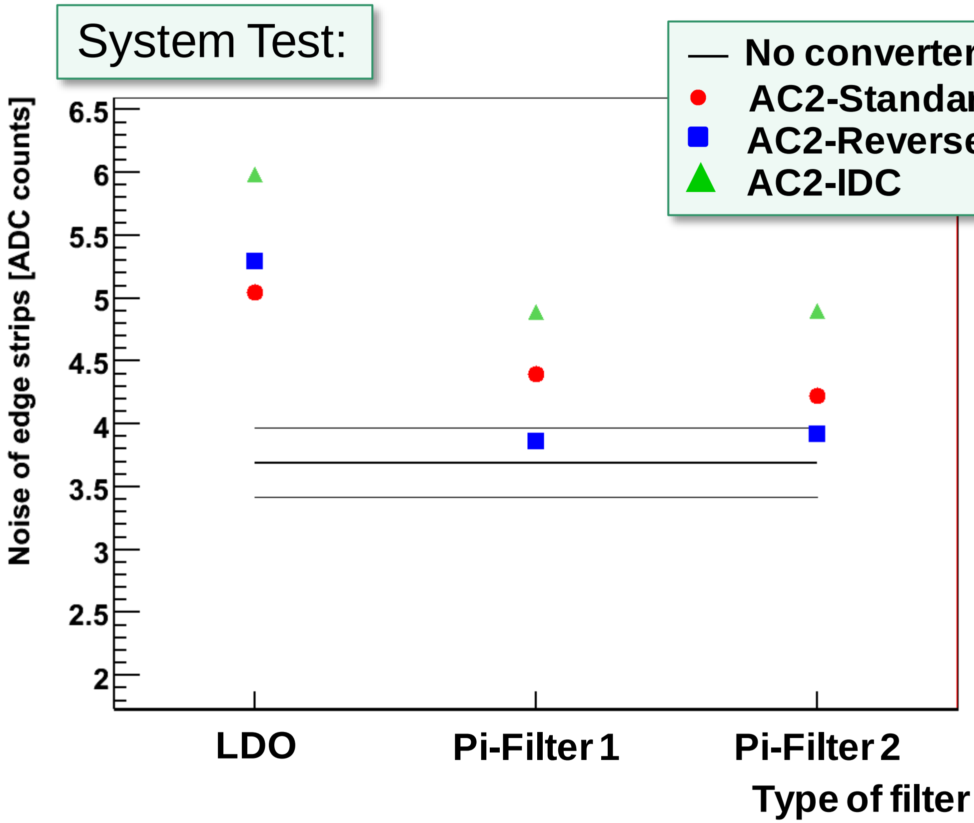
Sensitive variable chosen for all following comparisons:

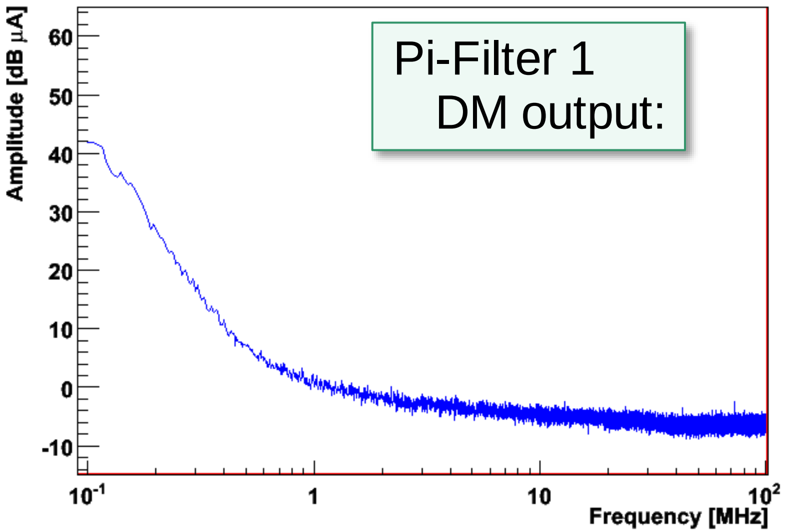
$$N = \sqrt{N_1^2 + N_{512}^2}$$

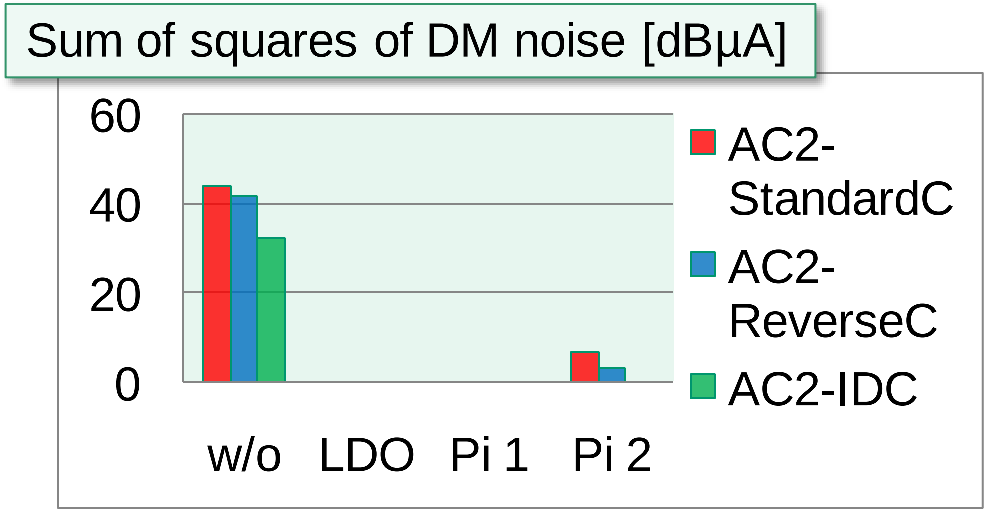


- Lower noise than with 2008 boards
- Mini Toroid shows lower noise and 5-30% higher efficiency ($\Delta I_L = V_L \cdot t_{ON} / L$)
- Boards with IDCs perform best

Noise Filters: π-Filters vs. LDO







- π -filters are as effective as LDO regulator!
- AC2-IDC performs “worst“ with filters/LDO; likely reason: higher CM

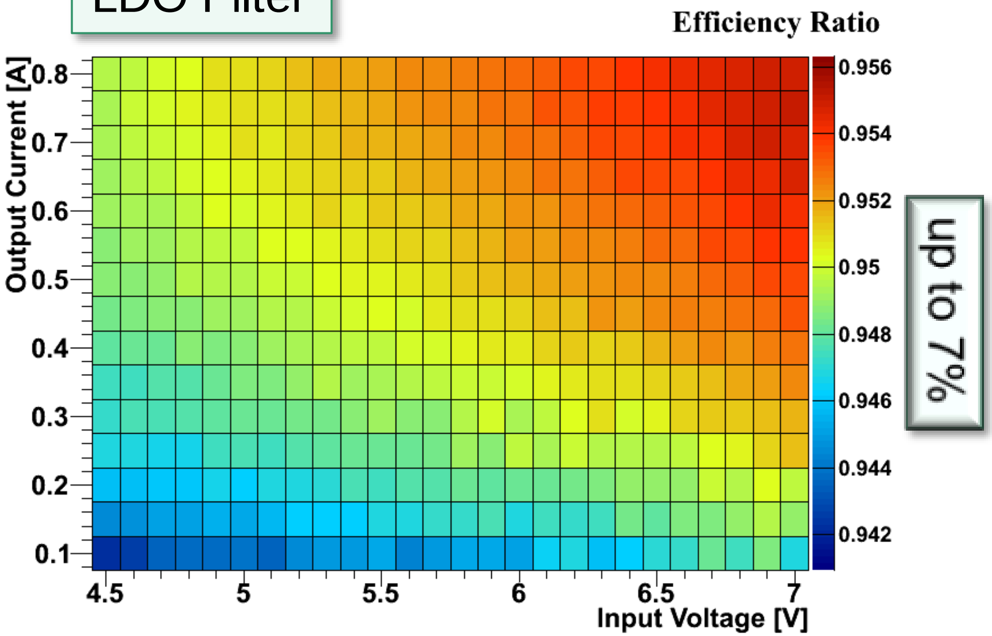
π-Filters vs. LDO: What about Efficiency?

Ratio of the efficiency with LDO / π-Filter and the efficiency without LDO / π-Filter

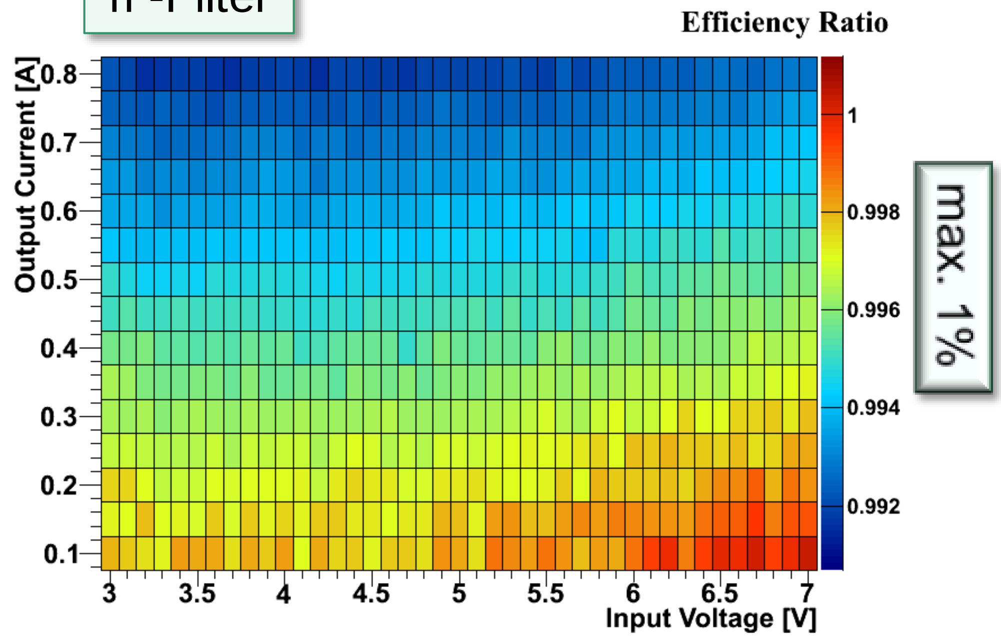
→ was measured for all board types, filters and V_{OUT} = 1.25V and 2.50V;

e.g. standard capacitors, 1.25V:

LDO Filter



π -Filter



- Losses of up to 7% observed with LDO regulator (50mV drop out voltage)
- Losses with our π-Filters stay below 1%
- π -filter clearly preferred