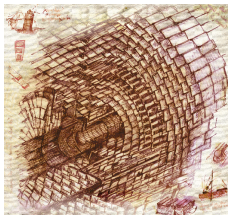
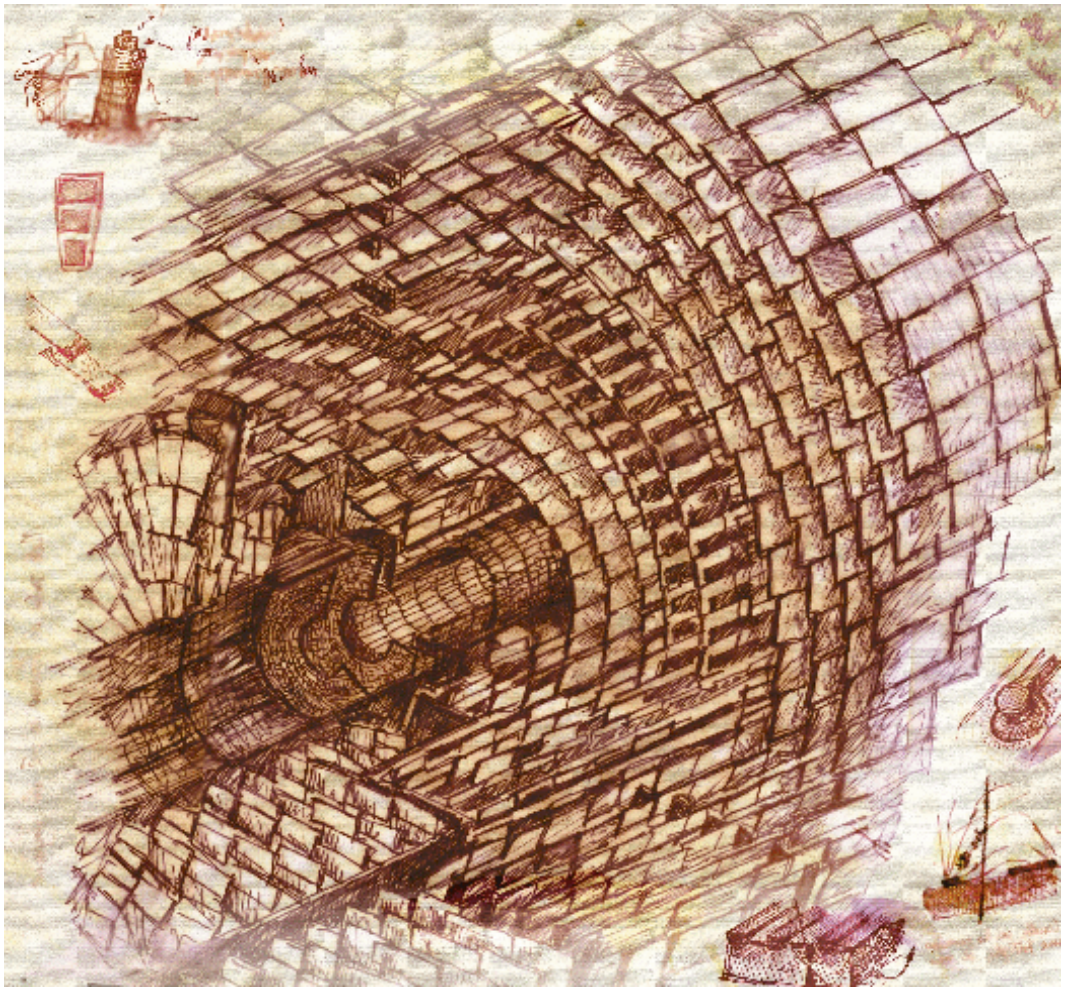
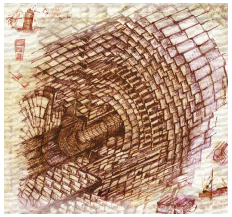


SLHC L1 Tracking Trigger Summary Part b

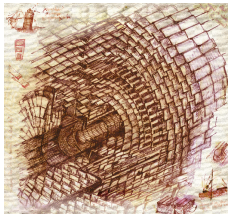




Cluster Width Approach for Tracker L1 triggering at sLHC

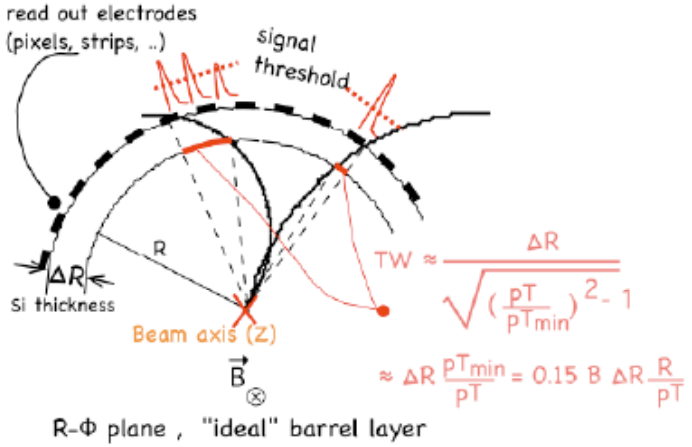
N.Beaupère, J. Bernardini, F. Bosi, G. Boudoul, D. Contardo,
R. Dell'Orso, A. Messineo, F. Palla, G. Parrini, E. Vataga

CMS Upgrade Workshop
29 October 2009



Cluster Width Approach

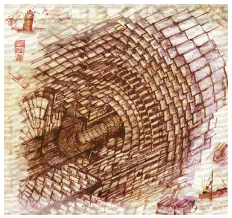
First principle of Cluster Width approach



G. Parrini

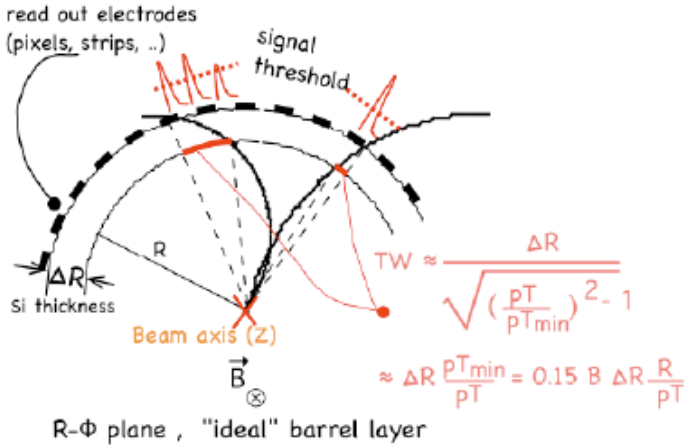
Select clusters associated to higher Pt
tracks by rejecting ones with larger width

Cluster Width (#strips) ~ (Sensor Thickness/Strip Pitch) x Layer Radius / Pt



Cluster Width Approach

First principle of Cluster Width approach

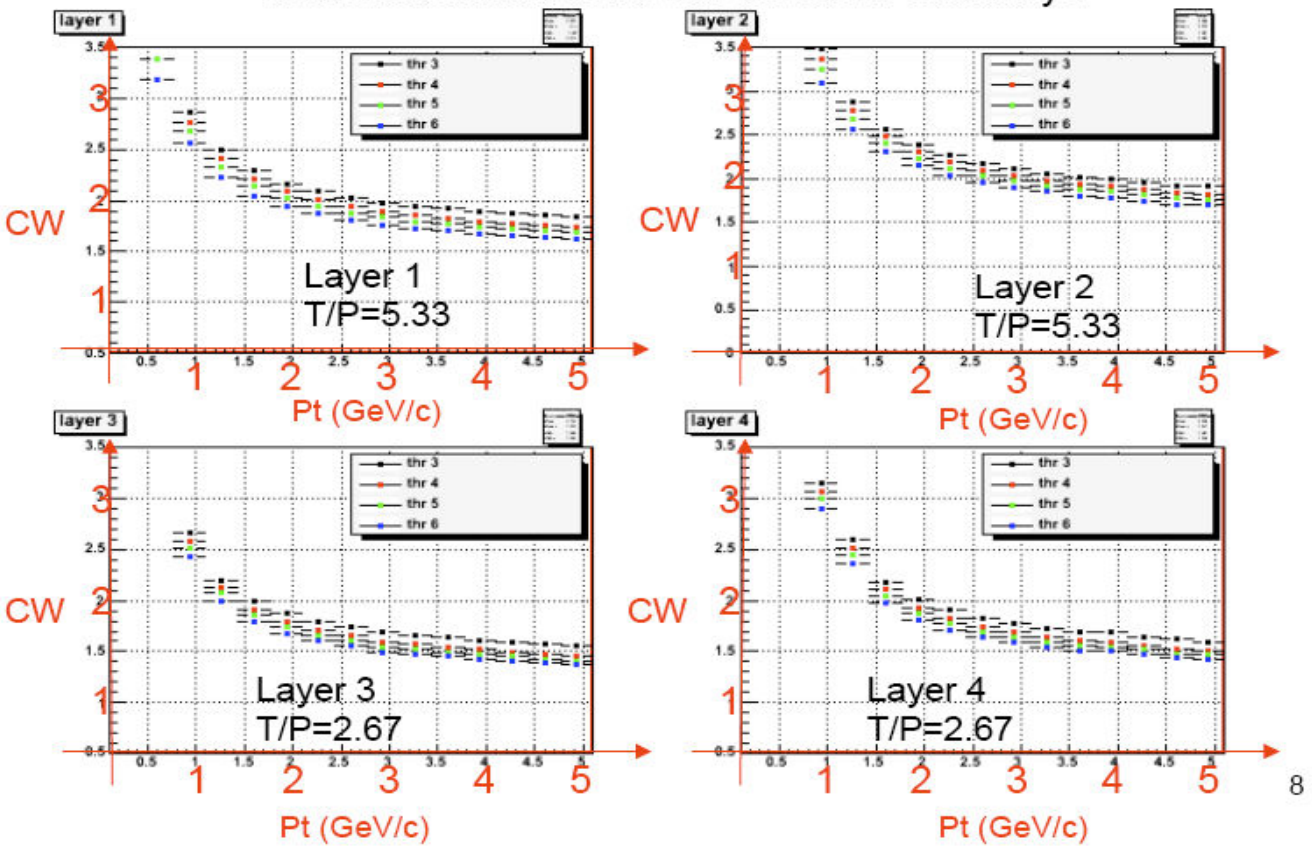


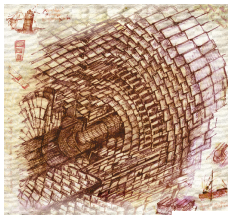
- **A method for local data reduction, at the single sensor level**
  - **Is used to reduce data rates from Slave sensor to Master tier in Stacked Modules**
- **Here it is looked at as a standalone method, in the region of the TOB**
- **Note: needs to be completed by another solution at high eta**

Cluster Width Approach

Cluster Width Profile Vs Pt

Gives an indication of the cluster width cut value,
Thresholds need to be fine-tuned for each layer





Cluster Width Approach

Cluster Width in cosmic ray events

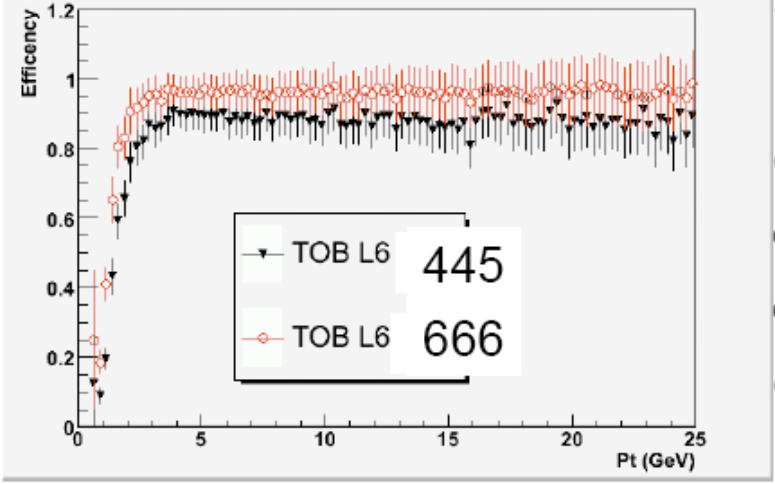
R. Dell'Orso - J. Bernardini

Efficiency TOB Lay 6 (data)

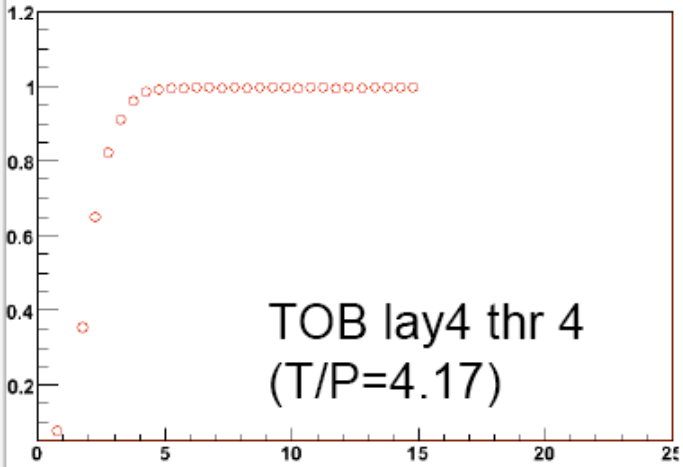
Efficiency TOB Lay 4 (sLHC-std hybrid simulation)

TOB layer 6 should be equivalent to layer 4 of sLHC std hybrid layout

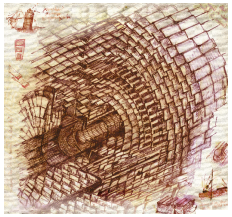
Data



sLHC simulation



Cluster efficiency compatible between CRAFT/simulation



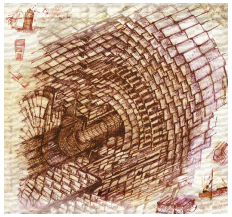
Cluster Width Approach

Goal of the study and layouts

- Establish performance
  - low Pt rejection versus high Pt efficiency as a function of
    - Layout parameters (Thickness, Pitch, Radius)
    - Selection parameters (Clustering Thresholds, Cluster Width Cut)
- Study on 4 RΦ Outer Barrel Layers
  - Based on SLHC Strawman A Hybrid
  - R = 50, 70, 90, 110 cm
  - No Lorentz angle compensation

Parameters of the simulated layers :

	Layer 1			Layer 2			Layer 3			Layer 4		
Sensor thickness T (μm)	500	320		500	320		500	320		500	320	
APV #/module	4	8	12	4	8	12	6	8	6	6	8	6
Strip #/module	512	1024	1536	512	1024	1536	768	1024	768	768	1024	768
Strip length (cm)	4.65			4.65			4.65			4.65		
Strip Pitch P (μm)	180	90	60	180	90	60	120	90	120	120	90	120
T/P	2,78	3.56	5.33	2,78	3.56	5.33	4.17	3.56	2.67	4.17	3.56	2.67



Cluster Width Approach

Choice of few Optimised Configurations (1)

4 layers in trigger (L1/L2/L3/L4)

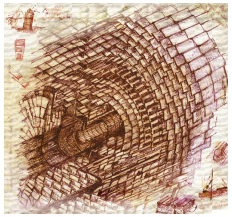
« high number of clusters / intermediate rejection »

Select layers with 99% of tracks efficiency at high Pt with >=3 hits out of 4 layers
and a cluster rate ~ 3.5 MHz per APV
⇒ 96% efficiency per layer with muons at Pt>5GeV/c

Layer #	1	2	3	4	Total
Sensor Thickness T (µm)	350	350	350	350	
APV #/module	**12**	**12**	**8**	**8**	
Strip #/module	1512	1512	1024	1024	
Strip length (cm)	4.65	4.65	4.65	4.65	
Strip Pitch P (µm)	60	60	90	90	
T/P	**5.33**	**5.33**	**3.56**	**3.56**	
Total # Strips	**1.587.600**	**1.814.400**	**1.689.600**	**1.894.400**	**6.896.000**
CW (strips)	**<=2**	**<=2**	**<=2**	**<=2**	
Strip threshold	**3**	**3**	**3**	**3**	
Integrated rejection	**0.25**	**0.25**	**0.35**	**0.37**	
Occupancy/APV (.10-3)	**0.23**	**0.12**	**0.21**	**0.13**	
ClusterRate /APV (MHz)	**6.95**	**3.51**	**4.39**	**2.75**	
ClusterRate/Layer (GHz)	**87.5**	**50.6**	**58.0**	**40.7**	

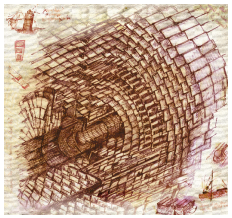
Layer 1:
3.5 MHz
not reachable

#Strips x2 ?



Conclusion

- Cluster Width approach is a simple solution to reduce cluster rate for low Pt track clusters with :
  - *Flexibility to chose a design adjusting thickness/pitch/length according to given criteria on : band width - power consumption - number of channels - material budget*
  - *Flexibility to adjust the rejection/efficiency performance with threshold and Cluster width for a given design*
  - *Redundancy with multiple layers to ensure large amount of tracks with more than 2 hits*
- Few designs shown in this presentation are satisfying reasonable criteria on cluster efficiency:
  - *To be checked the track reconstruction efficiency pattern like method as proposed with associative memories implementation.*
  - *Cluster and Track collections to be provided for Trigger studies*
- MonteCarlo studies are validated by cosmic data :
  - *Soon to be checked with collisions data*
- Needs to be completed by other solution at higher eta :Stack strip modules



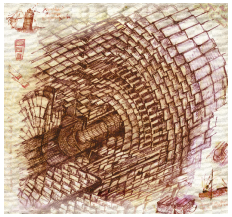
Tracker Trigger System: Possible Architectures for L1 Track Formation

- **Marvin Johnson & Ulrich Heintz, for the Tracker Trigger Group**
  - **October 2009**

- **Currently Active**

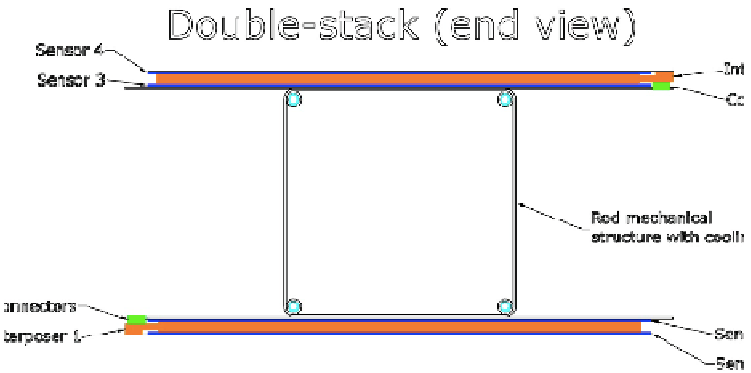
  - **U. Heintz , M. Narain from Brown U.**
  - **E. Hazen, S. Wu from Boston U.**
  - **M. Johnson, R. Lipton from FNAL.**

- **Very interested in getting new members**

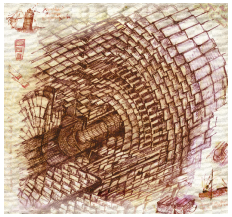


Goals and Constraints

- **Develop a robust track trigger for SLHC upgrade**
  - **find high pt tracks**
  - **identify isolated tracks**
  - **2.4 GeV/c minimum Pt**



- **Hardware**
  - **Current gate array technology to test ideas**
    - **Easy to scale to larger devices**
  - **Optical link rate < 10 GB/sec**

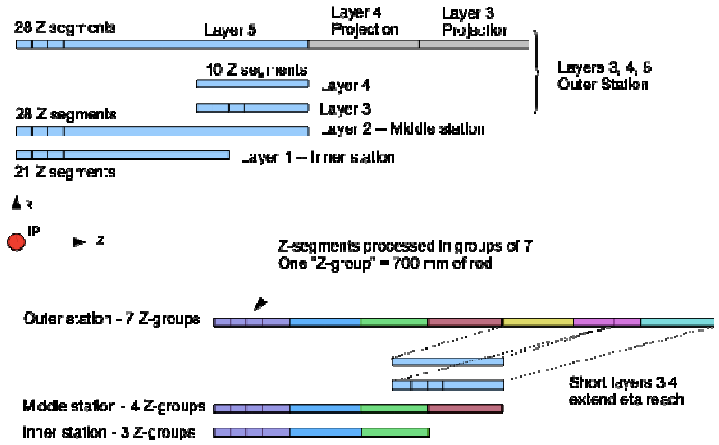


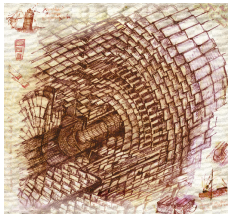
Tracker

- **Based on long barrel design but not restricted to long barrel design**

- **Layers 3 and 4 extend eta reach**
  - **Map 3 and 4 to outer layer**
  - **Logically this reduces the long barrel to a 3 layer design**

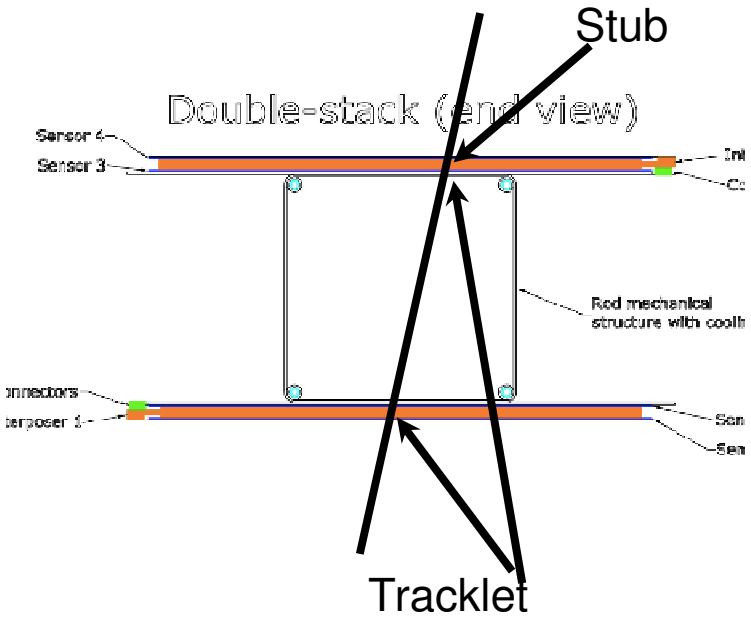
R-Z view of 1/4 of barrel showing Z segmentation

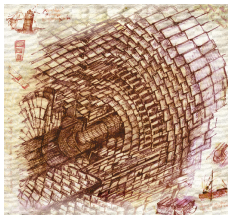




Definitions

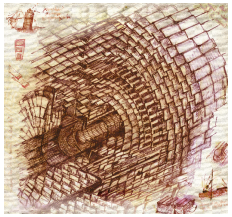
- **Stub:**
  - 2 hit track from a stack
- **Tracklet:**
  - 4 hit track formed from 2 stubs on a rod
- **Track:**
  - Combination of at least one tracklet and some stubs
- **Layer:**
  - Double stack





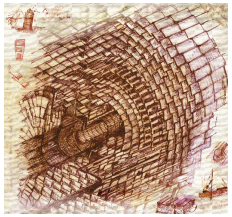
Detector Design

- **Send track stub data off detector**
  - **forming tracklets on detector requires stack to stack communication**
- **Data rates show that this is feasible**
  - **inner layer has 8 hits per 100 cm^2 sensor/crossing**
    - **rate is a factor of 10 over Cornell simulations**
  - **At 20 bits/ event this is less than 7 GB/sec**
  - **More on this later**



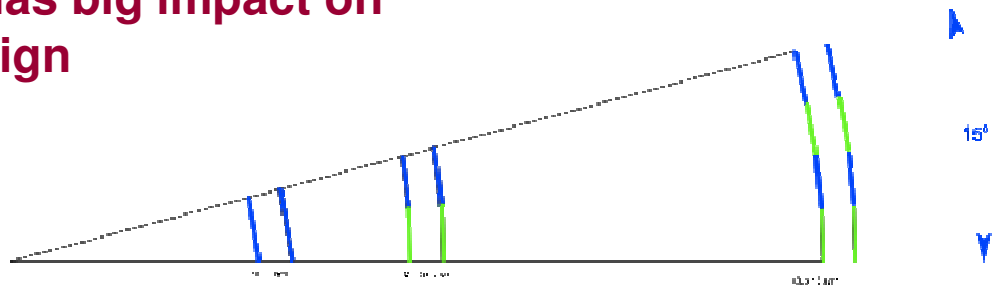
Practical Limits

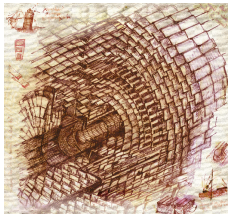
- Too many equations for single FPGA
- Requires too many high speed serial lines for single FPGA
  - All track data must be loadable into an FPGA in one crossing (25 ns)
  - Trigger hits must also be sent out at the same time
- Must spread problem over several FPGA's



Trigger Sector

- **Minimum Pt is 2.4 GeV/c**
- **Trigger element is 0.1 mm by 2 mm**
- **7 rods**
  - **4 outer, 2 middle, 1 inner**
- **Minimum Pt has big impact on hardware design**

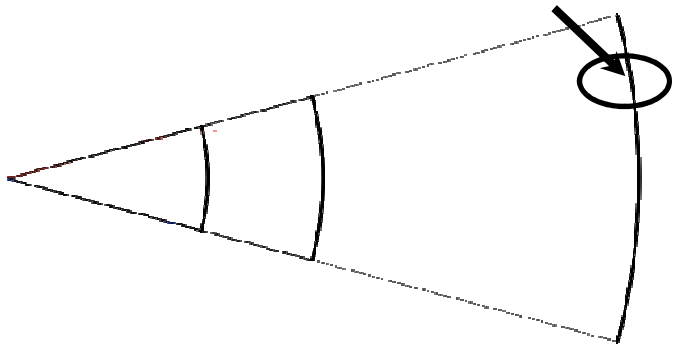




Why Tracklets?

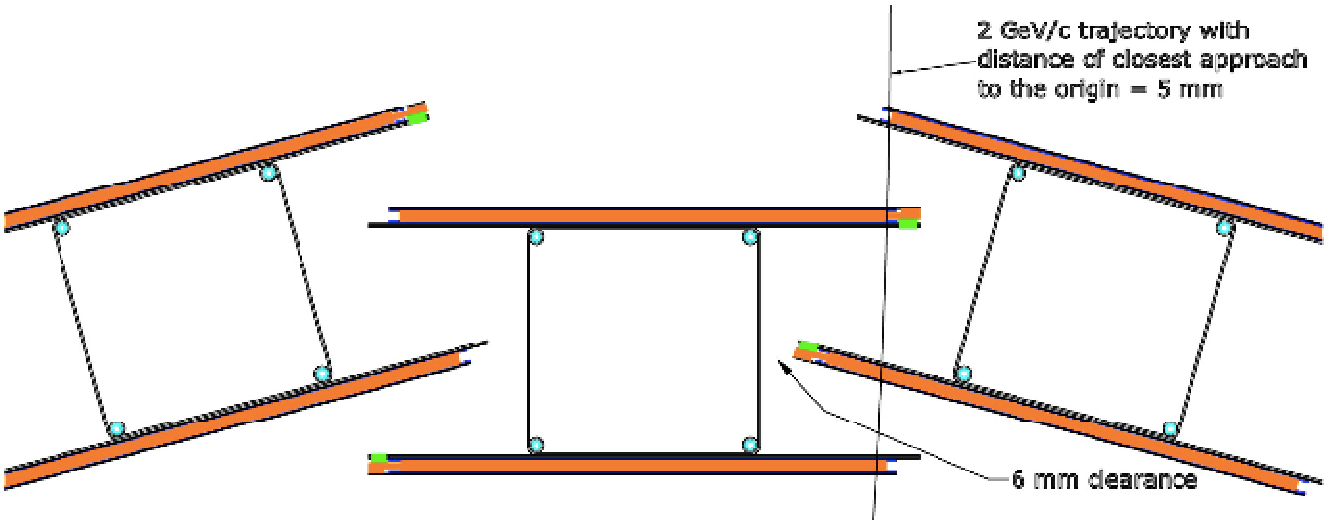
- **Consider 3 layers and no tracklets (track hits but no Pt)**
- **To find tracks need to test all combinations of tracks from all layers (minimum Pt covers entire sector)**
  - **Must be completed in 25 ns.**
- **Tracklets allow projection of the track hit from one layer to another**
  - **reduces the range to check in the destination layer**
- **All hits can be compared simultaneously in an FPGA**
  - **Practical limit is ~10 hits/layer**
  - **Subdivide layer to stay within this limit**

Tracklets allow reduced scan range

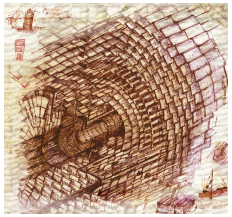


3 track 3 double-stack layer example

End View

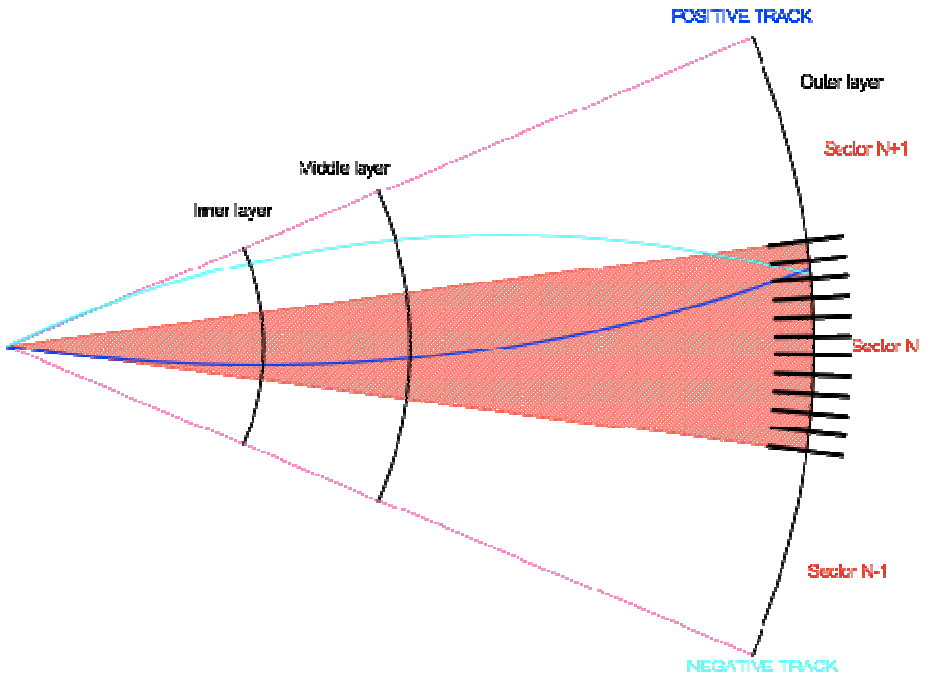


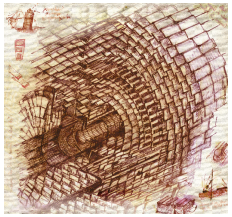
Sensor overlap so no communication between rods



Solution

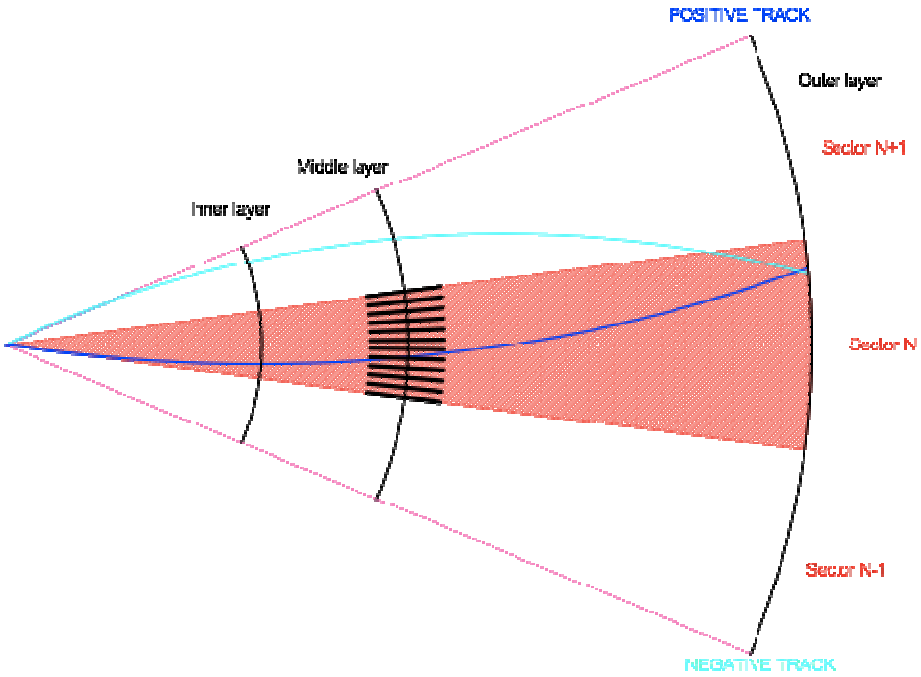
- Divide Outer layer into 12 segments
  - 36 segments for 3 sections
- Tracklets from inner 2 layers are projected to outer layer segment
- Outer layer uses stubs
  - Reduces effect of hardware failures
- Segments must overlap due to imprecise projection



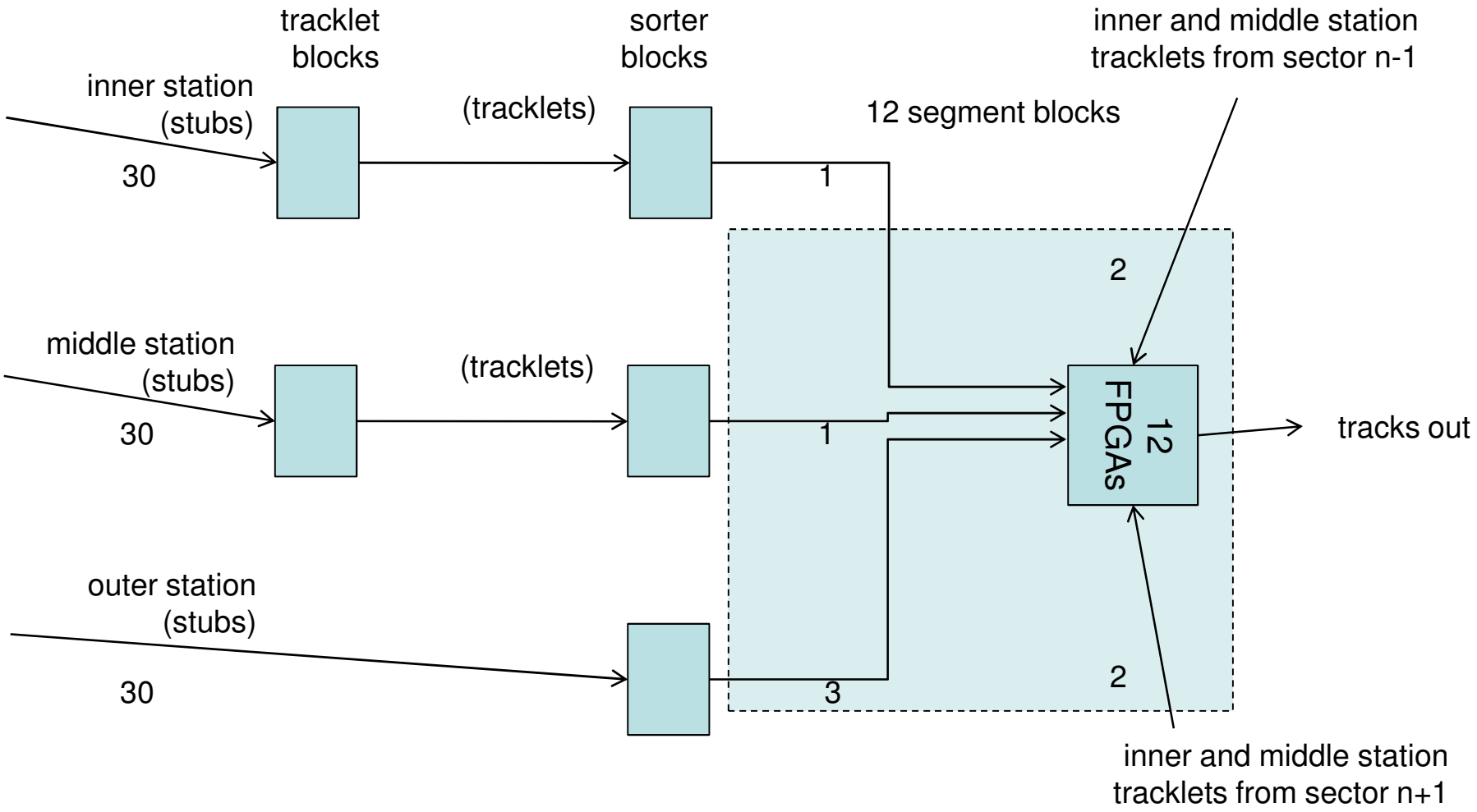


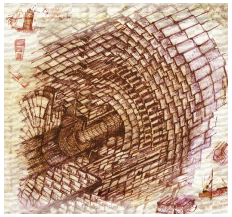
Repeat for Middle Layer

- Missing stack in middle layer eliminates middle layer tracklet
- Middle layer segmentation can use the stub
  - Recover half the information in the layer
- Do the same for the inner layer
- Must remove duplicates



Sector Processor Sketch

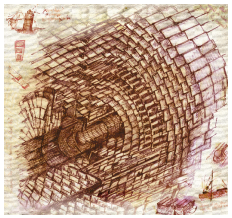




pipeline stages in tracklet block

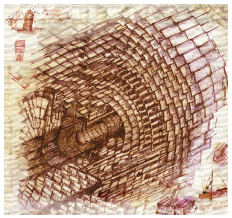
- (1) load stub data from sensors
- (2) form tracklets from stubs
- (3) sort tracklets by destination segment
- (4) transfer to segment processor
- (5) receive tracklet data from 3 stations
- (6) find tracks
- (7) check z consistency
- (8) transfer tracks to duplicate eliminator
- (9) receive track data from all 3 layers
- (10) compare inputs, eliminate duplicates
- (11) send track data to L1 trigger

  - ≈11 total pipe line stages for system
  - < 1 μs



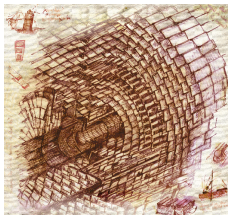
Robust Design

- **Finds tracks:**
  - **With tracklets in all 3 layers**
  - **With tracklets in 2 layers + 0 or 1 stub**
  - **With tracklets in 1 layer plus 0, 1 or 2 stubs**
- **Found Tracks tagged with tracklet info.**
  - **Specific trigger could require minimum number of tracklets and/or stubs**



Summary

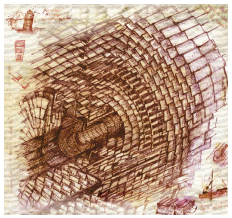
- Tracklets allow layer segmentation so can do track finding in an FPGA
- Multiple layers create a robust design
- Simultaneous track finding in all 3 double-stack layers allows use of track stubs providing that there is at least one tracklet



Summary and Conclusions Part b

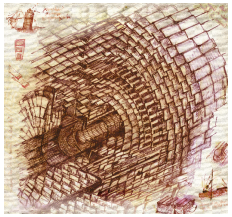
- **Most of the activity is focused on layouts which deploy layers of Stacked Modules**
  - **But work continues to evaluate possible alternatives**
    - **Cluster width, Strip Pt modules, etc.**

- **We make good progress on developing possible architectures for building L1 Trigger Track primitives**
  - **Off-detector Tracking Trigger architecture is closely coupled to basic features of layout**
    - **Present ideas make use of "local" Tracklet formation in r-phi hermetic sectors of double-stack layers**

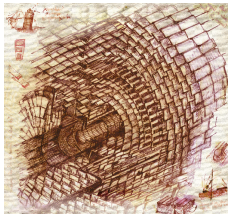


Summary and Conclusions Part b

- **Low Pt threshold ~ 2.5GeV, required for isolation, determines the data rates from FE chips / modules to USC**
  - **Material and Power associated to high bandwidth data transmission**
    - **Material in Tracker has adverse effect on performance…**
  - **Size and complexity of Off-detector Tracking Trigger system**
- **Need to evaluate pros and cons of Tracker isolation in the L1 Trigger**

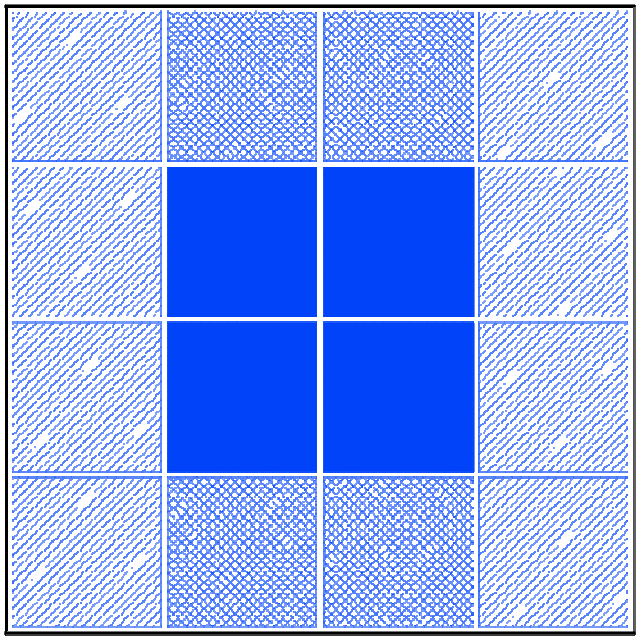


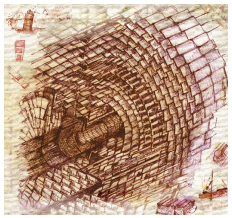
Back-up Slides



- **Communication from stack to outside world is difficult**
- **100 mm by 100 mm sensors requires 16 chips**
  - **set by reticle size**
- **The 4 inner chips have no exposed edge**
- **Central top and bottom conflict with adjacent sensors**
- **Also need chip to chip link for track finding**

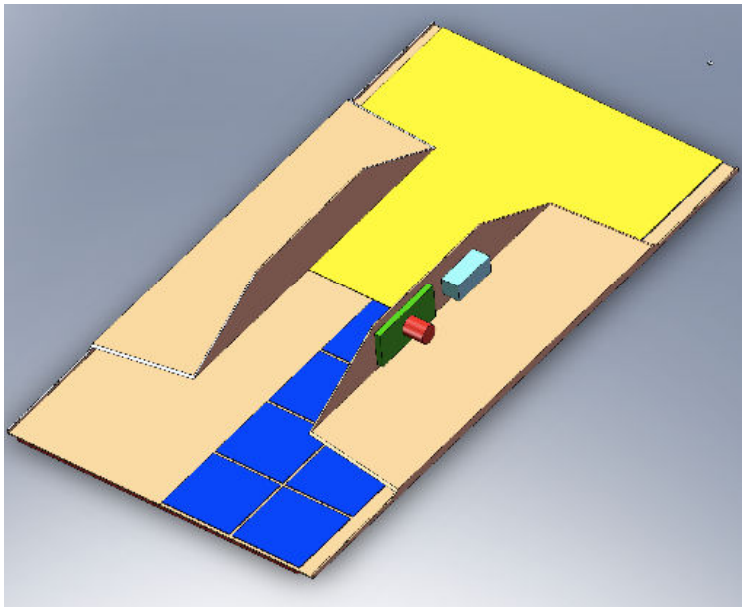
100 by 100 mm sensor with 16 chips



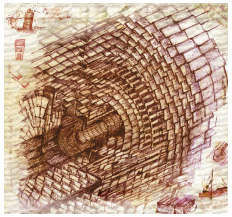


Yellow block is one sensor
Blue is read out chip
Tan is Kapton buss

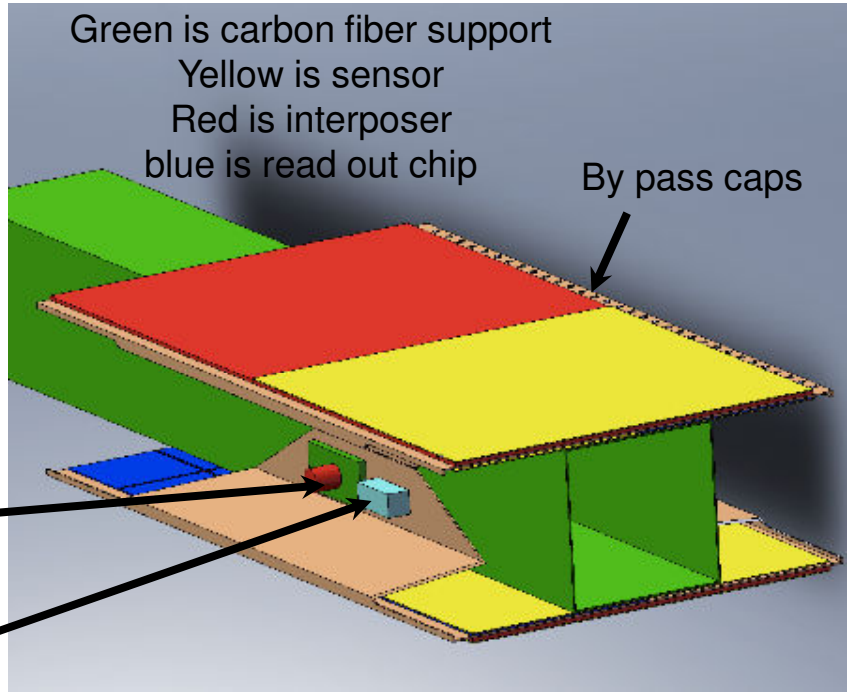
- **Divide buss in center of sensor**
  - **Readout half buss on either side of sensor**
    - short path for bypass capacitors and buss
- **Max rate is 8 tracks per crossing**
  - **20 bits/track =>6.4 GB/s**
  - **1 fiber per sensor**
  - **read out 2 half sensors/fiber**



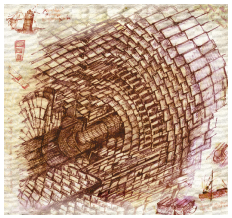
Green+red is DC-DC converter
Light blue is fiber driver



- **Don't need full bandwidth over entire rod**
  - **Rate drops by half at half distance from IP in inner layer**
- **Design optic chip with 4 inputs**
  - **use one chip to read 4 half sensors in outer part of inner layer**
  - **one chip per 8 half sensors in outer layers**
    - **Connector through carbon fiber rod**
  - **Minimizes mass**



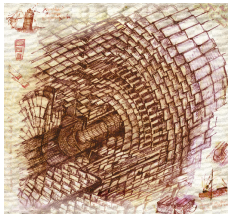
Tan is Kapton buss
green-red is DC-DC
blue is fiber driver



Some Reference Occupancy Estimates

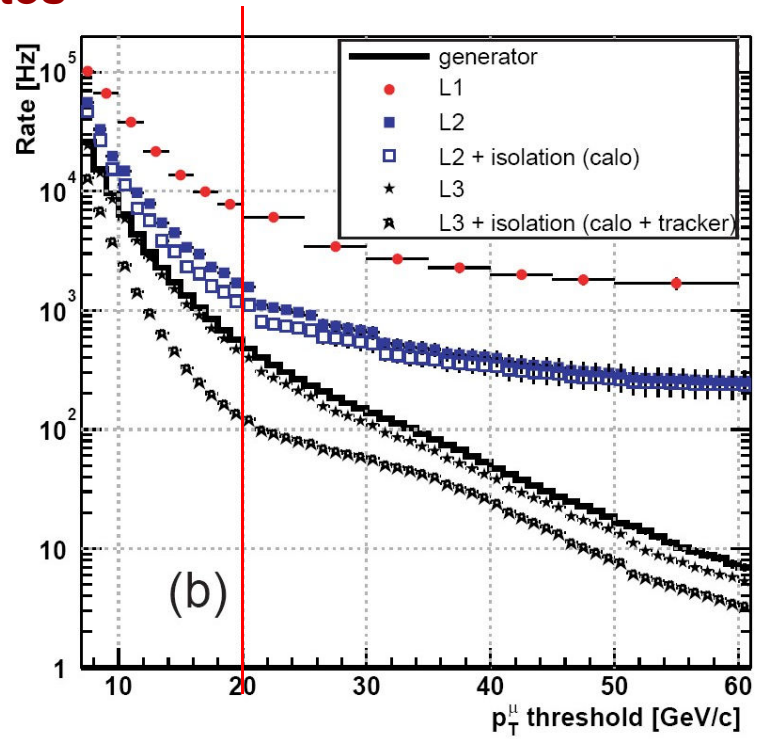
- **Hit Occupancies estimated for the present CMS Strip Tracker, with full Simulation at LHC Luminosity = 10^{34}, extrapolated to SLHC Luminosity = 10^{35}**
  - **Geoff Hall, compilation of results from Ian Tomalin at LHC:**
    - Strip Occupancy ~ 120MHz / cm^2 at R = 25cm
    - Strip Occupancy ~ 80MHz / cm^2 at R = 34cm
    - Strip Occupancy ~ 40MHz / cm^2 at R = 50cm
    - Strip Occupancy ~ 20MHz / cm^2 at R = 60cm

- **These are occupancies for un-clustered hits above threshold**
  - **Need to check exact definition…**

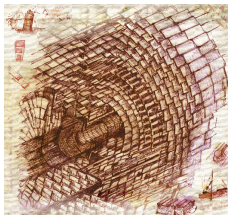


Required Functionality
L1 Trigger

- **Confirmation of Isolated High-pt μ Candidates**
  - Fast, Efficient & Clean Tracking
  - Excellent Pt resolution
  - Isolation
- **Separation of e/γ Candidates**
  - Match with Track (nb conversions…)
  - Isolation
- **Tau Jet trigger**
  - Low Multiplicity, Isolation
- **MET ?**
  - Clean up High Pile-up environment
- **Rejection of Uncorrelated Combinations, from different primary vertex**
  - Match with Tracks at Vertex required for Isolation…

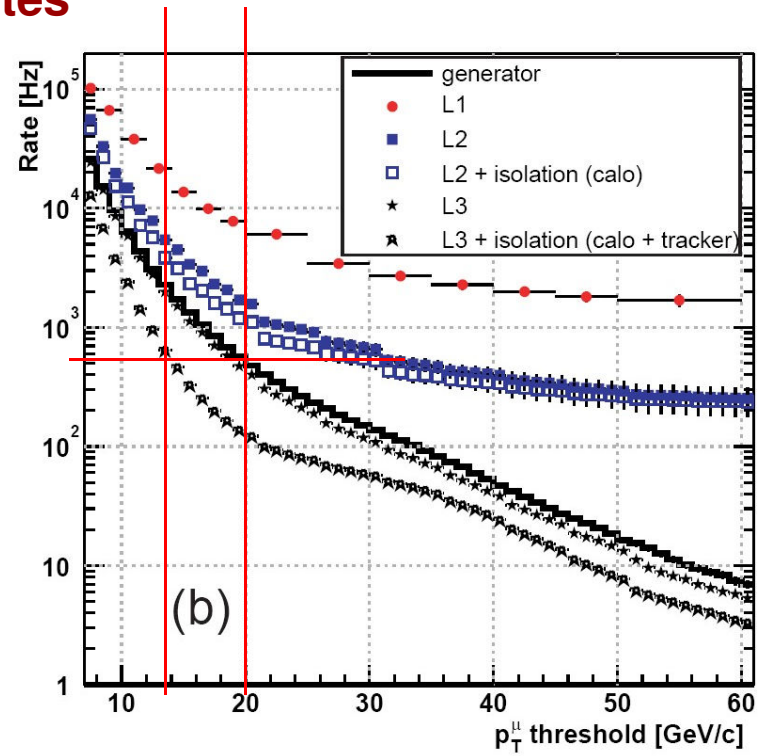


Factor ~ 100 reduction
For same Pt threshold

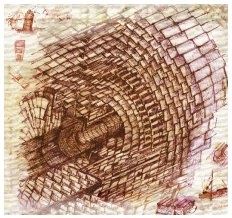


Required Functionality
L1 Trigger

- **Confirmation of Isolated High-pt μ Candidates**
  - **Fast, Efficient & Clean Tracking**
    - High signal efficiency
  - **Excellent Pt resolution**
    - Need sharp threshold cut in 15~25GeV range
  - **Isolation: reduce Pt cut for given rate**
    - ~ 6kHz muon rate for Pt > 20GeV
    - ~ 6kHz muon rate for Pt > 14GeV & Isolation
- **Rejection of Uncorrelated Combinations, from different primary vertex ?**
  - **Match with Tracks at Vertex**
    - Required to avoid false veto with Isolation



Factor ~ 100 reduction
For same Pt threshold

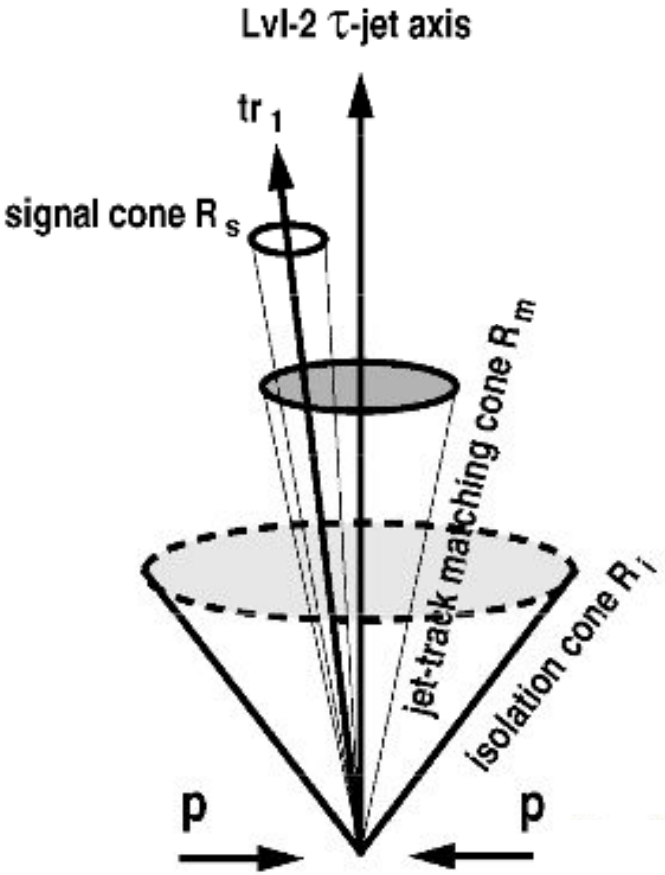


Required Functionality
L1 Trigger

- **Confirmation of High Pt Track Candidates**
  - Tracks with Pt above 15 ~ 20 GeV
  - Excellent Efficiency
  - Reasonable Pt resolution

- **Isolation**
  - Tracks with Pt above ~ 2 GeV
  - Low fake rate to avoid false veto
  - Good Efficiency

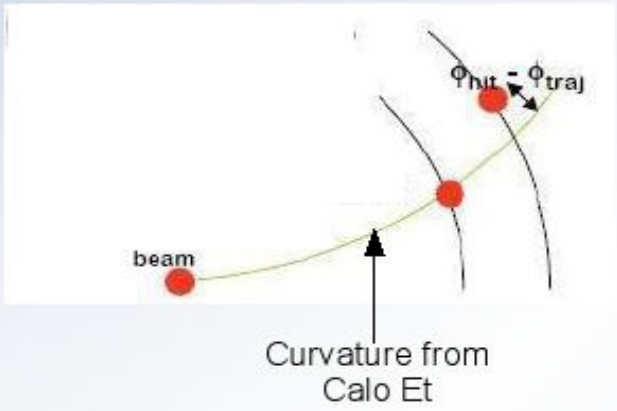
- **Longitudinal Vertex association**
  - Tracks with Pt above ~ 2 GeV
  - Good Z Vertex resolution

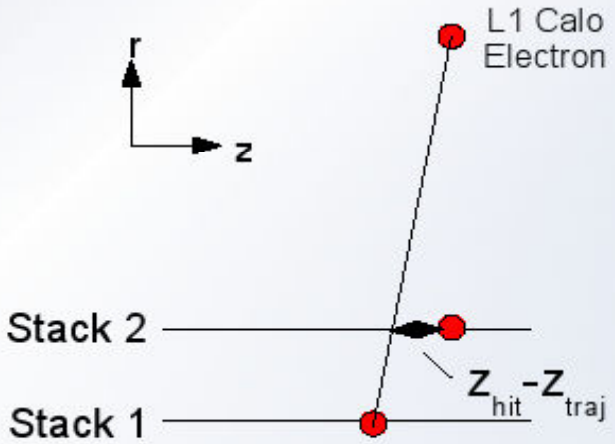


Status of Electron Trigger Objects Generation
Imperial College, Cornell

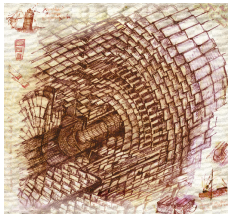
Electron Triggering Studies

- **Second Step:** identify **pairs** of hits consistent with cluster





- Hit pairs ("seeds") are identified through two variables
  - $\Phi_{miss} = |\varphi_{hit} - \varphi_{traj}|$
  - $z_{miss} = |z_{hit} - z_{traj}|$



little to be gained given the low inclusive muon threshold. The corresponding trigger table for high luminosity is listed in Table 15-2. In both cases, a 1 kHz bandwidth is allocated to minimum-bias events which will be used for calibration and monitoring purposes.

Table 15-1 Level-1 Trigger table at low luminosity. Thresholds correspond to values with 95% efficiency.

Trigger	Threshold (GeV or GeV/c)	Rate (kHz)	Cumulative Rate (kHz)
Inclusive isolated electron/photon	29	3.3	3.3
Di-electrons/di-photons	17	1.3	4.3
Inclusive isolated muon	14	2.7	7.0
Di-muons	3	0.9	7.9
Single tau-jet trigger	86	2.2	10.1
Two tau-jets	59	1.0	10.9
1-jet, 3-jets, 4-jets	177, 86, 70	3.0	12.5
Jet * E_T^{miss}	88 * 46	2.3	14.3
Electron * Jet	21 * 45	0.8	15.1
Minimum-bias (calibration)		0.9	16.0
TOTAL			**16.0**

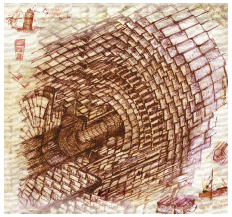


Table 15-2 Level-1 Trigger table at high luminosity. Thresholds listed correspond to values with 95% efficiency.

Trigger	Threshold (GeV or GeV/c)	Rate (kHz)	Cumulative Rate (kHz)
Inclusive isolated electron/photon	34	6.5	6.5
Di-electrons/di-photons	19	3.3	9.4
Inclusive isolated muon	20	6.2	15.6
Di-muons	5	1.7	17.3
Single tau-jet trigger	101	5.3	22.6
Two tau-jets	67	3.6	25.0
1-jet, 3-jets, 4-jets	250, 110, 95	3.0	26.7
Jet * E_t^{miss}	113 * 70	4.5	30.4
Electron * Jet	25 * 52	1.3	31.7
Muon * Jet	15 * 40	0.8	32.5
Minimum-bias (calibration)		1.0	33.5
TOTAL			**33.5**