Pixel Jet Trigger Studies

CMS Upgrade Workshop

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Background

- Trigger capability designed into the PSI46 readout chip
  – Hit double column and cluster mutliplicities
- Capabilities and performance studies described in Marlon Barbero’s thesis.

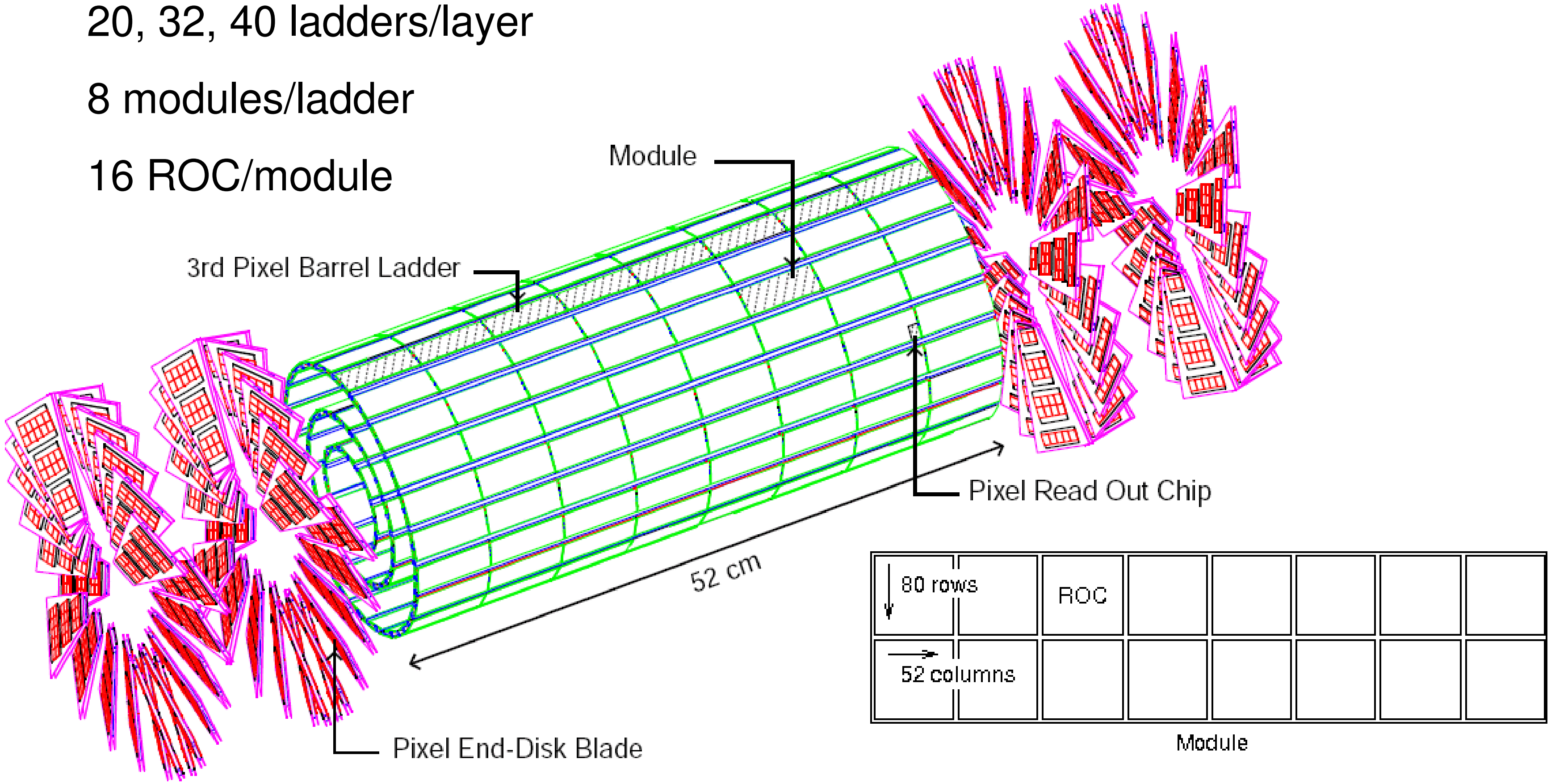
Detector/Readout Geometry

3 layers

20, 32, 40 ladders/layer

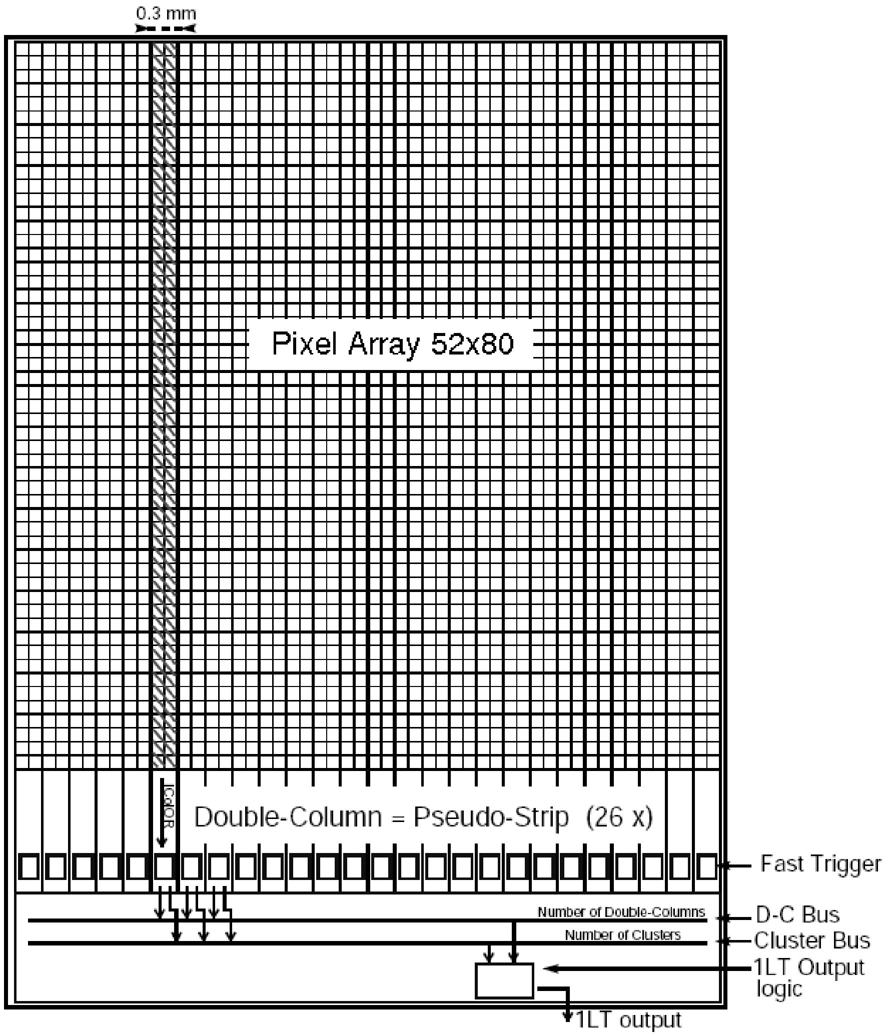
8 modules/ladder

16 ROC/module



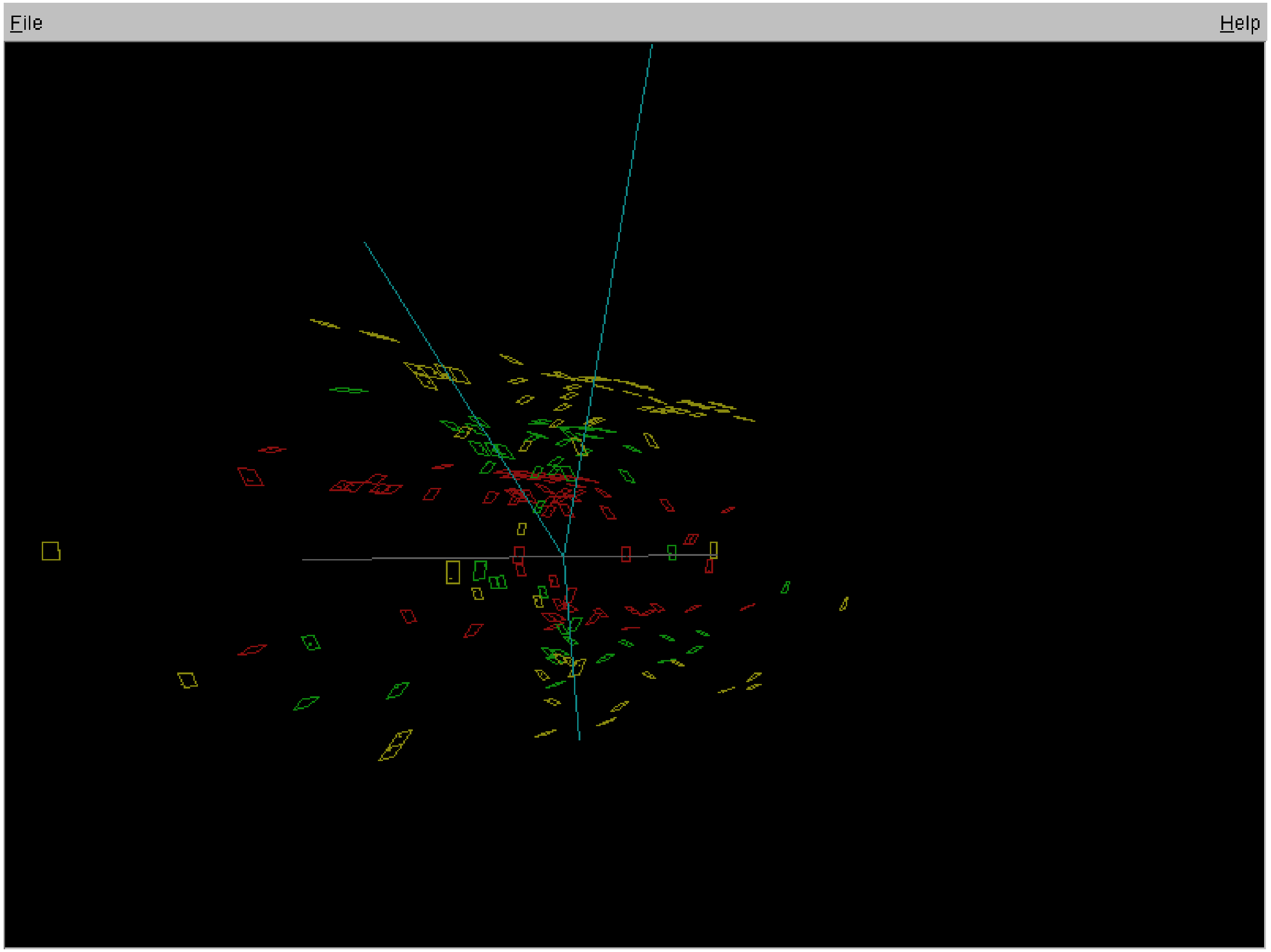
Pixel unit cell: 150x100 μm

Trigger Primitives at the ROC level



- A *hit double-column* is counted if the pixel hit multiplicity exceeds a specified threshold.
- *Cluster*: non-adjacent groups of hit double columns
- L1 trigger output based on:
  - Σ Double-columns
  - Σ Clusters

Pixel Jet Trigger Motivation



Pixel Jet Trigger Issues

- Efficiency at ROC level
- 3-layer pattern generation (or 2-layer + z)
- η, φ, z resolution
- Jet identification efficiency
- Trigger data bandwidth
- Implementation in hardware
- Trigger decision latency
- Interface with calorimeter trigger

Pixel Trigger Model

- Event samples:
  - /RelValQCD_FlatPt_15_3000/CMSSW_3_1_2-MC_31X_V3-v1/GEN-SIM-DIGI-RAW-HLTDEBUG
  - /RelValMinBias/CMSSW_3_1_2-MC31X_V3-v1/GEN-SIM-DIGI-RAW-HLTDEBUG
- Pixel geometry written to a file – read back to define the geometry in the model.
- Pixel DIGI hits written to a file – read back as input to trigger emulation.
  - Multiple min-bias events randomly overlaid with a physics process of interest (ie, high p_T jets)
- Emulation of ROC trigger primitives.

ROC Trigger Cuts

- Define “signal” as a ROC that lies along a jet axis, where jet $p_T > 250$ GeV/c.
- Define “background” as any ROC in an event with N_{mb} min-bias events overlaid.
- Examples:
  - Double-column hit multiplicity
  - Hit D-C multiplicity, Σ Double-columns
  - Cluster multiplicity, Σ Clusters

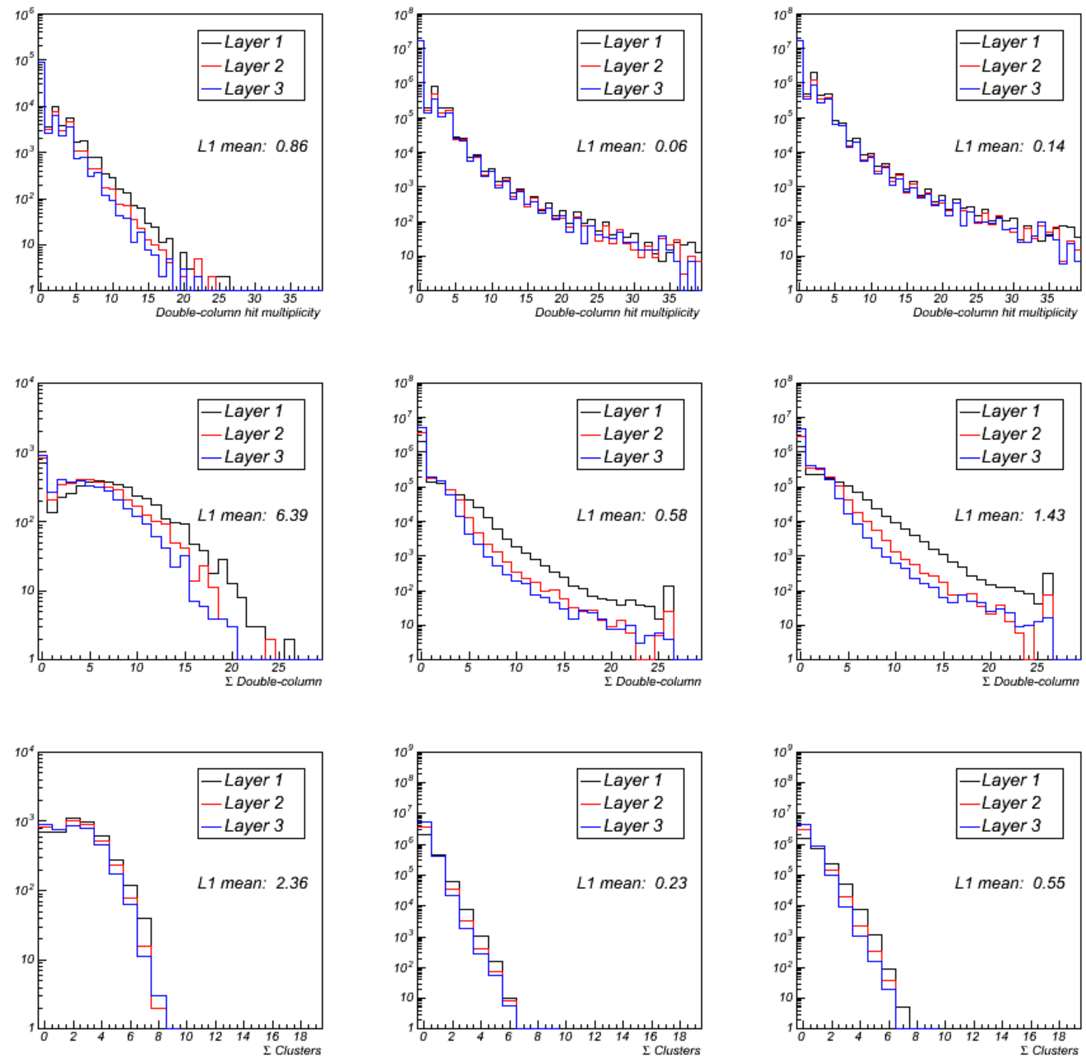
ROC Trigger Primitives

Jets | 20 min-bias | 50 min-bias

Double-column hit multiplicity

Σ Double-columns

Σ Clusters

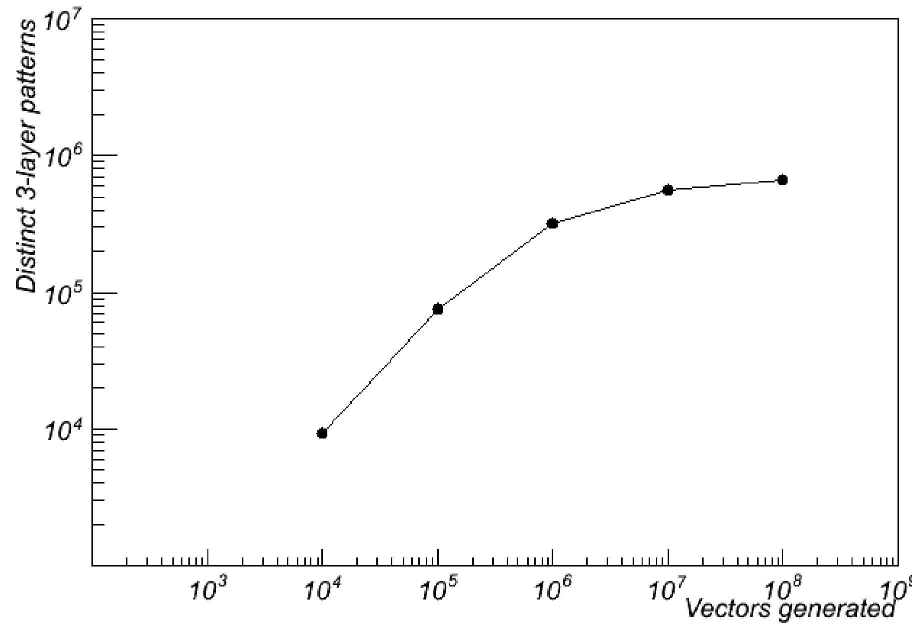


Pattern Generation

- Identify which ROC's line up, pointing back to the beam axis
  - Uniform vertex position, $-16 < z < 16$ cm
  - Uniform in azimuth, $0 < \varphi < 2\pi$
  - Uniform in pseudorapidity, $-2 < \eta < 2$
- Extrapolate vectors through pixel detector geometry model.
- Hit ROC is one through which the vector extrapolates.
- Worst case: no clustering of hit ROC's in trigger.

Pattern Generation (worst case)

- Extrapolate 10^8 vectors in ~5 min.
- More or less complete coverage.
- ROC usage in patterns by layer:



$$N = 2249 \times 47.8 \times 6.1 = 661494$$

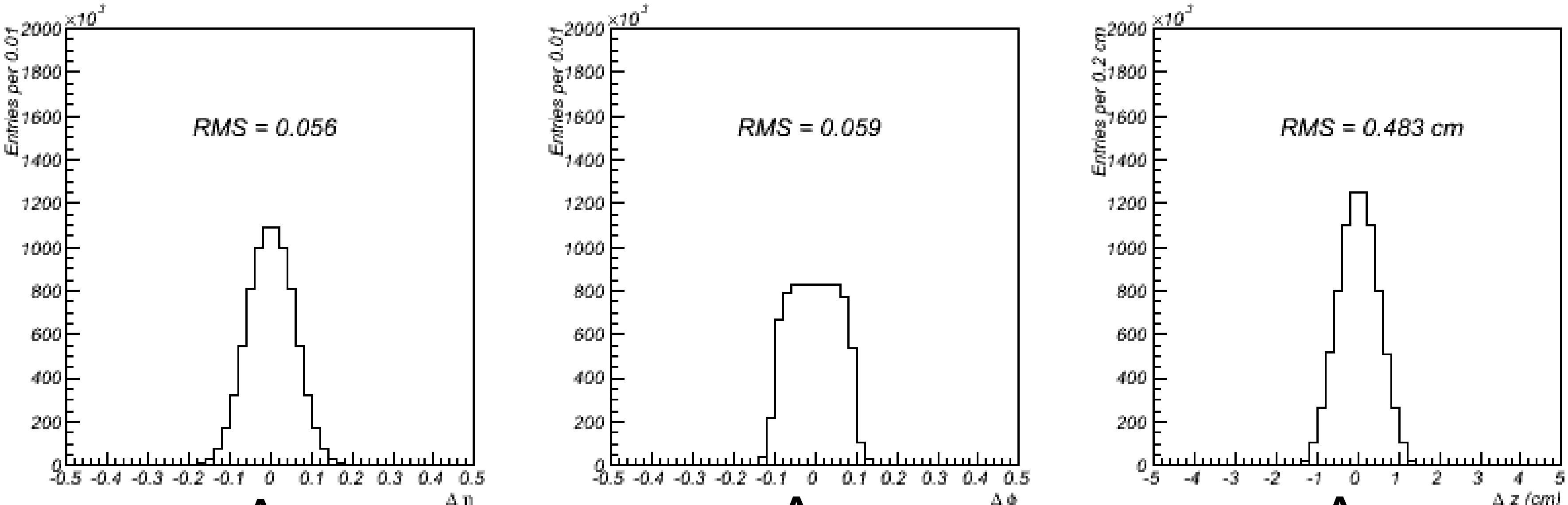
Compare with 2560 ROC's in Lyaer 1

For each Layer 1 ROC there are about 48 distinct patterns

For each pair of Layer 1 and Layer 2 ROC's, there are about 6 distinct patterns

Intrinsic Jet Parameter Resolution

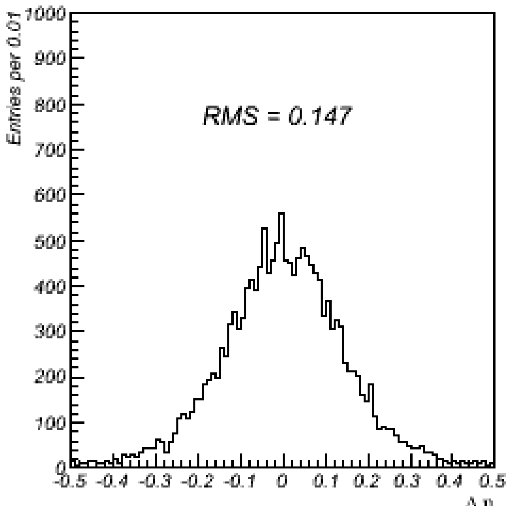
- Map each pattern into space of (η,φ,z) using 5 bits for each.
- Generate more vectors, compare parameters from matched pattern with generated parameters.
- Generated 10^7 vectors, observed 0.7% inefficiency.



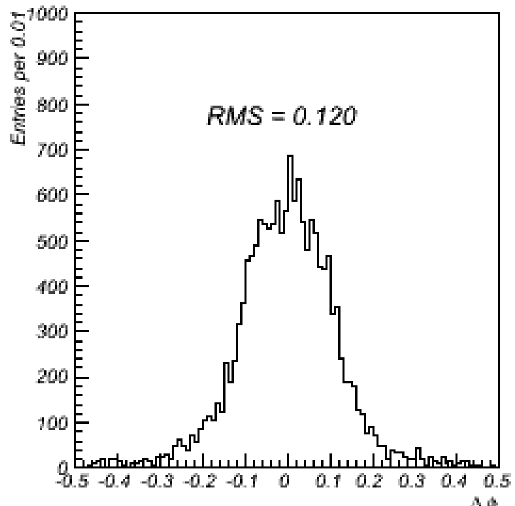
Δη Δφ Δz

Actual Jet Parameter Resolution

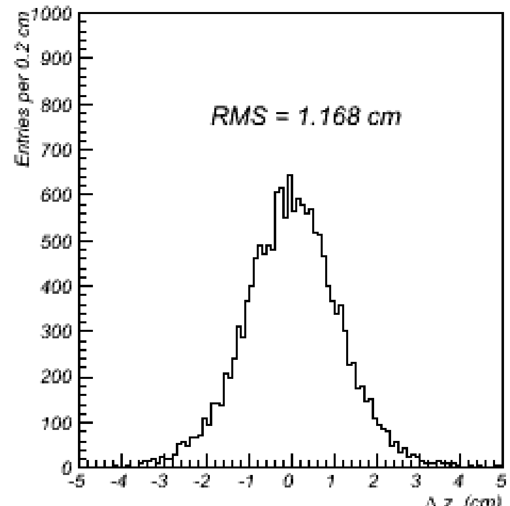
- Reconstruct jets (sisCone5GenJets), use p_T>250 GeV/c
- Low trigger thresholds:
  - Σ Double-columns ≥ 2
  - Σ Clusters ≥ 2
- Match in ($\Delta\eta$, $\Delta\varphi$) – look at Δz (+ cyclic permutations)



$\Delta\eta$



$\Delta\varphi$

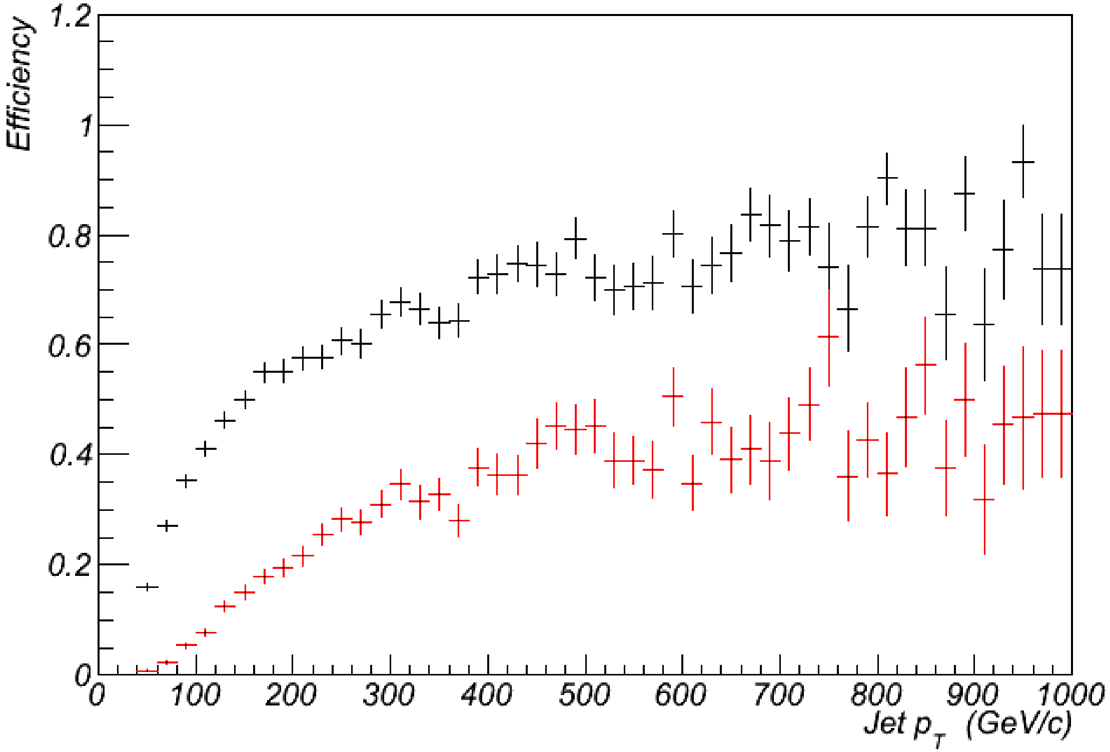


Δz

Jet Identification Efficiency

- Require jets match Δη, Δφ, Δz within ±2σ.

Similar to results in Marlon's thesis – eg. Figure 3.8.



Σ Double-columns ≥ 2
Σ Clusters ≥ 2

Σ Double-columns ≥ 3
Σ Clusters ≥ 3

- But the parameter space that can be optimized is very large...

Data Rates

- ~~Four~~ Three possible schemes:
  - Synchronous (all data every 25 ns) or zero-suppressed (only data from triggered ROC's).
  - Trigger on individual ROC's or from clusters of adjacent ROC's.
- Available bandwidth:
  - Assume 192 fibers for trigger (64 ROC/fiber)
  - Assume 320 MHz (8 bits/bunch crossing)?

⇨ Can't send synchronous data from all ROC's.

Data Rates

- Synchronous data each bunch crossing requires combining trigger data from ½ a module into 1 bit – *granularity too coarse*.
- Consider sending addresses of triggered ROC's or groups of ROC's:
  - Include bunch crossing identifier
  - List could be long for interesting events
  - Should very short for min-bias events
  - Min-bias events determine the *average bandwidth*.

Data Rates

- Data rate determined by packet size and the rate of hit ROC's.
  - Example: 18 bits to send $ROC_{addr1}/ROC_{addr2}/t_1 x\ t_2$
- Simulate by superimposing multiple min-bias events.
- Avg # of triggered ROC's / half ladder / event,
  (Loose cuts: Σ Double-columns ≥ 2, Σ clusters ≥ 2):

N_{mb}	1	20	50	100
Layer 1	0.030	1.777	7.321	18.42
Layer 2	0.011	0.595	2.689	8.068
Layer 3	0.005	0.273	1.224	3.897

(10^{34} $cm^{-2}s^{-1}$ = 19.2 min-bias events per bunch crossing)

Data Rates

- Rates can be controlled by tighter cuts on inner layers, but will incur a loss of efficiency.
- For example, a “high luminosity” scenario:
  - Layer 1: Σ Double-columns ≥ 8, Σ clusters ≥ 4
  - Layers 2 & 3: Σ Double-columns ≥ 4, Σ clusters ≥ 3
- Avg # of triggered ROC’s / half ladder / event:

N_{mb}	1	20	50	100
Layer 1	0.00265	0.145	1.048	4.450
Layer 2	0.00084	0.034	0.207	0.980
Layer 3	0.00059	0.017	0.079	0.357

- Motivates prioritizing trigger data.
- More realistic projections need to be tied to the actual hardware implementation.

Physical Implementation

- ROC trigger output:
  - Differential analog output: `Trig_out+/Trig_out-`
  - Analog coded ΣClusters or High Double Column Multiplicity
- Combination of ΣClusters from adjacent ROC’s important for jet identification efficiency.
- Motivates the functionality provided by a Module Trigger Chip
- Combine trigger information from 4 modules and drive on one fiber (“Side Trigger Control Chip”)

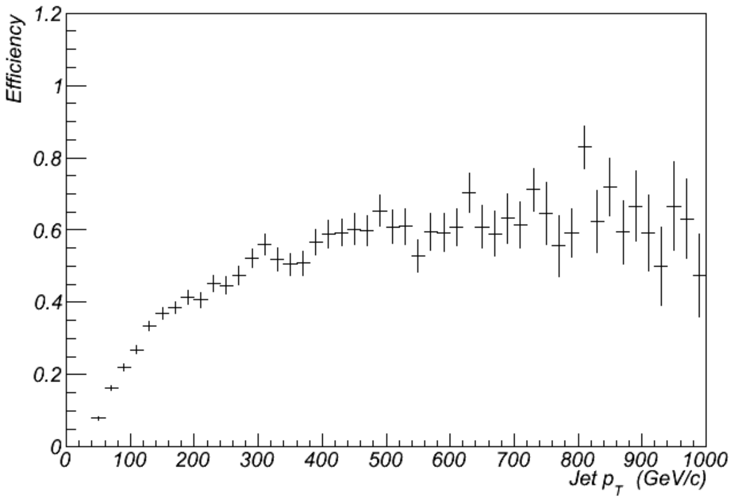
One Possible Scenario

- Module level clustering:
  - Sum the ΣClusters from 6 adjacent ROC's
  - Cut on ΣClusters in central ROC and in central + adjacent ROC's
  - Transmit central ROC address to "Side Trigger Control Chip"
    - Pipeline depth/output latency?
    - Output bandwidth?

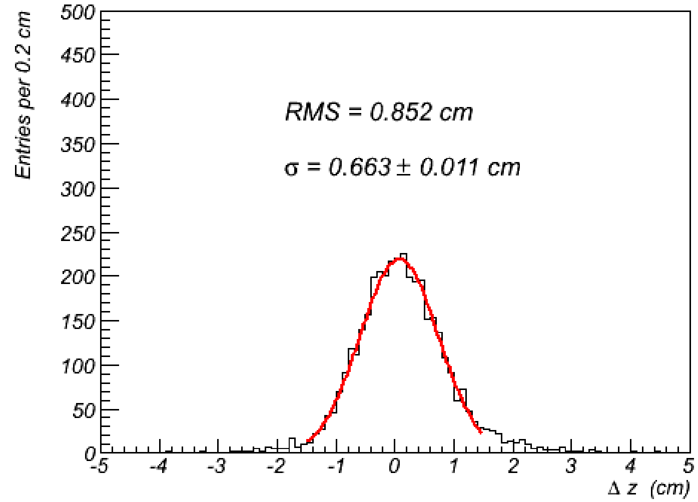
Example

- Cuts at ROC level:
  - High ΣDC multiplicity threshold = 4
  - ΣClusters ≥ 2
- Cuts at MTC level:
  - Output a single ROC address that has either:
    - High ΣDC multiplicity
    - Σclusters in ROC + adjacent 5 ROC's ≥ 3
- Bandwidth reduced by factor of 2
- Improved efficiency for tighter cuts
- Improved jet parameter resolution

Example with MTC



Efficiency



Z resolution, σ_z=0.7 cm

Number of MTC outputs per half ladder:

N_{mb}	1	20	50	100
Layer 1	0.097	1.999	3.584	3.963
Layer 2	0.013	0.495	1.921	3.423
Layer 3	0.0041	0.159	0.817	2.370
Matches/event	0.003	1.134	19.5	86.5

Observations

- Need to consider a nominal Phase 1 upgrade tracker geometry
- Need better estimates of link bandwidths
- Understand status of MTC + STCC
- Interface to calorimeter trigger
- Timing constraints
- Candidate firmware algorithms
- Testing/readout/monitoring interfaces

Summary

- Rapidly adapting to changing luminosity conditions is crucial
- The constraints already imposed by existing hardware designs are already very flexible.
- Emulation will continue to provide a realistic model of proposed hardware implementation.
- Need to focus on system level implementation, then return to performance studies.