Readout and DAQ for Micromegas

Guillaume Vouters

Plan

- **The HCAL Architecture**
- ASUs developed at LAPP for MICROMEGAS
  - ASU 8x32 with HARDROC v.1
  - ASU 32x48 with HARDROC v.2 for m²
  - ASU 8x8 with DIRAC v.1/DIRAC v.2
- DIF developments
  - Firmware for ASICs
  - Firmware for the CALICE DAQ

The HCAL Architecture

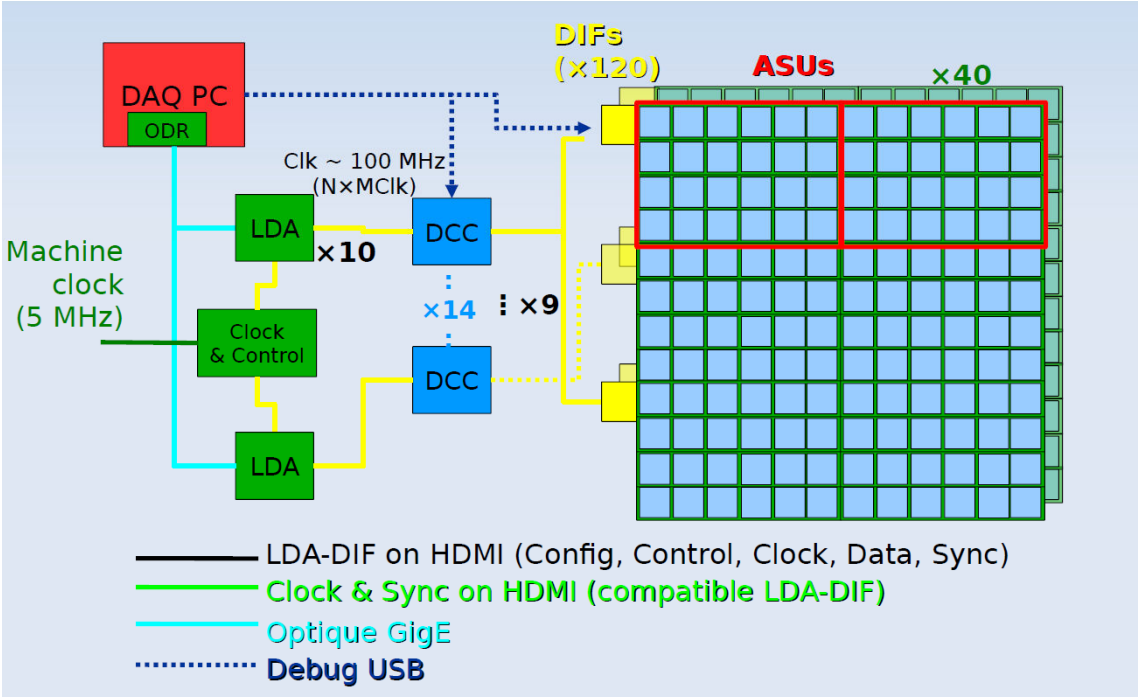
One cubic meter technological prototype :

→ 40 plans

→400 000 channels

→“Digital” Readout :
3 thresholds

→Power pulsing



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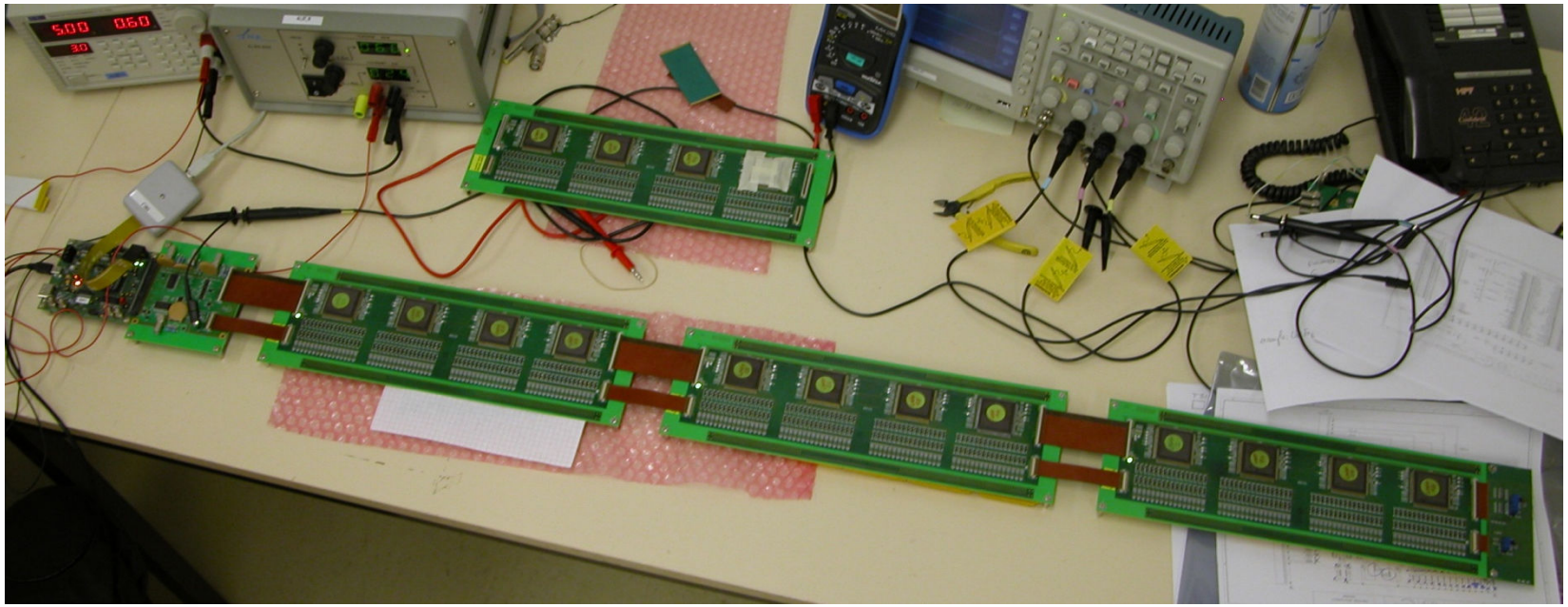
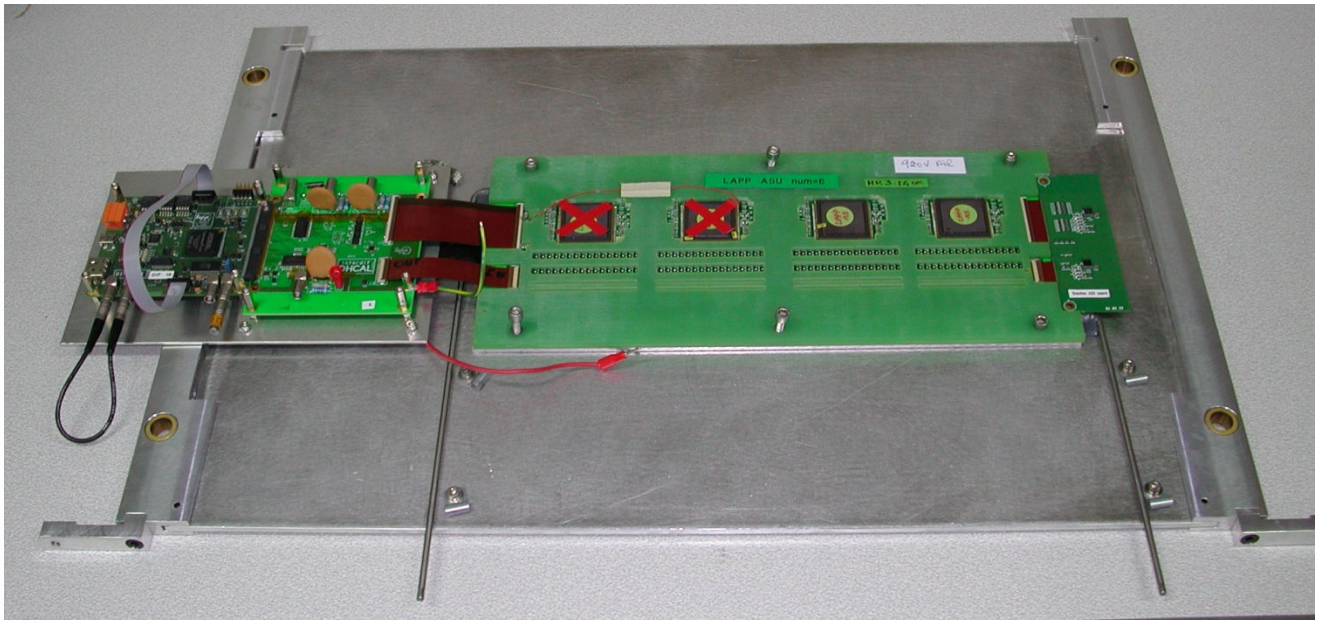
ASU 8x32 with HARDROC v.1



First we tried to communicate with our boards

→ We managed to control 12 HARDROCs v.1

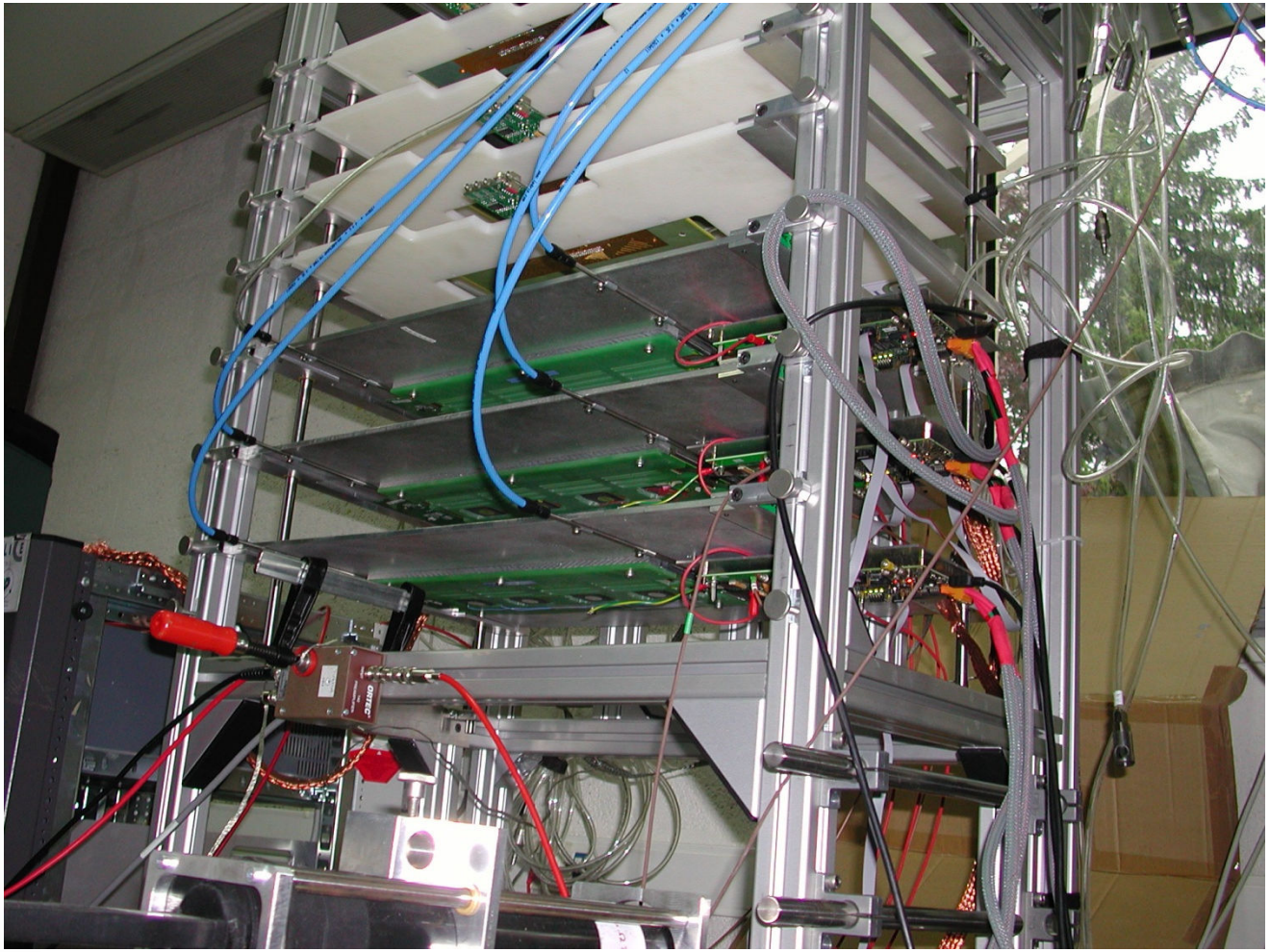
ASU 8x32 with HARDROC v.1



Then we built bulk MICROMEGAS

→We have now 4 detectors but there are only 11 HARDROCs v.1 still working

ASU 8x32 with HARDROC v.1



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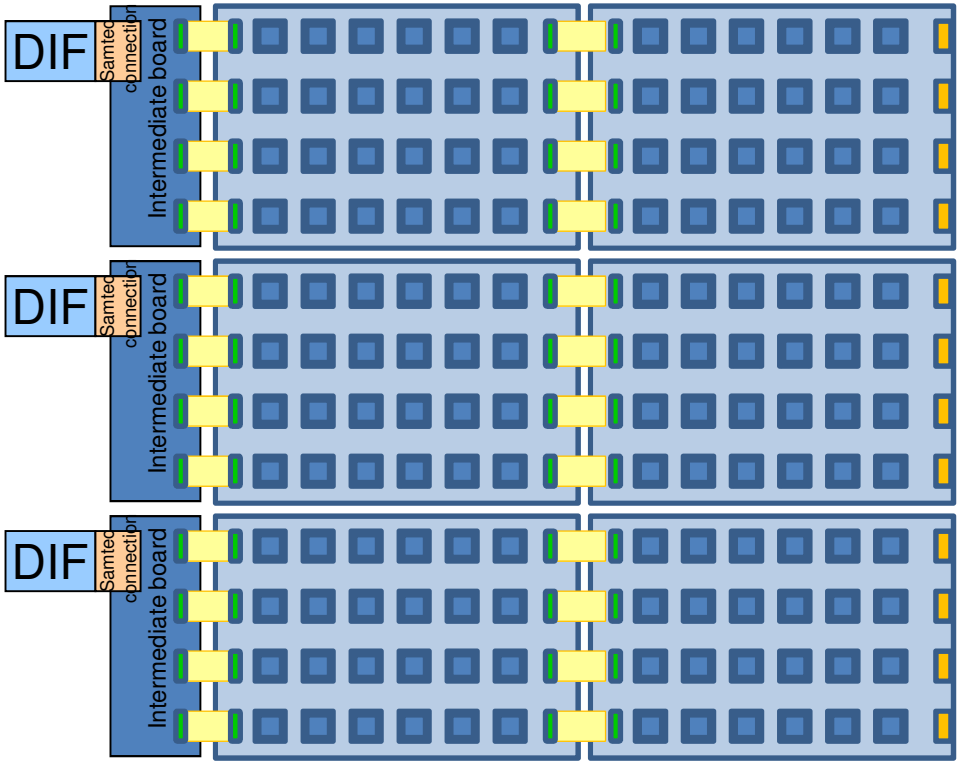
Architecture of the m²



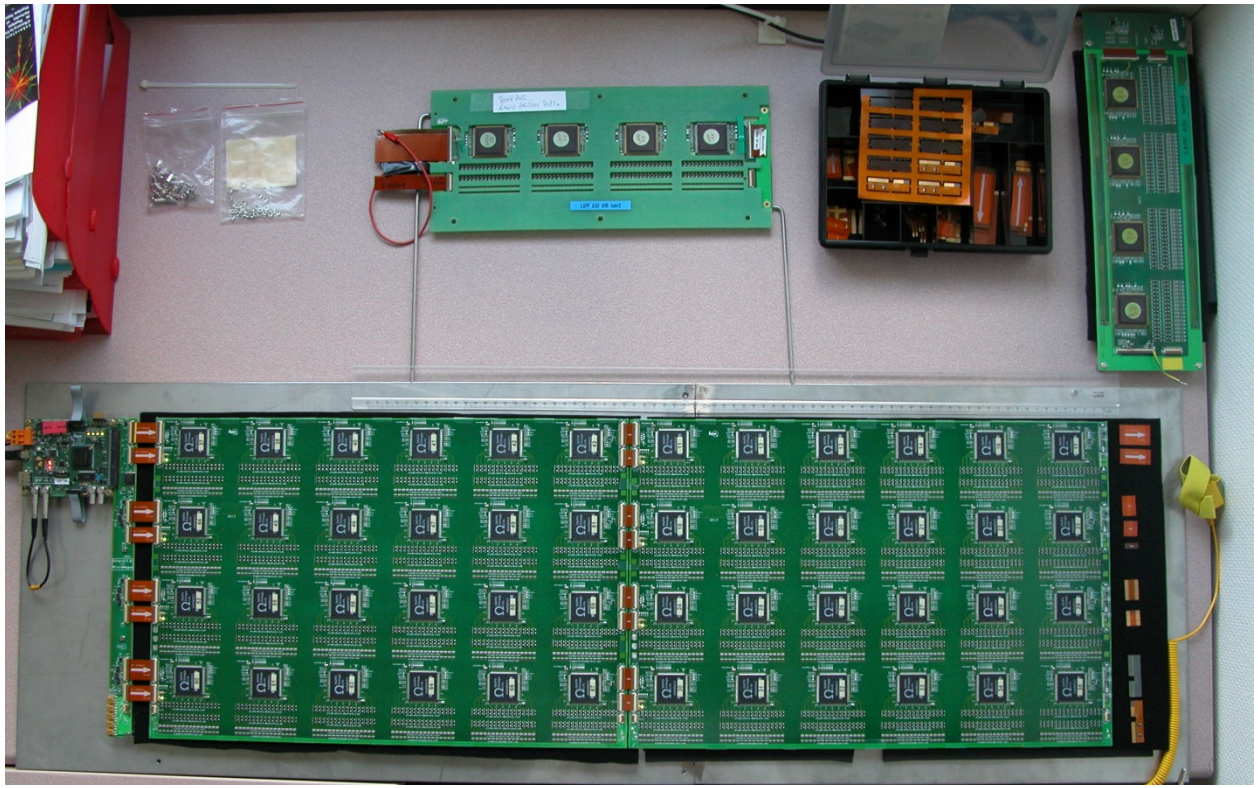
: Flat Printed Circuit

: ASIC chip (64 channels)

: Hirose connector

: Terminasion component

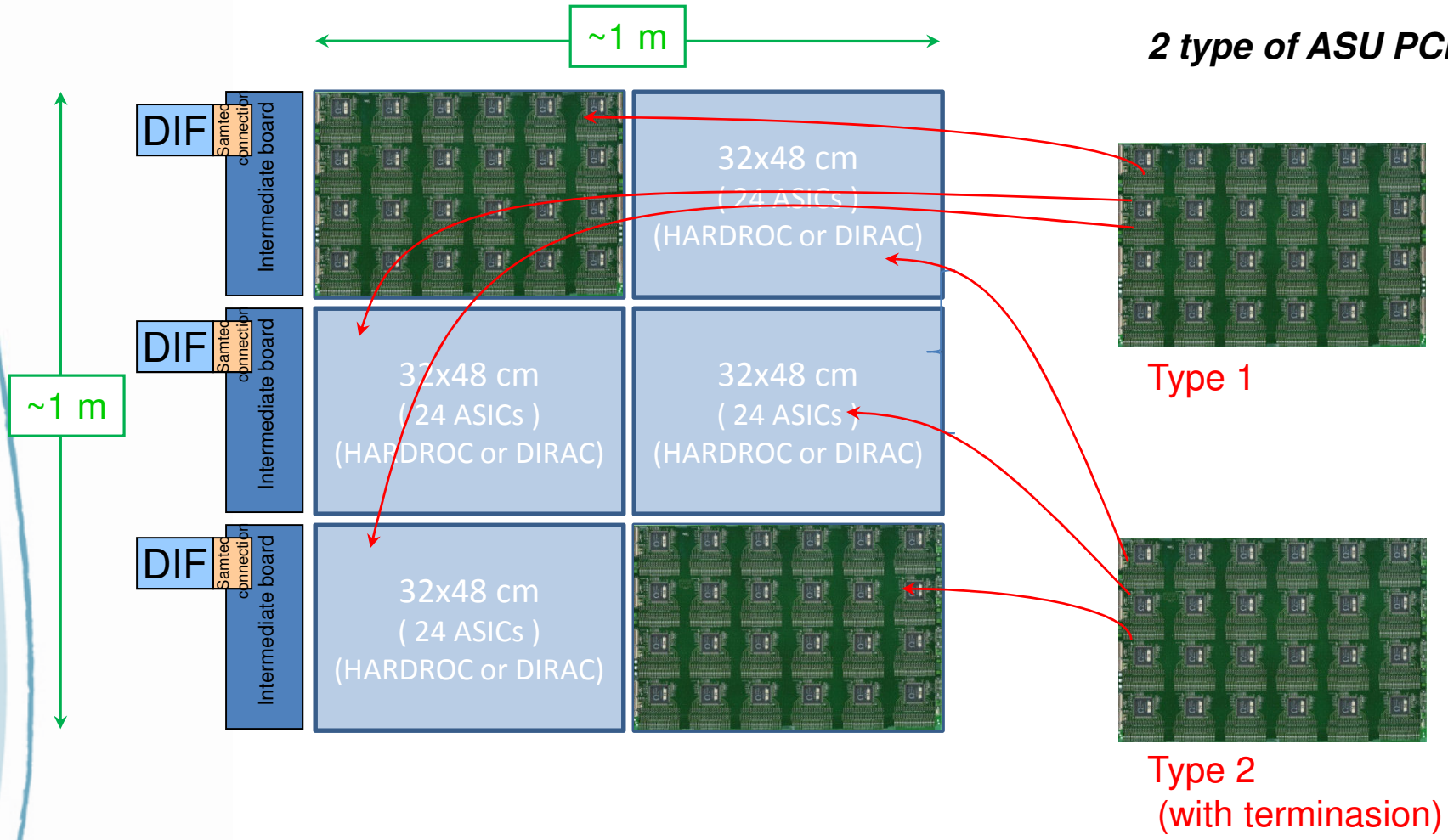
ASU 32x48 with HARDROC v.2



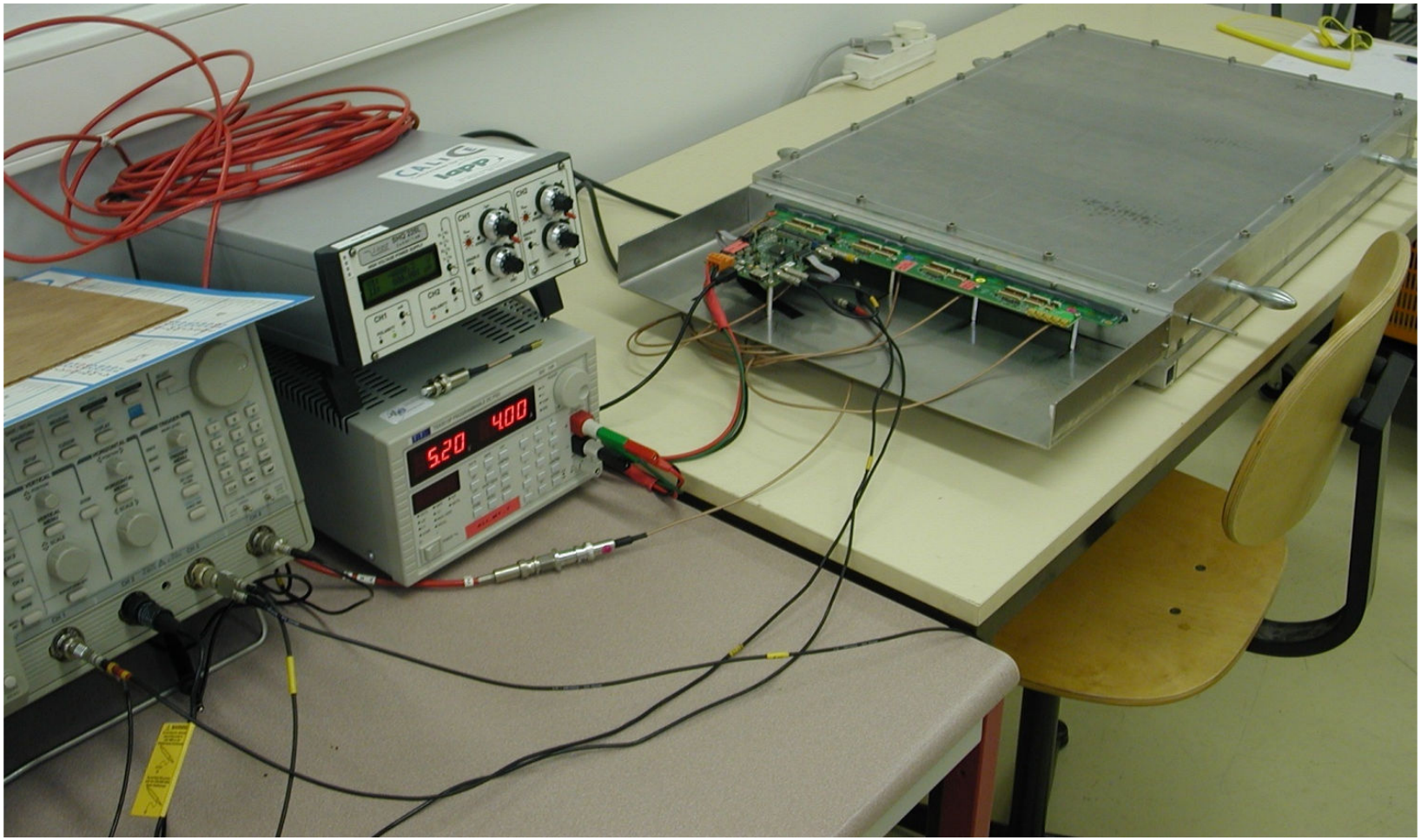
Here is a part of the square meter

→ We managed to control 48 HARDROCs v.2

MICROMEGAS m²



Test Box for ASU 32x48



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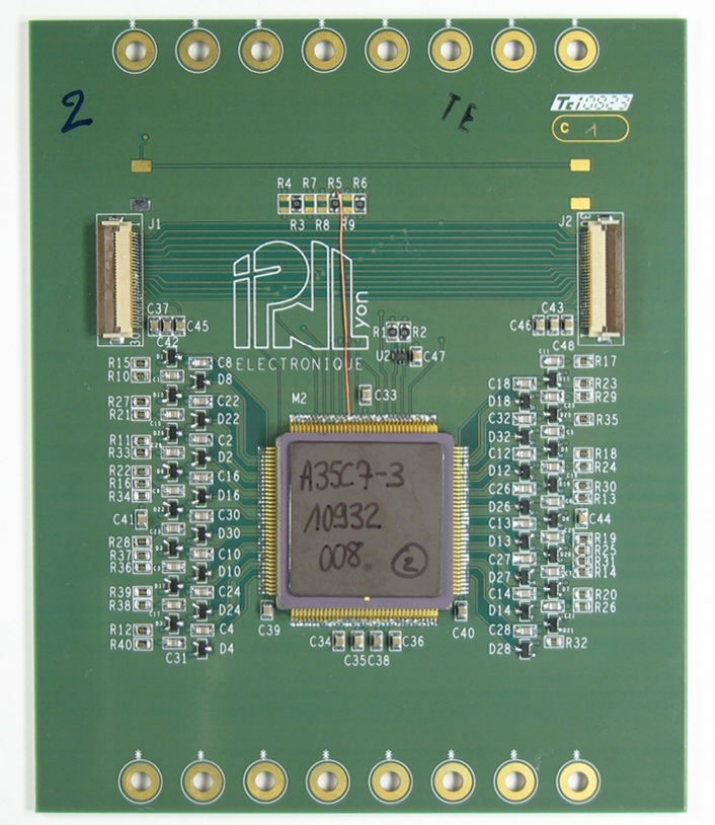
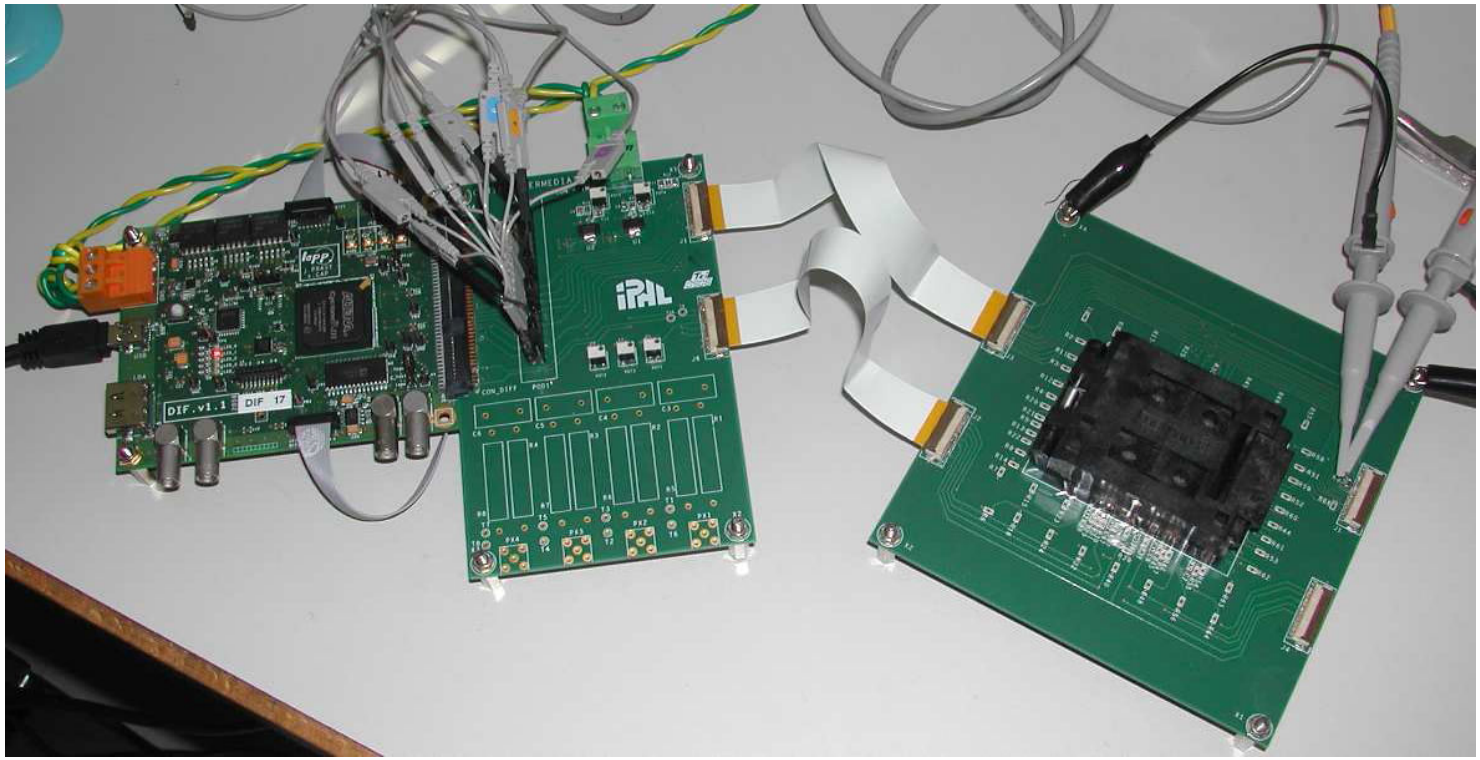
ASU 8x8 with DIRAC v.1

Dirac was initially developed at IPNL but now in tight collaboration with LAPP

First digital ASIC embedded on a bulk MICROMEGAS: tested successfully in 2008 beam test



ASU 8x8 with DIRAC v.2



Setup for DIRAC v.2 ASU

DIRAC v.2 was fully charactarized at LAPP

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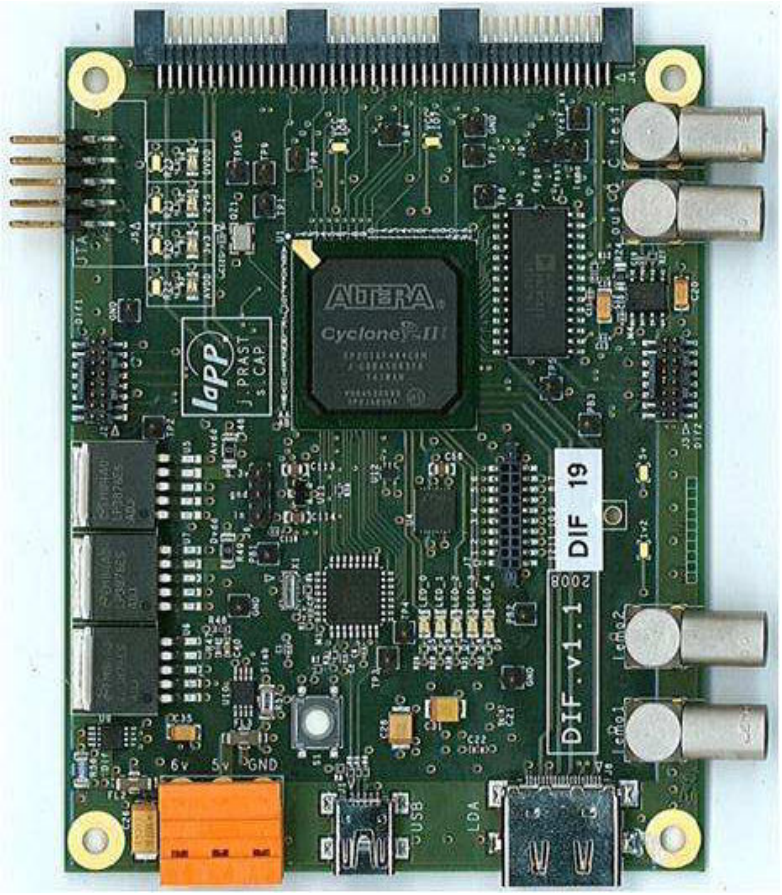
Detector InterFace developments

The DIF board is the first intermediate board between ASUs and DAQ

This DIF (see picture) has been developed at LAPP and has already been used in 2008 and 2009 for Eu-DHCAL MICROMEGAS and RPC beam tests

This DIF is also compatible with ECAL and AHCAL detectors



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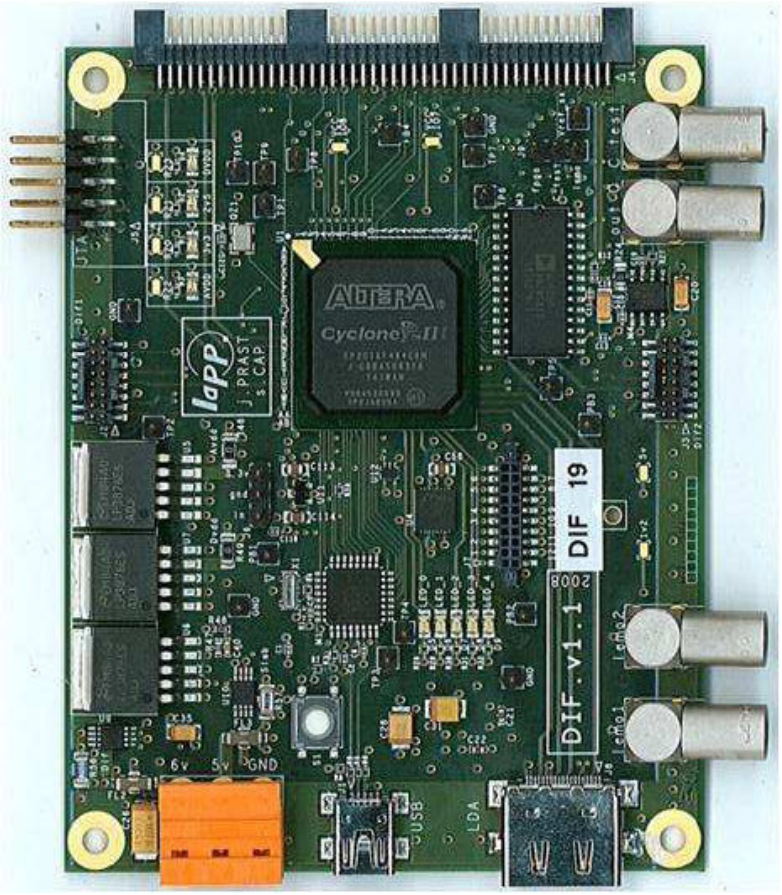
Detector InterFace developments

Firmware already existing for :

HARDROCs 1
used by LAPP (MICROMEGAS) and IPNL (RPC)

HARDROCs 2
used by LAPP (MICROMEGAS) and soon IPNL (RPC)

DIRAC 2
used by LAPP (MICROMEGAS)



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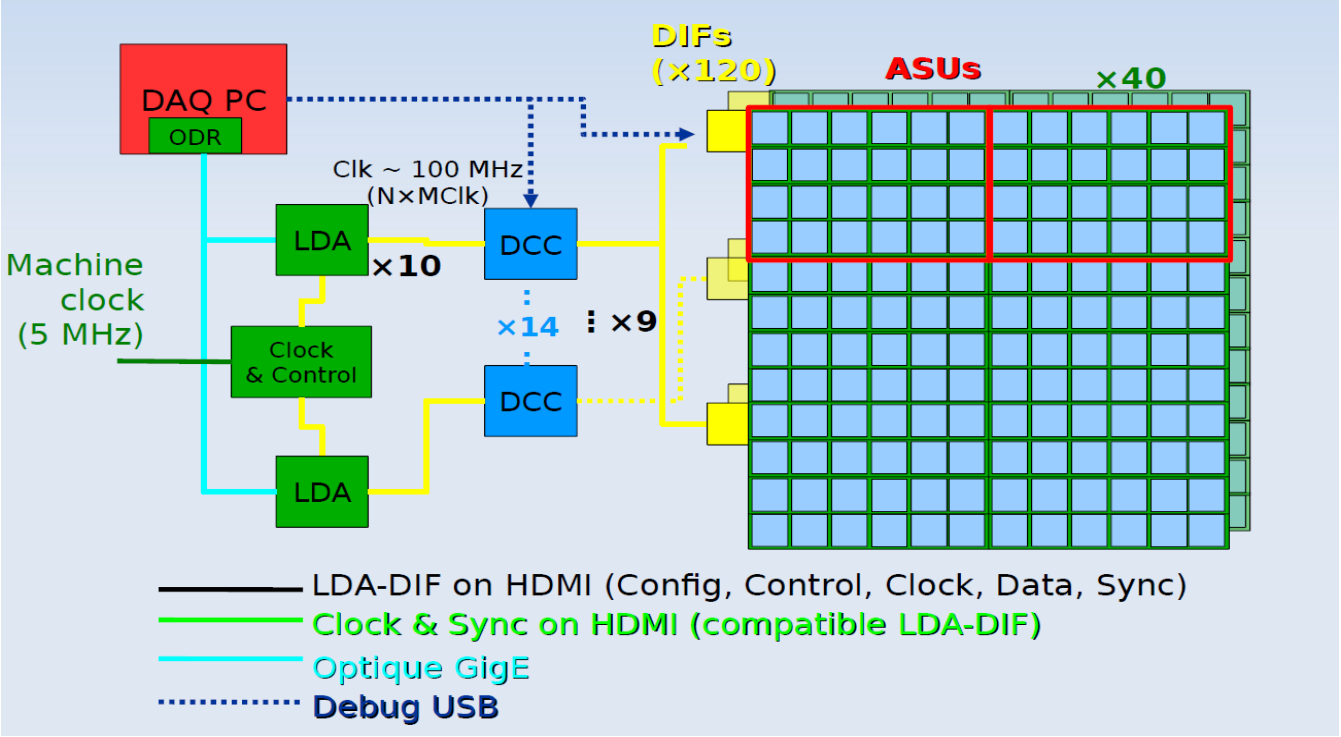
Detector InterFace developements

Firmware is on going for the CALICE DAQ

LAPP participates in the DIF Task Force which elaborates the CALICE DAQ protocol

Purpose: Perform a cubic meter with 400 000 channels read by DIFs and store data on a PC through the DAQ.



Conclusion

Developments of DHCAL readout and DAQ is in a good way :

→ DIF boards and VHDL firmware for different ASICs

→ Tests of various readout chips (Hardroc, Dirac)
Dirac optimized for MICROMEGAS

→ Work on a future CALICE DAQ
Should be ready in 2011