#### MICROMEGAS DHCAL

W-DHCAL workshop, Annecy

C. Adloff for A. Espargilière

September 24, 2009

#### Outline

- Simulation Activities
- MICROMEGAS Developments for DHCAL Active Layer
  - Bulk MICROMEGAS Prototypes
  - Electronics and acquisition
  - Analysis Framework
  - MICROMEGAS analog prototypes performances
  - Tests with digital electronics
  - Square meter project
- Engineering Developments
- Electronics Developments
  - Detector InterFace (DIF)
  - DIRAC ASICs Characterization and New Developments
- Conclusion

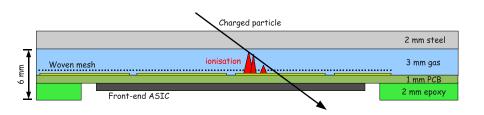


## SIMULATION ACTIVITIES

#### Simulation Activities

- Cubic Meter Simulation (Jan Blaha):
  - Better understanding of DHCAL generally
  - The first qualitative view on DHCAL global performance
  - Study performed:
    - Study of the main calorimeter characteristics
    - Comparison of various absorber materials: Fe, W, Pb
    - Comparison of analog and digital readout
    - Dependency on the readout threshold
- High Energy Physics Simulation (J. J. Blaising)

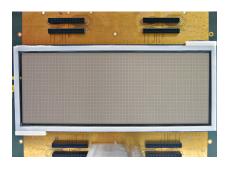
# MICROMEGAS DEVELOPMENTS FOR DHCAL ACTIVE LAYER



## Bulk Micromegas Prototypes

#### **General Features**

- Robustness, industry process
- ullet Low voltage ( $V_{
  m mesh}$  &  $V_{
  m drift}$  < 500 V)
- $120\mu m$  amplification gap
- 1 cm<sup>2</sup> pads readout
- Needs for low noise electronics
- Needs for reliable sparks protection

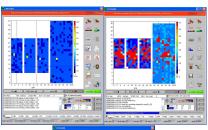


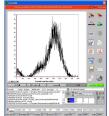
## ELECTRONICS AND ACQUISITION DAQ (D. Roy)

#### CENTAURE for analog readout

CENTAURE used for analog data acquisition and online monitoring

- Developed by D. Roy (SUBATECH, Nantes)
- GASSIPLEX chips on external boards
- Mesh readout





## ELECTRONICS AND ACQUISITION

DAQ (C. Drancourt)

#### LabVIEW for digital readout

- Home made software for chips characterisation
- HARDROC1, HARDROC2 (input for calibration) and DIRAC chips
- Development for cosmic data acquisition ongoing



## ELECTRONICS AND ACQUISITION

DAQ (C. Combaret)

#### X-DAQ

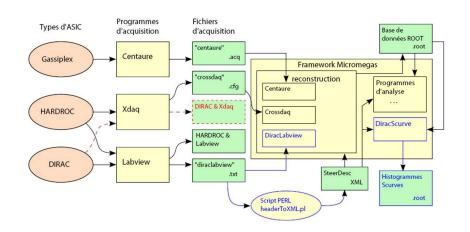
- Developed at IPNL
- Used for fast data acquisition
- Works for HARDROC1 and 2
- Development for DIRAC ongoing

#### Aspects

- Fast running
- html control interface
- need expert on site

#### **Analysis Framework**

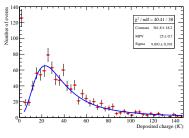
(J. Jacquemier)

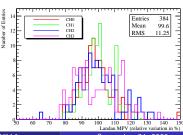


Characteristics (A. Espargilière)

#### Beam test 2008 Results

- Overall gain disparity  $\approx 11\%$  (384 cm<sup>2</sup>)
- Efficiency = 97% at  $1.5 \, \mathrm{fC}$
- $\bullet \ \mbox{Maximum Multiplicity} < 1.1 \ \mbox{at} \\ 1.5 \ \mbox{fC}$

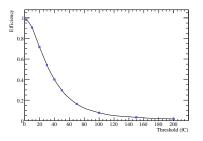


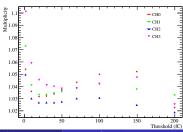


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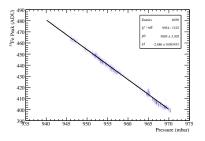




Environmental Study (M. Chefdeville)

- Two-week long data acquisition
- 5.9 keV photons from <sup>55</sup>Fe
- Dependency of response versus
   P and T
- Method for gain correction established:

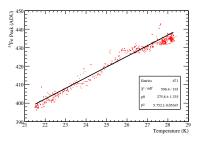
$$f_x = 1 - C_x \cdot \Delta(x)$$



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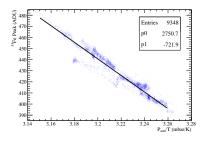
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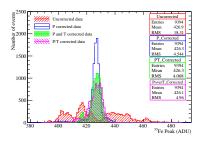
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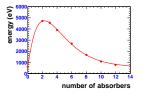
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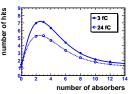
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Shower Measurements (M. Chefdeville)

- Micromegas behaviour in 2 GeV electron:
  - Stable and high gain during test period (a few HV trips over 12 days)
  - correction for P, T variations, pads intercalibration
- Energy and number of hit distributions:
  - Show a similar trend with the number of absorber
  - Longitudinal hit distribution maximum reached slightly deeper
  - Transverse hit distribution shows larger RMS at first shower stages
- Future plans
  - Comparison with simulation
  - Take data at different energies at next beam test (next week)





### Tests with digital electronics

#### First embedded electronics on a MICROMEGAS

- Single DIRAC chip 8×8 pad MICROMEGAS chamber
- 10,7 mm thickness

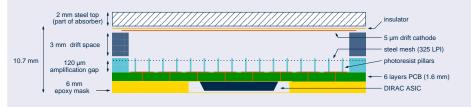


Figure: design of a bulk MICROMEGAS with embedded electronics

### Tests with digital electronics

#### First DIRAC operative test (Beam test 2008, August)

- Single ASIC 8×8 pad MICROMEGAS chamber
- Very first test of bulk MICROMEGAS with embedded digital readout
- fully successful
- Raw multiplicity of 1.1

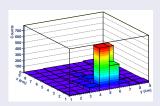
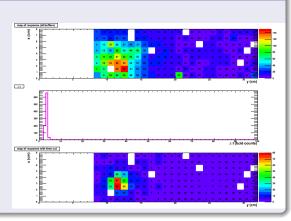


Figure: Beam profile obtained with digital readout using the DIRAC ASIC.

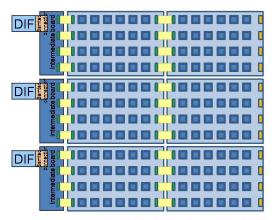
## Tests with digital electronics

#### First $\operatorname{HARDROC1}$ operative test on $\operatorname{MICROMEGAS}$ (Beam test 2009, May)

- Beam profile observed w and w/o scintillator coincidence
- ▶ data mostly corrupted
- Raw efficiency estimated around 60%

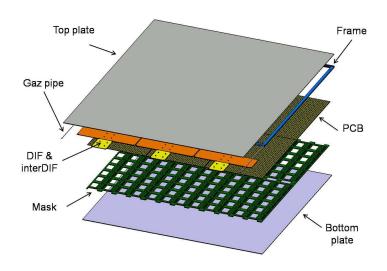


Layout (N.Geffroy)

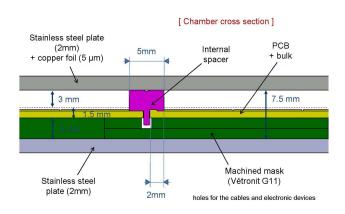


- : Flat Printed Circuit
- : ASIC chip (64 channels)
- : Hirose connector
- : Terminasion component

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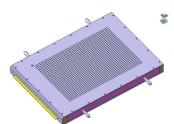


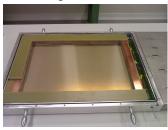
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Test Box (N.Geffroy, F. Peltier)

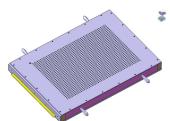
- Every ASU has to be tested individually:
  - Electronics verifications
  - Mesh cooking
  - Get physical signal from the pads (<sup>55</sup>Fe source and/or cosmics)
- Clean room available for handling naked mesh ASU
- A test box has been built:
  - ASU easily inserted and removed
  - Plexiglass lid for mesh cooking
  - Aluminum lid, drilled above every pad for X-rays injection
  - Drift cathode on the aluminum lid
     ⇒ 3 cm drift gap
  - A fully functional MICROMEGAS test chamber

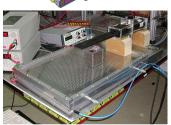




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## Square Meter Project Test Box

#### First tests of MICROMEGAS HARDROC2 at LAPP

- Two 32×48 pad ASU
- 24 HARDROC2 chip each
- Foreseen to equip the m<sup>2</sup> physics prototype

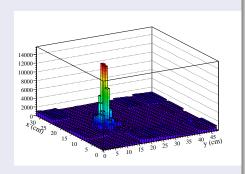


Figure: Response of a  $32\times48\,\mathrm{pad}$  ASU after irradiation with an  $^{55}$ Fe source

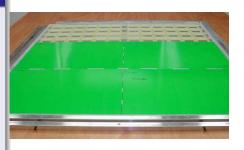
Mechanical Prototype (N.Geffroy, F.Peltier)

- Test various assembly possibilities on small samples
- Establish an assembly process
- Train on building a prototype w/o real ASUs
- Perform mechanical tests
- Verify gas tightness



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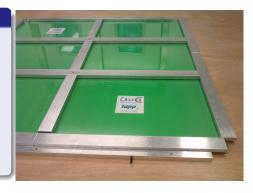
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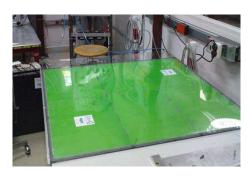
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• 1 week needed for assembly



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- A third of the m<sup>2</sup> will be equipped (2 ASUs)



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- Both ASUs are under intensive tests to prove their reliability before integration to the m<sup>2</sup>
- next : Physics m<sup>2</sup> assembly



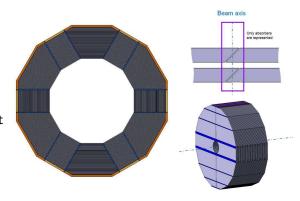
## Engineering Developments

## SID DHCAL Mechanical Design

(N.Geffroy)

#### SiD HCAL:

- Designed at LAPP
- Taken as a baseline in SiD LOI
- Detailed design needed
- Deeper study foreseen at LAPP (N. Geffroy)
- → Construction of a module 0

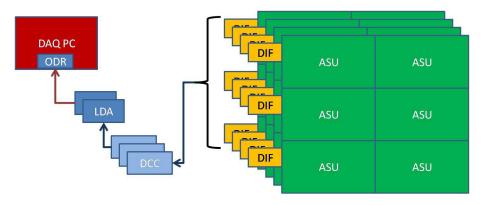


## ELECTRONICS DEVELOPMENTS

## Detector InterFace (DIF)

(J. Prast, G. Vouters)

#### Calice DAQ Scheme:



 $\mathsf{DIF} \Longleftrightarrow \mathsf{front}\text{-}\mathsf{end}\ \mathsf{electronics}\text{:}\ \mathsf{data}\ \mathsf{transfer},\ \mathsf{very}\ \mathsf{front}\text{-}\mathsf{end}\ \mathsf{chip}\ \mathsf{control}$ 

## Detector InterFace (DIF)

(J. Prast, G. Vouters)

- Fully Designed at LAPP (J. Prast, S. Cap)
- First intermediate board between ASU and DAQ
- Programmable via VHDL code
- VHDL code implemented at LAPP (G. Vouters)
- Many firmwares available (see C. Drancourt's talk)
- Used in 2008 and 2009
   Eu-DHCAL beam tests:
   MICROMEGAS and RPC



## DIRAC ASICs Characterization and New Developments (R. Gaglione)

- DIRAC initially developed at IPNL
- Now in tight collaboration with LAPP
- DIRAC2 intensively tested at LAPP
- Best Power pulsing performance (stable at  $2.7 \,\mu \mathrm{s}$  power-on time)
- Very low threshold achievable (<10 fC?)</li>
- First digital ASIC embedded on a bulk MICROMEGAS: tested successfully in 2008 beam test
- DIRAC2 m<sup>2</sup> foreseen for 2010

## CONCLUSION

#### Conclusion

- Developments of MICROMEGAS chamber as an active layer for DHCAL
  - MICROMEGAS performances in agreement with the DHCAL requirements
  - Digital front-end electronics ready
  - MICROMEGAS related collaborators: CERN (bulk MICROMEGAS) and Saclay (Beam tests ...)
  - Eu-DHCAL collaborators: CIEMAT, IPNL, LAL, LLR
  - Building thin and large area chambers
  - Very good progress toward a 1 m<sup>3</sup> technical prototype
- Other applications of MICROMEGAS now thinkable
  - MICROMEGAS W-HCAL (almost "copy and paste")
  - MICROMEGAS W-ECAL (segmentation and thickness)