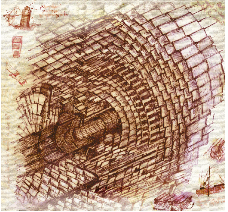
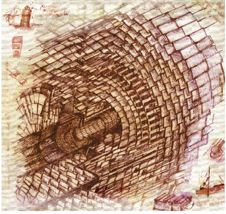
Possible Tracking Trigger
Stacked Module Options



Possible Tracking Trigger Stacked Module Options

- The schemes proposed so far for constructing L1 Trigger primitives using information from the Tracker, all rely on the ability to filter hits from low Pt tracks, locally to a module, in order to reduce both data rates and combinatorial complexity to a realistically manageable level.
- One of the proposed schemes relies on “Stacked Modules”, with a pair of sensors separated by approximately 1mm. The sensors typically consist of “long pixels”, with a pitch of ~ 100um and a length in the range of 1 ~ 2.5mm.
- In this scheme, hits from the pair of sensors are combined to provide local track vectors, or “Stubs”.
  - A rejection factor of ~ 10 can be achieved, for a corresponding Pt threshold as low as ~ 2GeV
- In the Double Stack Tracker Straw Man [Ref.1], Stacked Modules are deployed throughout the Tracker, and are used for both the L1 Trigger and Tracking functions.
  - In this case, the Stacked Module must also be able to make all hits/clusters available to be read out for events accepted by the L1 Trigger.



Possible Tracking Trigger Stacked Module Options

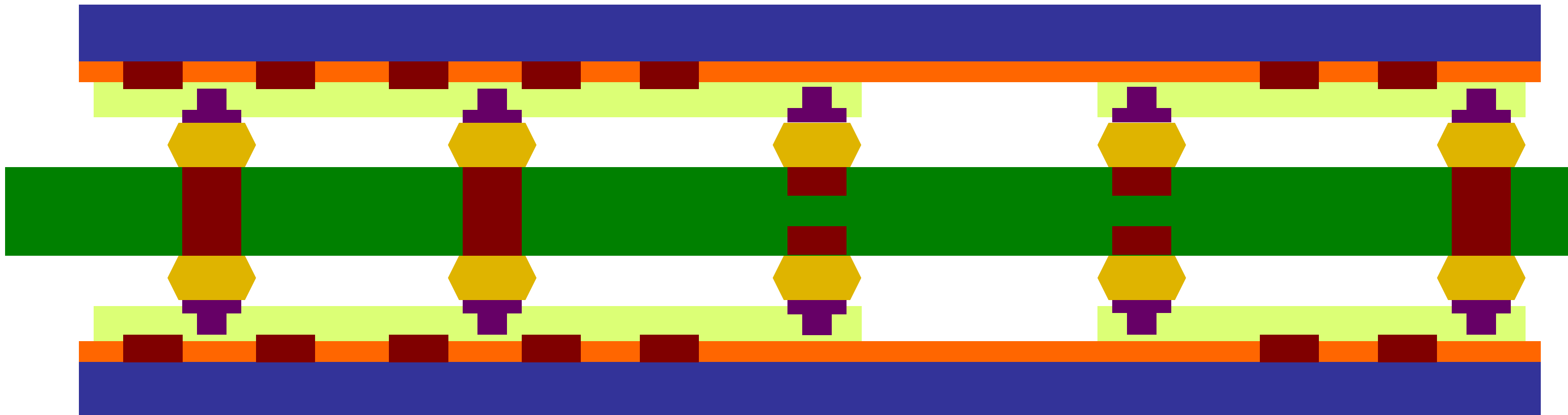
- The key functionality of the Stacked Module, however, is to bring together the information from the top and bottom sensors, such that Stubs may be formed and acted upon.
- An interesting approach to this, is that of a Vertically Integrated module, in which the information from one sensor ("Slave") is brought to the electronics servicing the second sensor ("Master") in a distributed fashion, through the bulk of the Module.
- Engineering studies and discussions with a number of potential Industrial Partners are underway, and R&D initiatives are being prepared to identify and develop viable technologies and designs for the production of such modules, in large quantities.
  - These will be the subjects of a coordinated set of R&D proposals.

Example Stacked Module: Chip Through Vias & Direct Oxide Bonds V1

- Signal & services routing possible over large area
  - Can shield & Minimize cross-talk to sensor

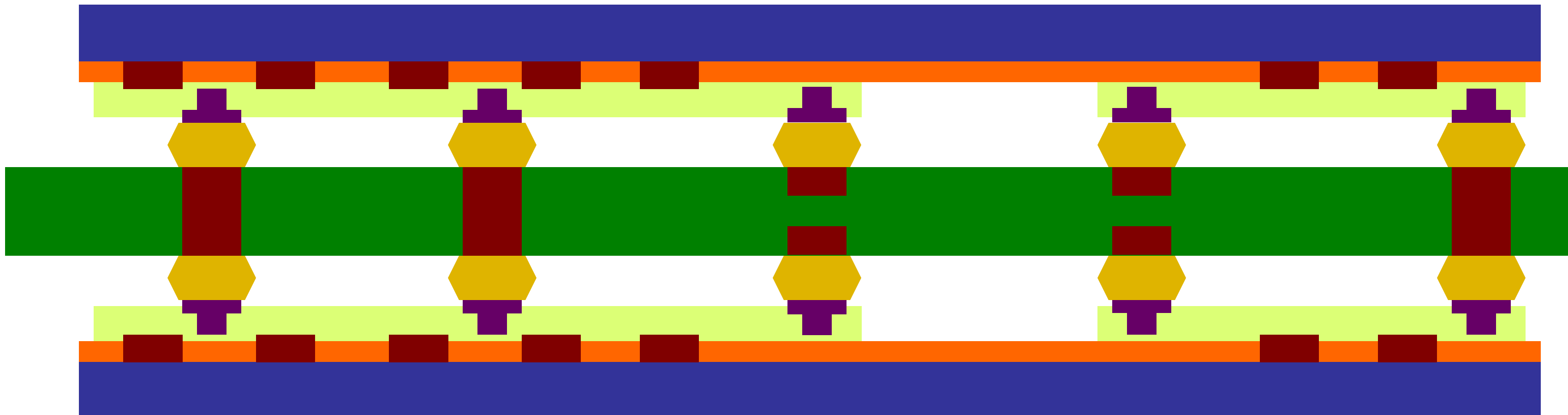
However:

- Requires Direct Oxide Bonding to Large Area device
  - Large size chip probably favored
- Requires chip silicon through-vias

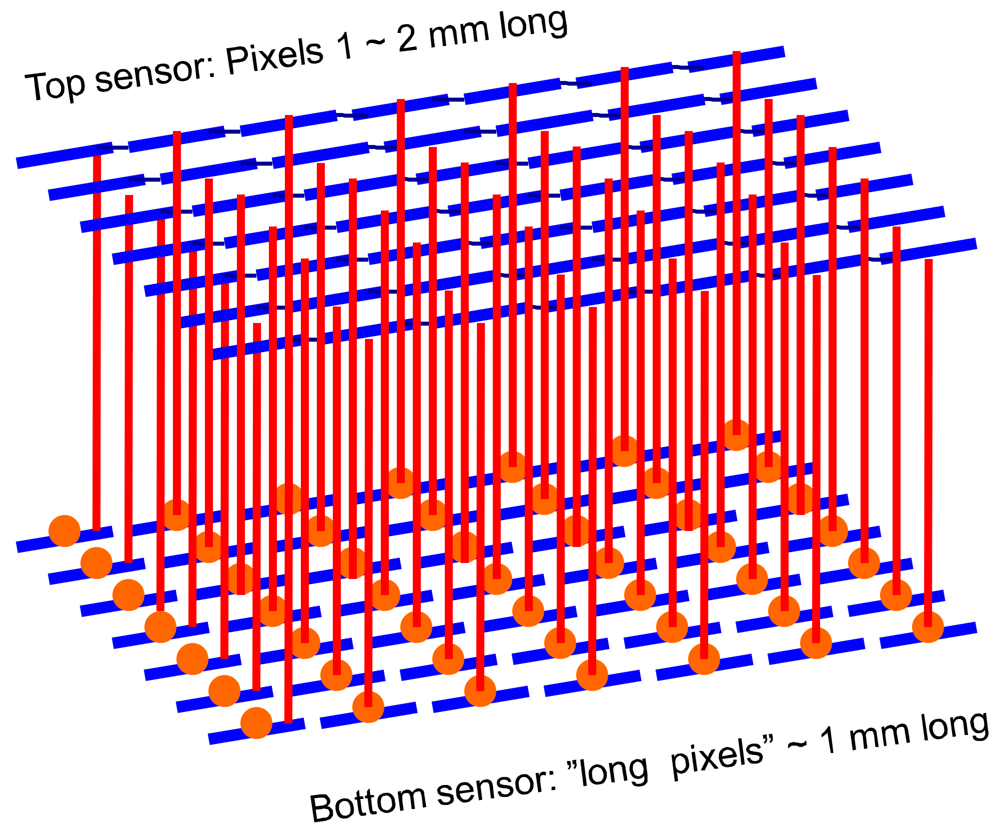


Example Stacked Module: Chip Through Vias & Direct Oxide Bonds V1

- Sensor to Read-Out Chip (ROC) Connections density 400 ~ 800 / cm^2
- ROC to Interposer Connections density ~ 20 / cm^2 Distributed
  - Excluding ROC1 to ROC2
  - Power, L1 Trigger & Read-Out Data, and Control Lines
  - Use ROC through -vias
- ROC 1 to ROC 2 Connections density 40 ~ 200 / cm^2 Distributed
  - Data from ROC1 (slave) to ROC2 (master) layers
  - Use ROC and Interposer through-vias



Schematic Illustration
Pixels on top tier
individually connected to bottom tier



Top to bottom connections:
Interposer and Front-End chips
Not shown

Schematic Illustration
"Short Logical Strips" on top tier individually connected to bottom tier

Schematic Illustration
"Short Logical Strips" on top tier connected to bottom tier with Nx multiplexing

Top sensor: "short Strips" 5 ~ 10 mm long

Top to bottom connections:
Interposer and Front-End chips
Not shown

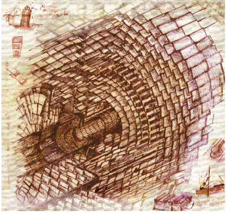
Bottom sensor: "long pixels" ~ 1 mm long

Schematic Illustration "Short Logical Strips" on top tier connected to bottom tier with Nx multiplexing

Top sensor: "short Strips" 5 ~ 10 mm long

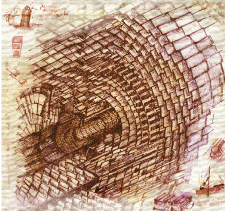
Top to bottom connections:
Interposer and Front-End chips
Not shown

Bottom sensor: "long pixels" ~ 1 mm long



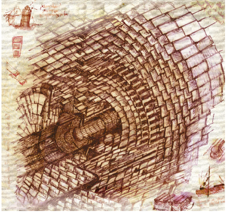
Schematic Illustration "Short Logical Strips" on top tier connected to bottom tier with Nx multiplexing

- In this example, we consider
  - Pixels of 100um * 1.25mm
  - Logical Strips consisting of the "OR" of 8 longitudinally adjacent Pixels covering 100um * 10mm
  - multiplex groups of 8 Slave Tier logical strips, adjacent in phi, onto a single transmission line
  - Read-Out chips are taken to be 128 pixels wide in phi by 16 pixels long in Z, to cover two consecutive logical strips
    - This corresponds to approximate chip dimensions of 12mm* 20mm
  - modules are 8 chips wide by 4 chips long
    - total of ~ 2 * 65'500 pixels in each module
  - each group of logical strips in the Slave Tier is assumed to have an L1 Data Path both to the chip directly below it on the Master Tier, as well as to its neighbor
  - this leads to a density of data paths through the interposer of about 25/cm^2
    - If arranged in-line at the Z boundaries of the read-out chips, this corresponds to a net pitch of ~ 400um



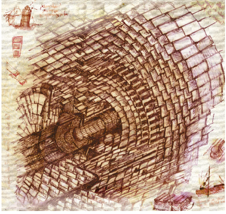
Schematic Illustration "Short Logical Strips" on top tier connected to bottom tier with Nx multiplexing

- **An option under consideration for the data links from the Slave to the Master Tier uses differentially driven current switching**
  - The operation of such links at 320Mbps, over distances of order meters, with power consumption in the range of ~ 1mW, is currently under study
  - With ~25 links/cm^2, this would result in a power consumption of ~ 2W for the Slave to Master Tier data transfer in an 80cm^2 module
  - In this scheme a reduction by at least a factor of two in the power dissipation per link, exploiting the very short transmission distance and correspondingly low parasitic resistances and capacitances involved, would clearly be desirable, and it would be mandatory in case shorter logical strips are required to maintain a sufficiently low occupancy
    - A possibility may be to operate the data links at higher speeds. Operating at 640Mbps, for example, could allow multiplexing 16 logical strips onto a single link, thus reducing the number of links and the associated power by a factor of two



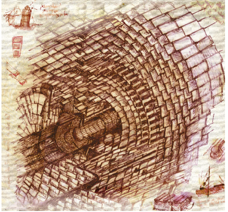
Schematic Illustration "Short Logical Strips" on top tier connected to bottom tier with Nx multiplexing

- **Alternatively, schemes that exploit the very low cell occupancy to substantially reduce power for the Slave to Master Tier data transmission may also be considered.**
- **For example, in voltage switching or current modulation schemes, in which "0" is a low power quiescent state, the power consumption could be greatly reduced.**
  - **However, the implications on the system performance of the transients associated with such schemes require careful study.**
- **We assume that the Slave to Master Tier data transfer for a module of ~ 80cm^2 can be achieved for ~ 1W or less.**



Schematic Illustration "Short Logical Strips" on top tier connected to bottom tier with Nx multiplexing

- We assume a total of ~ 24 bits associated to each stub transmitted off module for the L1 Trigger.
  - At a radius of ~ 34cm, assuming a cluster occupancy of ~ 40MHz/cm^2, and that ~1/10 of clusters form an accepted stub, the resulting average data rates transmitted off module for the L1 Trigger are ~ 8Gb/s. Allowing for a factor of two margin requires an available bandwidth of ~ 16Gb/s for modules at this radius.
- For L1 accepted events, it is assumed that all hits digitized by each the Slave and Master Tiers are independently read-out, at the full pixel granularity of 100um * 1.25mm.
- A simple on-chip clustering and zero-suppression is assumed, and we allow for 32 bits of information for each cluster.
  - For modules at a ~ 34cm radius, and assuming a cluster hit rate of 40MHz/cm^2, this results in an off-module data rate for the read-out of L1 accepted events at 100kHz of ~ 2 * 250Mb/s per module, a small fraction of the L1 Trigger data rate.
  - We assume that an independent data path is provided for this purpose

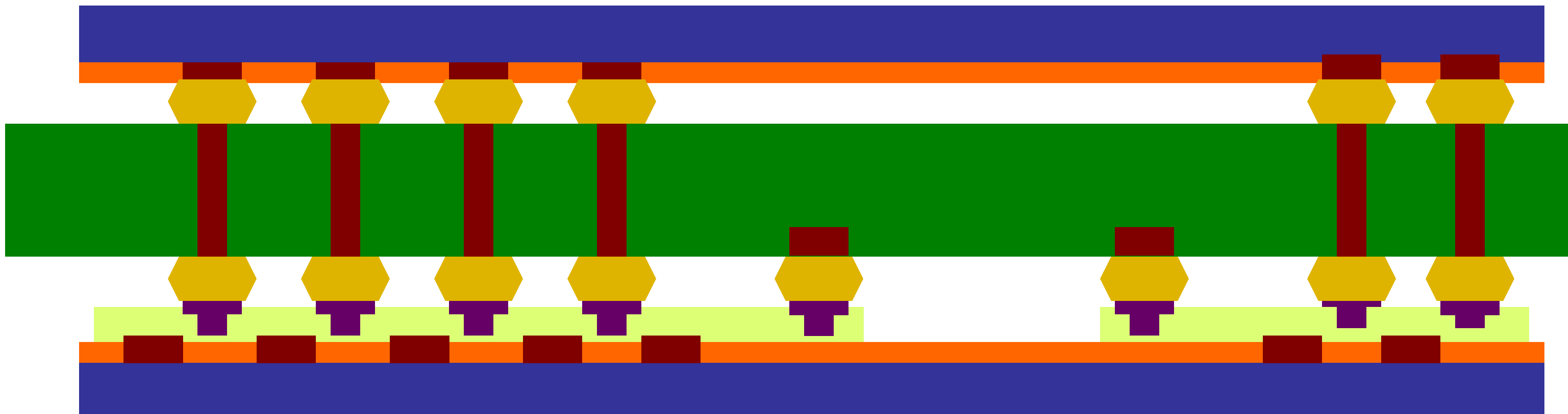


Example Stacked Module: Chip Through Vias & Direct Oxide Bonds V2

- Only one chip layer, not two
- Information brought directly where you need it, at the Pixel level

However:

- Increased input capacitance? Shielding & cross-talk to sensor ?
- Requires Direct Oxide Bonding to Large Area device
  - Large size chip probably favored
- Requires chip silicon through-vias



Example Stacked Module: Chip Through Vias & Direct Oxide Bonds V2

- Sensor to Read-Out Chip (ROC) Connections density 400 ~ 800 / cm^2
- ROC to Interposer Connections density ~ 20 / cm^2 Distributed
  - Excluding ROC1 to ROC2
  - Power, L1 Trigger & Read-Out Data, and Control Lines
  - Use ROC through -vias
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  - Data from Sensor 1 (slave) to ROC2 (master) layers
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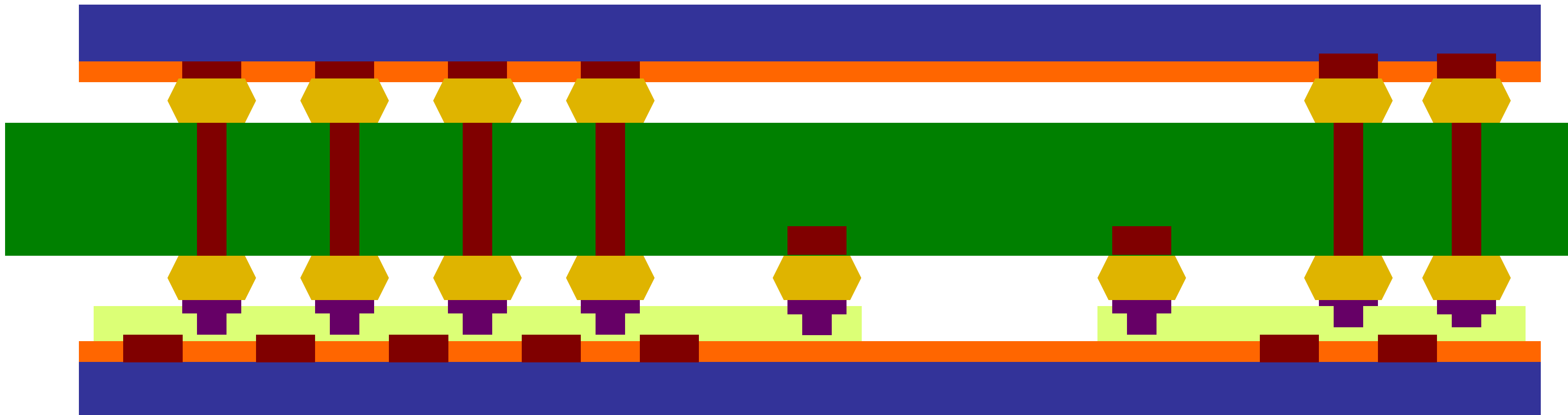
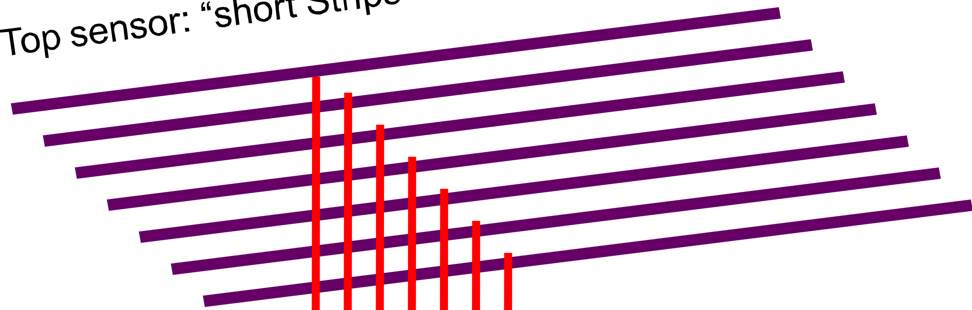
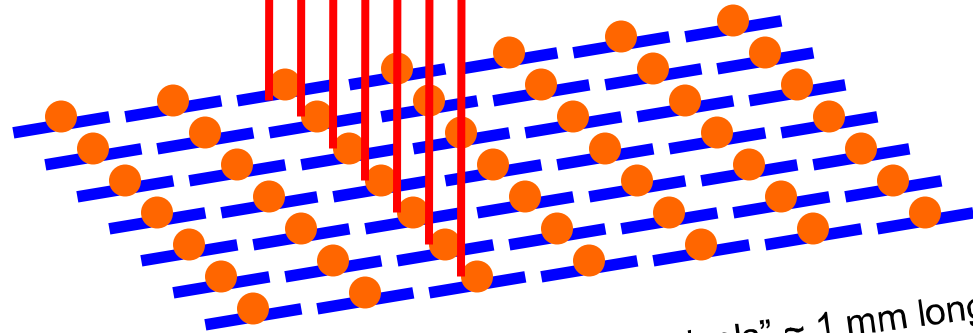


Schematic Illustration
"Short Physical Strips" on top tier individually connected to bottom tier

Top sensor: "short Strips" 5 ~ 10 mm long



Top to bottom connections:
Interposer and Front-End chips
Not shown



Bottom sensor: "long pixels" ~ 1 mm long

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Top to bottom connections:
Interposer and Front-End chips
Not shown

Bottom sensor: "long pixels" ~ 1 mm long

Schematic Illustration "Short Physical Strips" on top tier individually connected to bottom tier

This leads to a density of connections, from the Slave to the Master Tier, of about 100/cm^2.
If arranged in-line at the Z boundaries of the Master Tier read-out chips this corresponds to a net pitch of ~ 50um

Top sensor: "short Strips" ~ 10 mm long

Top to bottom connections: Interposer and Front-End chips Not shown

Bottom sensor: "long pixels" ~ 1 mm long

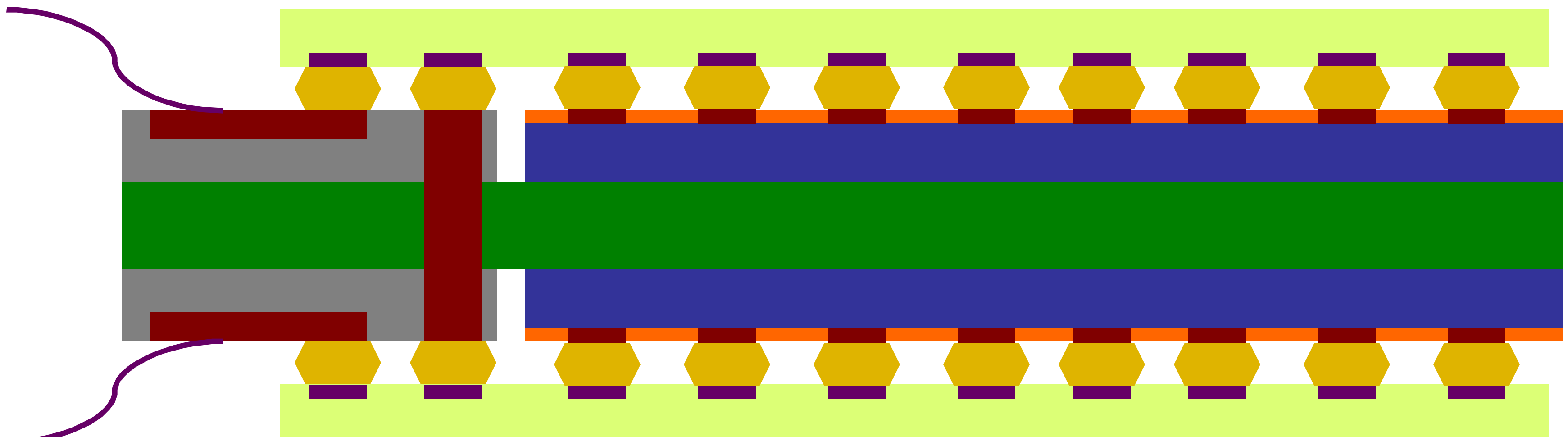
Backup material

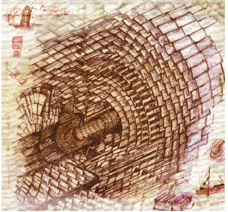
Example Stacked Module: Bump Bonding

- **Relatively Coarse Pitch Bump Bonding technology ~ in hand**
  - For example, IBM C4 (multi-tier bump bonds is a complication)

However:

- **Long Signal Routing to Module Periphery**
  - Power penalty
  - Module width = 2 * Chip Width; Large size chip probably favored





Example Stacked Module: Bump Bonding

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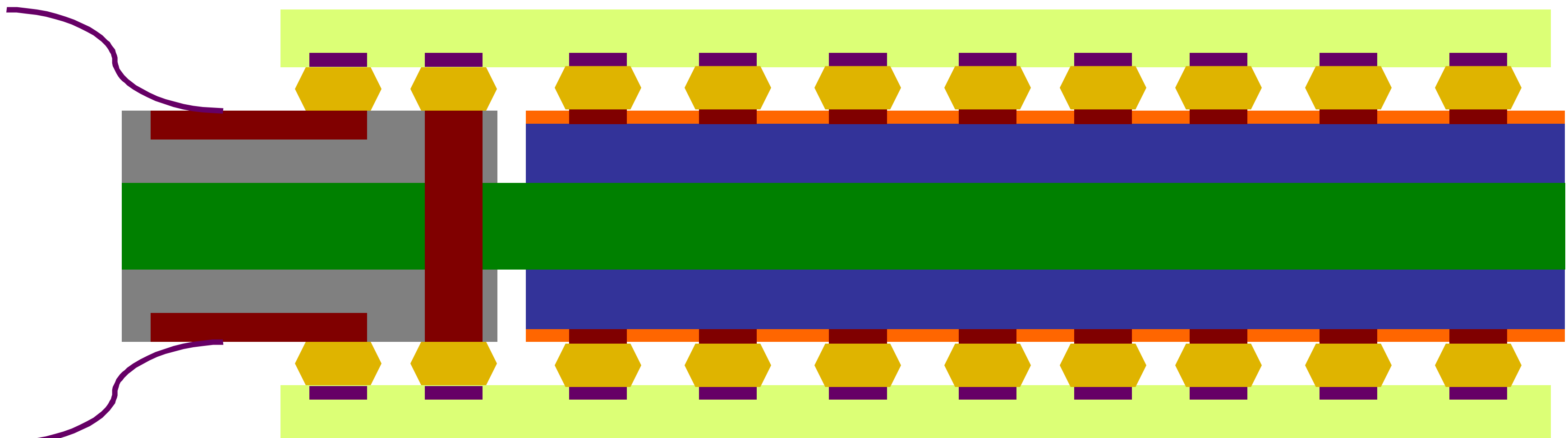
  - Excluding ROC1 to ROC2
  - Power, L1 Trigger & Read-Out Data, and Control Lines
- ROC 1 to ROC 2 Connections density 200 ~ 800 / cm^2 Locally
  - Data from ROC1 (slave) to ROC2 (master) sensor layers
  - Use 2'nd metal layer on sensor & through-vias in bus-bar

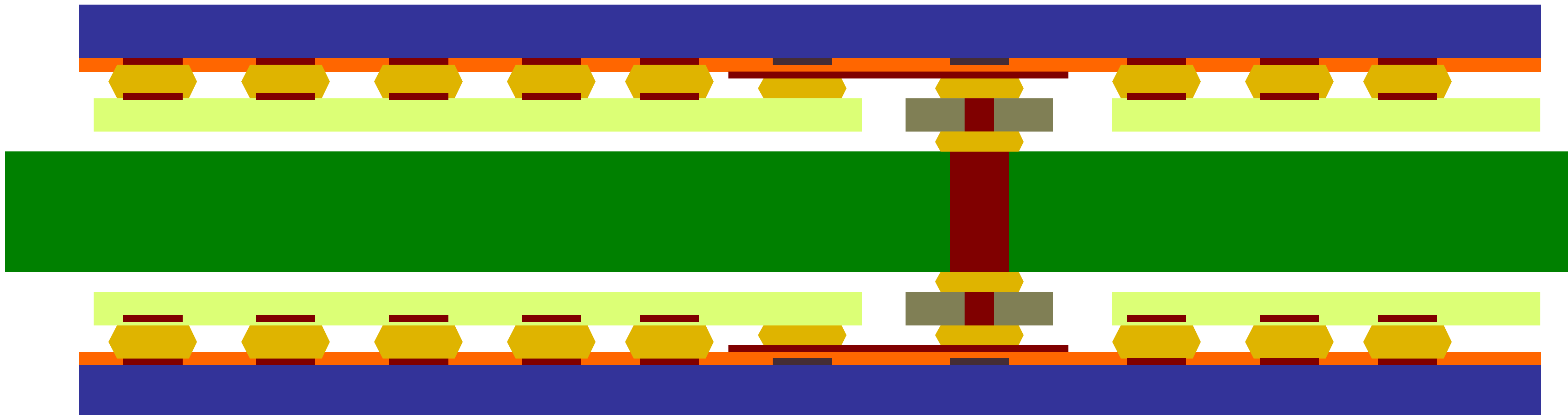


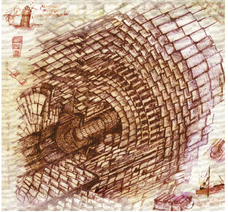
Example Stacked Module: 2 Metal Layers on Sensor & Bump Bonds

- Relatively Coarse Pitch Bump Bonding technology ~ in hand
  - For example, IBM C4 (multi-tier bump bonds is a complication)

However:

- Signal & services routing along narrow 1 ~ 2mm wide bus-bar
  - Very challenging: cross-talk from 2nd metal to sensor? Space available?
  - Small chip size will be favored





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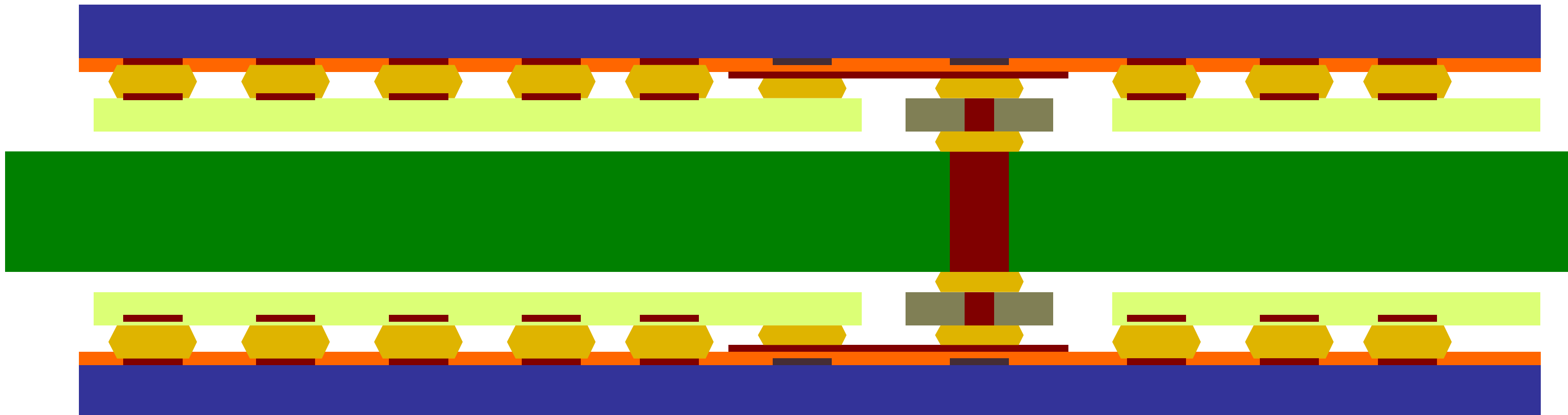
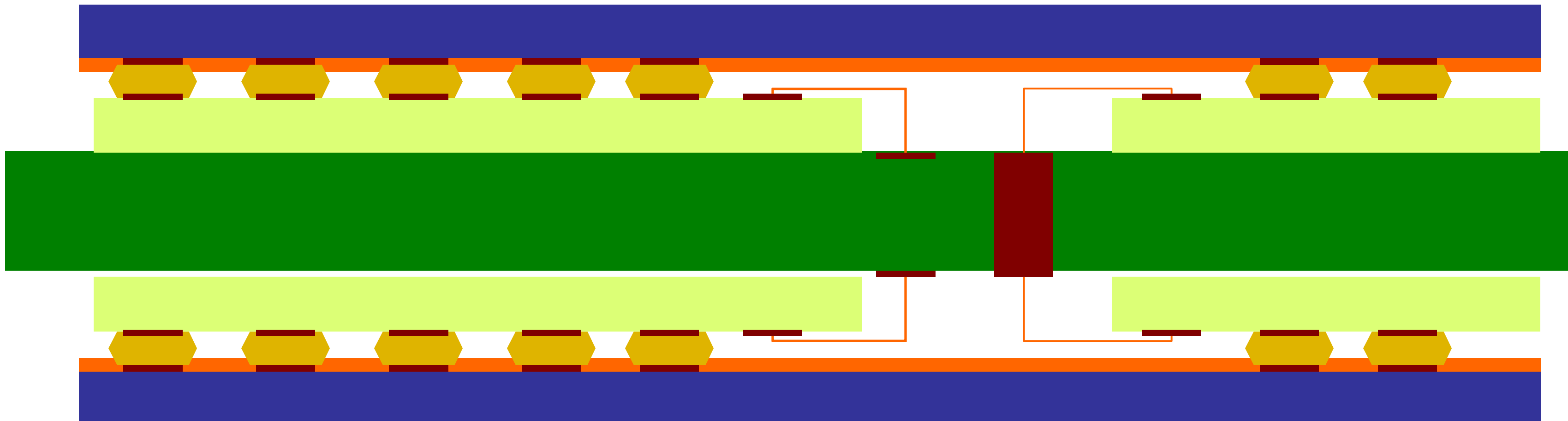


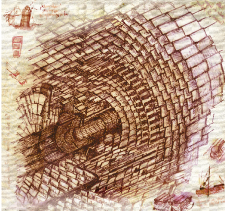
Example Stacked Module:
2 Metal Layers on Sensor & Bump Bonds

- **Relatively Coarse Pitch Bump Bonding technology ~ in hand**
  - For example, IBM C4 (multi-tier bump bonds is a complication)

However:

- **Signal & services routing along narrow 1 ~ 2mm wide bus-bar**
  - Reliable wire bonding within limited height ? Space available?
  - Small chip size will be favored





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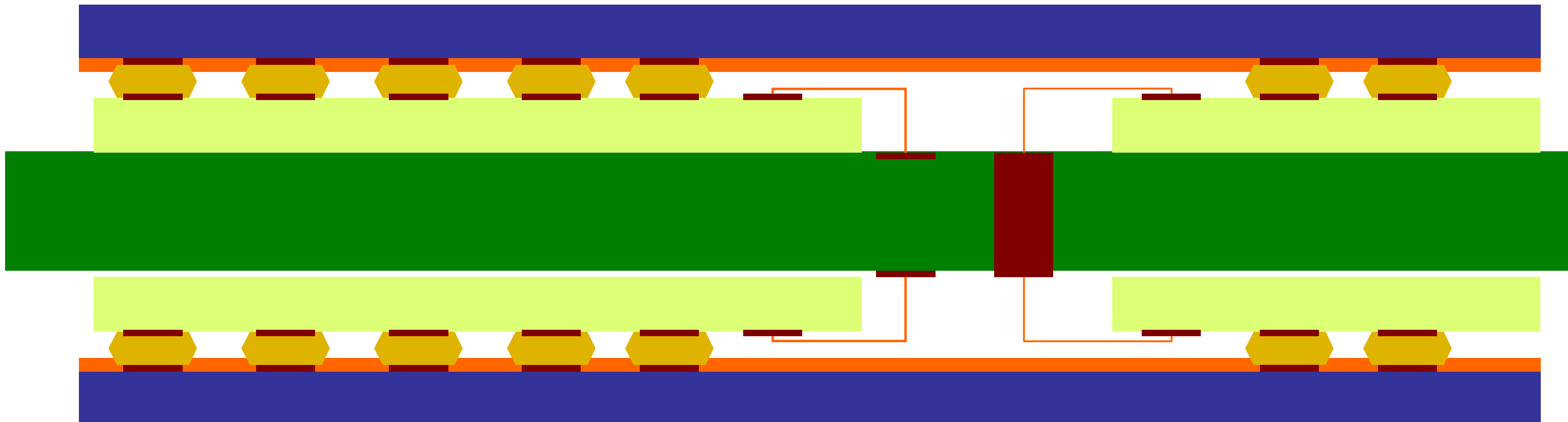
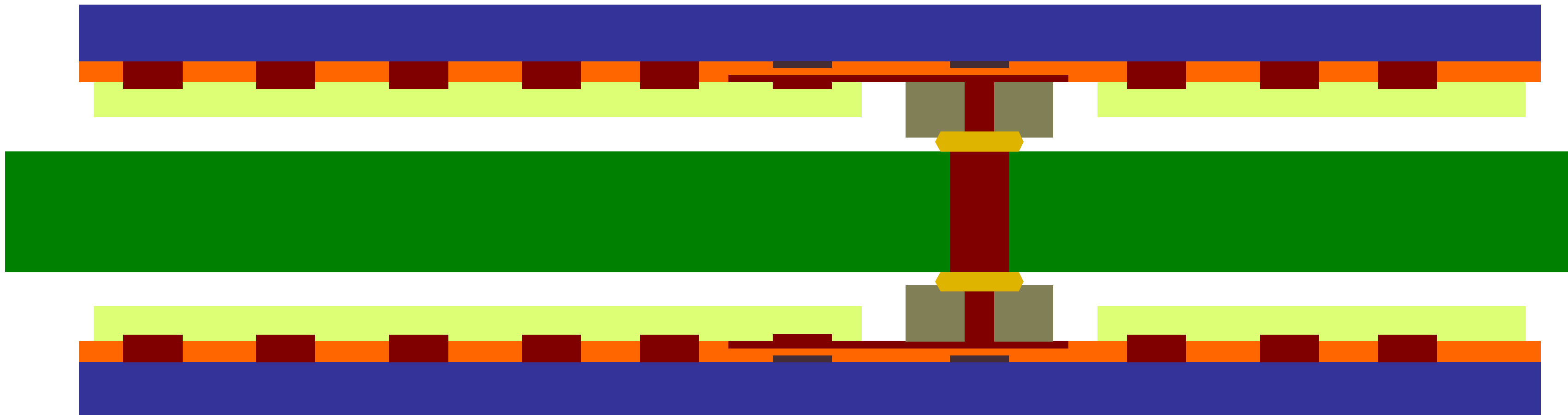


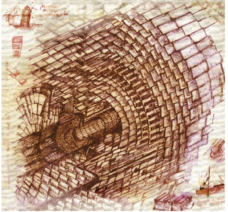
Example Stacked Module: 2 Metal Layers on Sensor & Direct Oxide Bonds

- Multi-tier bump bonding issue may be simplified ?

However:

- Requires Direct Oxide Bonding to Large Area device
- Signal & services routing along narrow 1 ~ 2mm wide bus-bar
  - Very challenging: cross-talk from 2nd metal to sensor? Space available?
  - Small chip size will be favored





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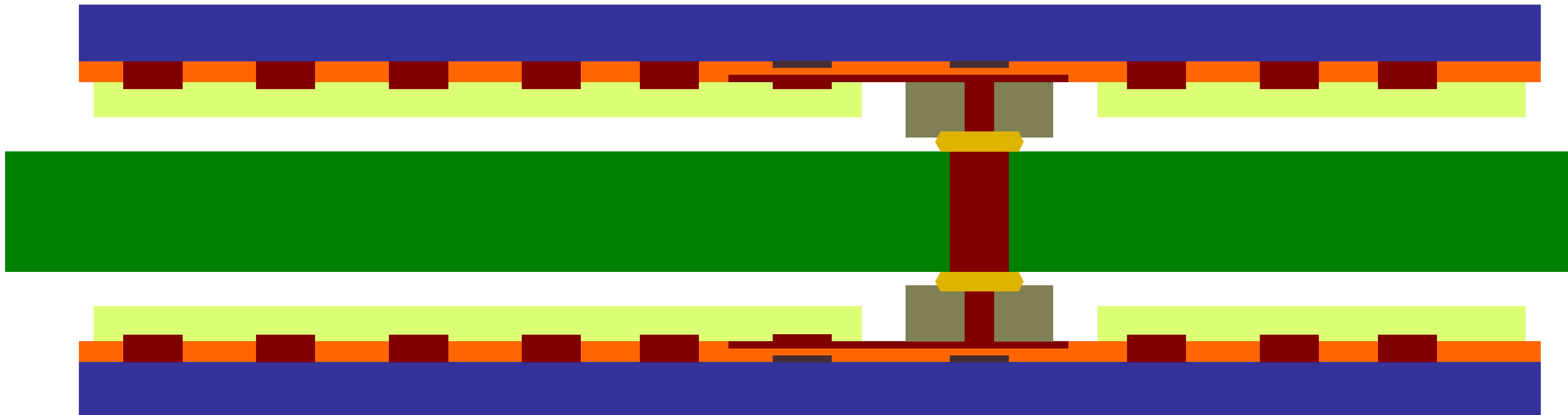
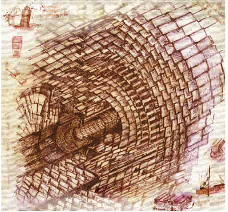


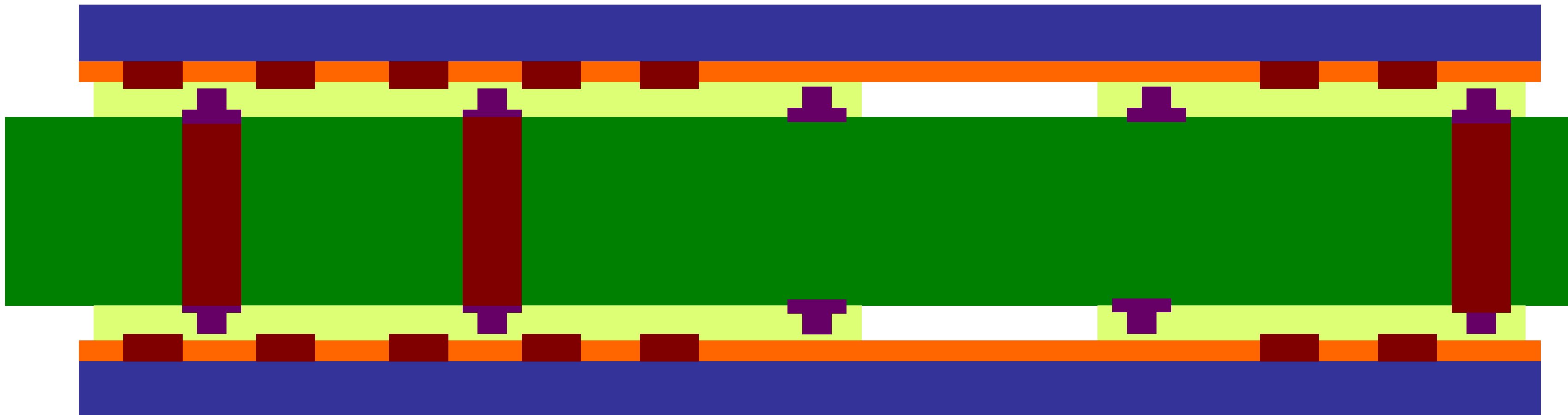


Example Stacked Module: Chip Through Vias & Direct Oxide Bonds V1

- Signal & services routing possible over large area
  - Can shield & Minimize cross-talk to sensor

However:

- Requires Multi-Tiered Direct Oxide Bonding to Large Area device
  - Large size chip probably favored
- Requires chip silicon through-vias



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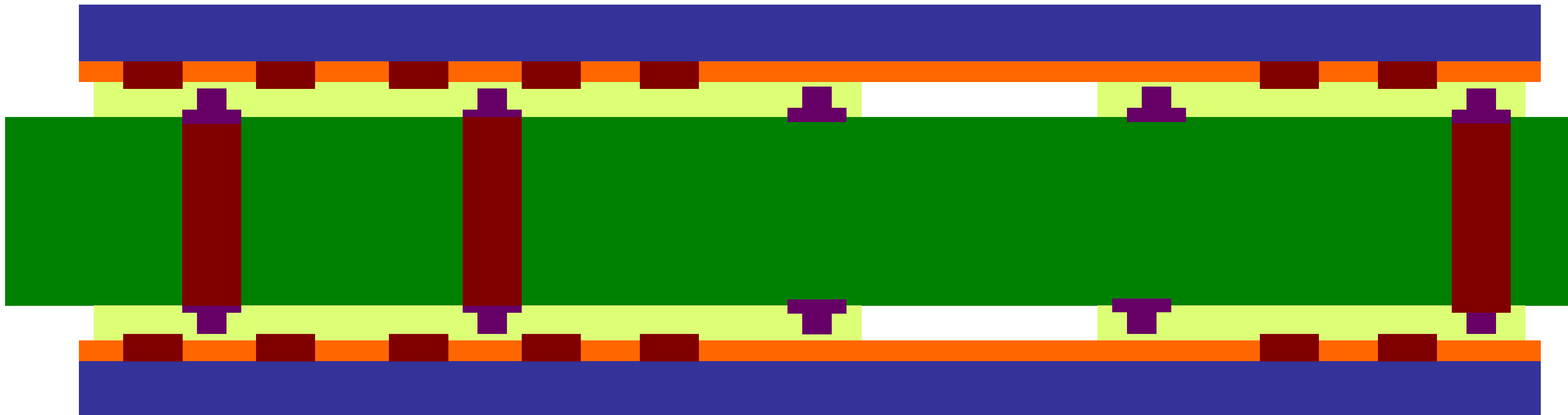
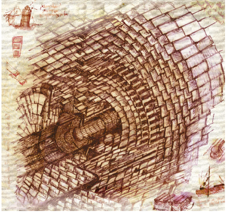


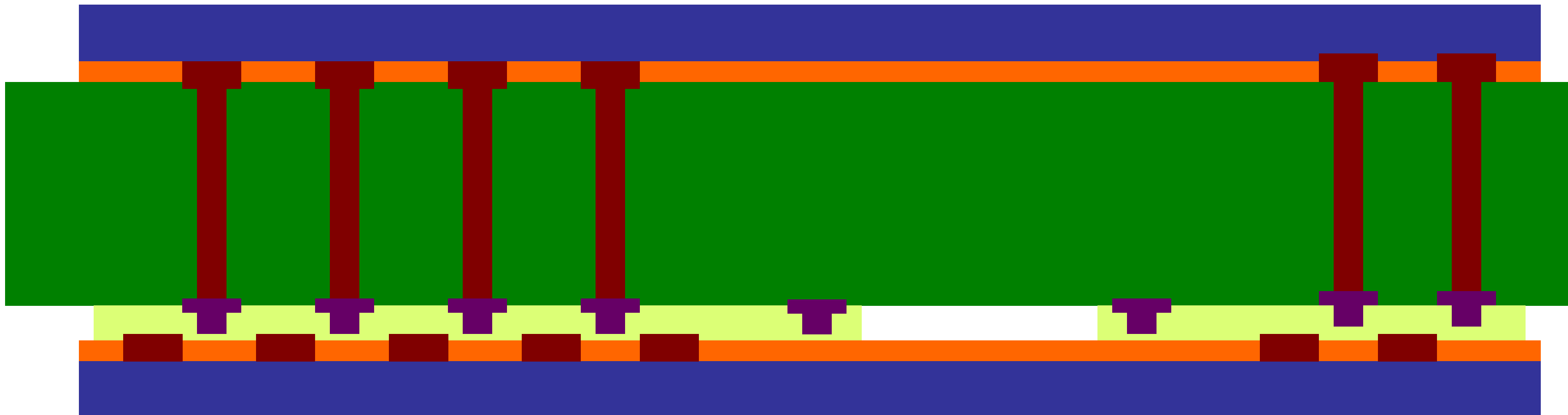


Example Stacked Module: Chip Through Vias & Direct Oxide Bonds V2

- Only one chip layer
- No high speed data lines from Slave to Mater layers

However:

- Increased input capacitance? Shielding & cross-talk to sensor ?
- Requires Direct Oxide Bonding to Large Area device
  - Large size chip probably favored
- Requires chip silicon through-vias



Example Stacked Module: Chip Through Vias & Direct Oxide Bonds V2

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  - Excluding ROC1 to ROC2
  - Power, L1 Trigger & Read-Out Data, and Control Lines
  - Use ROC through -vias
- Sensor 1 to ROC 2 Connections density 400 ~ 800 / cm^2 Distributed
  - Data from Sensor 1 (slave) to ROC2 (master) layers
  - Use ROC and Interposer through-vias