ATLAS Upgrade Plans

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- Provide a very brief overview of Phase-1 Upgrades
- Provide deeper look at Phase-2 Upgrades drawing from six approved TDRs and Timing Detector TP
- Details are generally to be found in later talks in this workshop!
Phase-1 Upgrades

- ATLAS produced a total of five “Phase-1” TDRs, and has additional “small projects”.

- Two TDR projects are in commissioning phase (FTK = hardware tracking trigger, and AFP = forward proton detectors in Roman pots) => not discussed further here.

- Additional small project BIS78 = upgrade of largest $\eta$ chambers in BI (Inner Layer of Muon Spectrometer Barrel) with phase-2 “final prototypes” = sMDT + RPC chambers. Total of 16 chambers, 8/side. Chambers ~ final, electronics = prototypes.

- Three major projects are Phase-1 LAr upgrade, Phase-1 TDAQ upgrade, and NSW. All of these upgrade projects must be “phase-2 compliant”, and will continue to be used during HL-LHC operations.
  - **Phase-1 LAr**: Upgrade of trigger path for LAr calorimeter. Analog trigger tower sub-divided into 10 supercells digitized into 12-bits@40 MHz, and transmitted optically to FPGA-based back-ends for calibration and signal processing.
  - **Phase-1 TDAQ**: Includes L1Calo upgrade to digital “feature extractors” (eFEX for $e/\tau$, jFEX for small-R jets and MET, gFEX for large-R jets), TREX (tile feature extractor), updated Sector Logic and MUCTPI (Muon trigger upgrade), and FELIX (network-based switching fabric for phase-1 and phase-2)
  - **NSW**: replacement for present small wheels (1.3 < $\eta$ < 2.7) based on sTGC and MicroMegas chamber technologies with 8+8 measurement planes and sophisticated digital trigger processor to provide track segments pointing back to the vertex and matching endcap muon systems.
Overview of Phase-2 Upgrade Program
(ultimate $L=7.5 \times 10^{34}$, $\mu = 200$)

**ATLAS Phase-II Upgrade**

Overview, for more details on Phase-II ATLAS upgrade projects, please see slides in backup.

- **Upgraded Trigger and Data Acquisition System:**
  - L0: 1 MHz
  - Improved High-Level Trigger

- **Electronics Upgrade:**
  - LAr Calorimeter
  - Tile Calorimeter
  - Muon system

- **New Inner Tracking Detector**
  (all silicon tracker, up to $|\eta| = 4$)

- **Options:**
  - High granularity timing detector (forward region)
  - High-$\eta$ muon tagger
  - Forward detectors, incl. luminosity

- **New muon chambers in the inner barrel region**
Phase-2 Inner Tracker (ITk) Overview

• Complete replacement of Inner Detector with all-Silicon tracker covering to $\eta = 4.0$

• Highly optimized Tracker layout provides 4 Strip measurements at large radius, and 5 Pixel measurements at small radius in barrel.
• Layout is still evolving for a few more months. Will be based on quad modules.
• Strips has 4 barrels and 6 disks (see material map below). Pixel layout evolves from flat barrel geometry at small $\eta$, to inclined layout at intermediate $\eta$, and ring geometry at large $\eta$. Minimizes silicon area and material.
• Number of hits in barrel $\sim$ 13 (2 hits/strip module), and in more forward regions at least 9 pixel hits (see hit plot below right).
Phase-2 Inner Tracker (ITk) Performance

- Performance shown for d0 and z0, vertexing, and b-tagging up to $\eta=4.0$ (Run 2/ITk)
Phase-2 Inner Tracker (ITk) Strip/Pixel Layout and Fluences

- Complete replacement of Inner Detector with all-Silicon tracker covering to $\eta = 4.0$

- All fluences include ATLAS safety factors (1.5), Strip = 3 ab$^{-1}$, Pixel = 4 ab$^{-1}$.
- Lower left = Strip TID map, max at last disk layer is roughly 0.5 MGy (8 x $10^{14}$ 1 MeV n equivalent).
- Lower right = Pixel TID map, max in innermost layer ($r \sim 39$ mm) is ~10 MGy (1.3 x $10^{16}$ 1 MeV n equivalent) for 2 ab$^{-1}$. Must assume that inner two Pixel layers are replaceable!
Phase-2 Inner Tracker (ITk) Strip System

- Upper left = FE ASIC block diagram (binary readout, 256 ch/ASIC). Upper right = barrel module, lower left barrel “mini-stave). Lower right = strip endcap with petals.
Phase-2 Inner Tracker (ITk) Pixel Modules

- Pixel FE ASIC prototype = RD53A (400x192 pixels) – first bumped assemblies now available! Several module geometries, use mostly quad modules. Final ASIC = 400x384 pixels, ~600K channels/quad.

- Data transmission challenge:
  - FE ASIC uses 4 x 1.28 Gb/s links.
  - Innermost layer FE uses 5.12 Gb/s, outermost layer Quad uses 5.12 Gb/s
  - Use TWP + Twin-ax electrical link in tracker volume.
Phase-2 High Granularity Timing Detector (HGTD) I

- Disks covering $2.4 < \eta < 4.0$ with 2(3) hits per track for $R > 30$ cm and $R < 30$ cm.
Phase-2 High Granularity Timing Detector (HGTD) II

- Disks covering $2.4 < \eta < 4.0$ with 2(3) hits per track for $R > 30$ cm and $R < 30$ cm.

- Upper plots = ROC curves for pileup jet rejection in region covered by HGTD.
- Observe factor 5-10 additional rejection using HGTD using RPT observable (based on tracks pointing to jet, and timing compatibility with PV).

- Lower plots = b-tagging performance and light-jet mis-tag performance versus $\eta$ with and without HGTD. Factor 1.5-2 for tagging, factor 2-3 for mis-tag.
- Based on simple algorithms!
Phase-2 High Granularity Timing Detector (HGTD) III

- Disks covering $2.4 < \eta < 4.0$ with 2(3) hits per track for $R > 30$ cm and $R < 30$ cm.

- Design based on LGADs from HPK and CNM. Nominal geometry will be 15x15 array of 1.3 x 1.3 mm pixels.
- Modules made up of 2 ASICs bump-bonded to single sensor => roughly 2 x 4 cm$^2$.
- Upper right = gain versus NIEL fluence and HV bias.
- Nominal goal = gain of 10, achievable for fluence up to $\sim 3\times10^{15}$ 1 MeV n equivalent.
- Lower left = first FE ASIC prototype jitter versus charge (nominal $\sim 10$ fC from gain 10 and 50µ sensitive layer).
- Lower right = timing resolution after irradiation for both 50m and 35m devices => trade-off $\sigma(t)$ versus C ! (find timing resolution roughly constant for specific gain).
Phase-2 LAr Electronics Upgrade Overview

- Upgrade full electronics chain for phase-2 targets (no detector changes – sFCal dropped in 2016). Stream all digitized data off-detector at 40 MHz.

- On-detector electronics based on new preamp/shaper design in 65/130 nm CMOS.
- Followed by dual 14-bit 40 MHz custom ADC (both full-custom and IP-block being explored).
- Initial prototypes for preamp/shaper and ADC being evaluated, design is ongoing, converge in 2020.
- Will transmit both ADC measurements off-detector at 40 MHz. relative gains optimized to provide 16-17 bits dynamic range, covering low-$\mu$ and $\mu=200$.
- Plots indicate this combination delivers excellent performance.
- Use ~30K lpGBT links to transmit data to back-end FPGA-based processing.
Phase-2 LAr Electronics Upgrade Details

- Further details of on-detector and off-detector electronics.

- On-detector ~1500 boards, each with 22 lpGBT data links and 4 clock/control links.
- Each board handles 128 readout channels.
- Off-detector based on large FPGAs in ATCA, does signal processing (e.g. using Wiener filter with forward correction shown below using up to 24/32 samples). Very sophisticated pileup corrections, calibration, etc.

![Diagram showing the layout of on-detector and off-detector electronics](image)

- Wiener Filter with Half-Value Post-Peak
  - $x(n) \rightarrow y(n) \rightarrow E_i(n)$
  - Forward Correction

- Energy Identification

- Middle Layer, $\tau=0.025$
  - $N=8$, $\sigma_{\text{noise}}=83$ MeV, $\varphi_{\text{EC}}=0$ ns
  - Deposited Energies
  - ADC
  - WFCC

![Graph showing deposited energies and corrections](image)
Phase-2 Tile Calorimeter Upgrade Overview

- Major upgrade of on-detector mechanics and electronics

On-detector Electronics hosted inside girders at rear of TileCal.
- Today, includes LV/HV PS. Consider local vs remote HV.
- All data will be digitized on-detector at 40 MHz. Shielded location allows use of qualified COTS components.
- Shaper followed by dual 12-bit ADCs.
- Careful analysis of failures over last 10 years, improved redundancy and serviceability.
Phase-2 Tile Calorimeter Upgrade Details

- On-detector electronics is highly redundant to minimize failures.

- Detailed organization of on-detector electronics for a “super-drawer”.
- Data transmission uses 9.6 Gb/s optical links.
- Off-detector uses ATCA-based FPGA pre-processor board to process data from 8 super-drawers.
- Reconstructs and prepares data for TDAQ.
Phase-2 Muon Spectrometer Upgrade

- Muon upgrade requires replacement of all on-detector electronics. All data streamed off-detector at 40 MHz. Major upgrade of trigger capability by replacement of BI layer.

- Replace MDT in BIS with sMDT, add RPC triplet for full BI.
- Substantial improvement in trigger capability plus robustness against failures in original RPC layers.
Phase-2 Muon Spectrometer Upgrade Triggering

- Present MS has three RPC layers (below left), L1 Trigger based on RPC and TGC. Addition of fourth RPC layer (triplet not doublet) => major improvement in robustness!

Plots here assume worst-case RPC aging scenario for original chambers (only 65% single-hit efficiency).

In addition to use of fourth RPC layer, also add L0MDT, fast hardware reconstruction of tracks in MDT chambers => allows looser RPC coincidences, gives better PT precision.
Phase-2 TDAQ Upgrade Overview

- Major upgrade of TDAQ system, extending L0Calo FEXs, Muon trigger processors, and adding event-sequential Global trigger at L0 (max L0 rate = 1 MHz, latency 10 µs)
Phase-2 TDAQ Upgrade Trigger

- More detailed view of L0 Trigger showing detector object flow. Addition of Global after FEXs allows sequential rejection using full calorimeter granularity, much more sophisticated algorithms (e.g. k_T jet algorithms using topoclusters).
- Replaces present topological trigger strategy with much more sophisticated options.
Phase-2 TDAQ Upgrade DAQ and HLT

- DAQ system based on FELIX universal network-based interface for TTC and all DAQ functions. Data Handlers provide detector-specific processing, Storage Handler manages event flow to/from Event Filter trigger stage.

- Event Filter consists of HTT “co-processor” (hardware track trigger based on 28 nm AM technology for pattern finding and FPGAs for track fitting) and commodity hardware for sophisticated HLT event selection.

- HTT runs in regional mode on 1 MHz event stream => ~400 kHz output, then global HTT runs at ~100 kHz to find all tracks with PT > 1 GeV. Final output ~10 kHz.
Phase-2 TDAQ Upgrade Trigger Evolution

• Defined an “evolutionary” scheme in which all “hooks” (capabilities needed, which can only be conveniently added during phase-2 upgrade period) are implemented.

• Necessary TDAQ scaling (without requiring major new design work) can be carried out when evolving is deemed necessary (driven by physics or TDAQ/HL-LHC performance). Allows scaling L0 to 4 MHz, and adds L1 hardware track trigger using re-configuration of original HTT hardware. L1 rate ~600-800 kHz (limited by Strips).