CMS Upgrade plans
ACES Workshop, Apr. 24, 2018
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CMS Phase-2 upgrade overview

L1-Trigger/HLT/DAQ
https://cds.cern.ch/record/2283192
https://cds.cern.ch/record/2283193
- Tracks in L1-Trigger at 40 MHz for 750 kHz
  PFlow-like selection rate
- HLT output 7.5 kHz

Barrel Calorimeters
https://cds.cern.ch/record/2283187
- ECAL crystal granularity readout at 40 MHz with precise timing for e/γ at 30 GeV
- ECAL and HCAL new Back-End boards

Muon systems
https://cds.cern.ch/record/2283189
- DT & CSC new FE/BE readout
- New GEM/RPC 1.6 < η < 2.4
- Extended coverage to η ≈ 3

Calorimeter Endcap
https://cds.cern.ch/record/2293646
- Si, Scint+SiPM in Pb-W-SS
- 3D shower topology with precise timing

Tracker
https://cds.cern.ch/record/2272264
- Si-Strip and Pixels increased granularity
- Design for tracking in L1-Trigger
- Extended coverage to η ≈ 3.8

MIP Timing Detector
https://cds.cern.ch/record/2296612
- ≈ 30 ps resolution
- Barrel layer: Crystals + SiPMs
- Endcap layer: Low Gain Avalanche Diodes

TDR, interim TDR and TP references
Status of Phase-2 approvals and broad brush planning

- All upgrades have been approved by the LHCC/UCG and the CERN RB to proceed to the next step
- The funding process is proceeding and must converge in preparation of construction MoUs at the Oct. 2018 RRB
- First large orders start in 2019
Upgrade plans during LS2

Complete Phase-1 and anticipate Phase-2 to release LS3 schedule

Pixel Tracker Phase-1 revision
• Replace L1, TBM, DC-DC

Barrel ECAL Phase-2
• New chilled water feed pipe

Barrel HCAL Phase-1
• Replace rad damaged HPD by SiPM

Magnet - yoke opening - primary infrastructure Phase-2
• Cooled freewheel thyristor+power/cooling
• New opening system (telescopic jacks)
• New YE1 cable gantry
• Primary power, cooling, cableways, USC

Beam-pipe Phase-2
• Cylindrical central Be/Al + Al bellows
• Al outer with shallower cone

Near beam & Forward Systems Phase-1
• BCM/PLT refit
• New Totem track det.
• CTPPS: RP det. & moving sys upgrade

Muon Systems Phase-2
• New Cathode Strip Chamber FE electronics for inner rings of endcap (disks 1, 2, 3 & 4)
• New GEM layer in inner ring of 1st endcap disk
• Major leak repair campaign in barrel RPC (green- house gas emission targets)
• Services for Phase-2 forward chambers
Tracker design

- Outer Tracker design driven by ability to provide tracks at 40 MHz to L1-trigger
- Tilted modules in OT 3 inner layers
- Inner Tracker (pixel) design to extend coverage to $\eta \approx 3.8$

2-sensor modules concept for track-trigger

- OT Si-sensors $\approx 200\mu$m thick - 90/100$\mu$m pitch - 2.5/5cm strips - 1.5 mm macro-pixels in inner layers
- IT Si-silicon sensors $\leq 150\mu$m thickness - 50x50 to 25x100$\mu$m$^2$ - large pixels in outer layers?
Outer Tracker on-detector readout

- **Functionality:**
  CBC - MPA/SSA find clusters with programmable width - correlate top-bottom sensors (stubs) with programmable window - send stubs at 40 MHz and full data at 750 kHz to CIC for ZS and aggregation of 8 FE, buffering of 8 BX and synchronous transfer to LpGBT

- **Specifications:**
  CBC (5 cm strips): 50 ns return to baseline, 1000e⁻ noise, 0.5 mW/ch, 130 nm - SSA (2.5 cm strips): 700e⁻ noise, two level threshold to tag high charge - MPA (1.5 mm macro-pixels): 200e⁻ noise, bum-bonded to sensors, 65 nm

- CBC3 available and fully functional - final version addressing few logic issues submitted
- MPA/SSA full size chip received Dec. 2017 - fully functional going through rad. tol. test
- LpGBT expected for users in Sep. 2018 - reaching schedule critical path
- DC-DC powering - issues observed with Phase-1 pixel detectors still to be understood
- Hybrids, 3 potential vendors - warpage and delamination issues - new order this month

D. Ceresa’s presentation
Inner Tracker on-detector readout

ASIC chip developed by RD53 collaboration for both ATLAS and CMS pixel detectors

- 50x50m² pixel size
- Larger chips
- Hit rates up ≈ 2-3 GHz/cm²
- Rad. Tol. to 1 Grad, ≥ 10¹⁶ n/cm²
- Rate/latency 1 MHz/≥ 10 µs
- Low power budget ≲ 1 W/cm²
- Low noise ≈ 1000 e⁻

- Aug. 31, 2017: Submission
- Dec. 6, 2017: First chip test
- Mar. 15, 2018: 25 wafers ordered
- Apr. 13, 2018: First bump-bonded chip test

- Good news from initial tests on all aspects, minor issues seem understood
- Was on critical path for radiation tolerance qualification of pixel sensors - will also allow progress for serial powering system test
- Final chip size is driven by IT design, also few other readout differences compared to ATLAS

F. Lodo’s presentation
Tracker off-detector electronics

- **DTC boards** to route trigger and data flows to DAQ - two variant for OT and IT also include some specific features for luminosity monitoring at 75 kHz
- **L1-TrackFinder** boards implementing pattern recognition and track cleaning and fitting in FPGAs (Hough transform or Tracklet propagation)

**Common infrastructures for HW, FW, SW**
- Few existing systems to develop future hardware platform
- Target first prototype 10/2019
- Final prototype 09/2020

**Power Supply Systems baseline similar to current** - investigating option with commercial 12 V PS in lower radiation and field area below CMS to save cost (also for other systems)
Barrel Calorimeters upgrade

- Crystal granularity readout at 40 MHz
  - VFE 20 ns peaking time, 160 MHz sampling for rejection of spurious interactions and 30 ps resolution 30 GeV e/γ showers
  - FE with IpGBT at 10 Gbps
  - LV boards implementing DC/DC conversion
- Operation at 9° to mitigate APD aging
- New ATCA backend boards for EB and HB
Barrel Electromagnetic Calorimeter on-detector readout

- **EB Very Front End (VFE)**
  - TIA concept demonstrated with FPGA demonstrator and V0-ASIC
  - CATIA FE ASIC with full features in final design for TSMC 130 nm MPW Jun. 2018
  - ADC IP block now purchased after contract negotiations
  - LiTE-DTU ASIC combines ADC with custom Data Transfer Unit (DTU) in 65 nm - MPW submission foreseen Nov. 2018

- **EB Front End (FE) board** (on detector link board with IpGBT (9.6Gbps))
  - FE demonstrator in Apr. 2018 H4 test beam
  - FE prototype 1 with GBTx (4.8 Gb/s) now in production
Barrel Electromagnetic Calorimeter off-detector electronics

- **EB/HB Processor (BCP)** (data/trigger concentration and clock and control)
  - Demonstrator specification completed for production during summer
  - HB demonstrator chain (HB Phase 1 on-detector electronics + calo trigger board)
    - Hardware assembled Q1 2018
    - Build firmware for HB to prepare for BCP Q2/Q3 2018

![Diagram of BCP board 2x16 Gbps FPGAs Ultrascale](image1)

![Diagram of BCP demonstrator](image2)
The Phase-2 Upgrade of the CMS Endcap Calorimeter
Technical Design Report

https://cds.cern.ch/record/2293646
Calorimeter Endcap design

3D shower topology and time resolution of ~ 30 ps (Pt > few GeV)

- **Calorimeter Endcap Electromagnetic (CE-E)**
  - 28 layers of Silicon sensors in W/Pb absorber (25 $X_0$ - 1.7 $\lambda$)
- **Calorimeter Endcap Hadronic (CE-H)**
  - 24 layers: 8 silicon + 16 silicon/scint. tiles at high/low $\eta$ in stainless steel absorber (9 $\lambda$)
Calorimeter Endcap on-detector electronics

- HGROC1 several block variants - received Dec. 2017 - tests on-going
- HGROC DV1 with full digital functionality submission mid-2018 - schedule critical path

P.M. Rubinov’s presentation

**HGROC**
- 20 ps peaking time, 2500e⁻ noise, 20mW/ch, ± input polarities
- Current conveyor for Scint+SiPM
- 10 bits ADC 0.2-100fC - 12 bits ToT 50fC - 1pC - linearity 10%
- Time measurement 10 bits TDC
- Data Buffer 12.5 us - Zero suppression < 0.5MIP
- 130 nm TSMC - TID 150 Mrad

![Diagram](image)

Low voltage supply
Final specs Q2 2019
Prototype tested by Q2 2020
Calorimeter Endcap off-detector electronics

Use generic baseboard for DAQ and Trigger Primitive Generation

- **DAQ boards** use both interposer (daughter board)
  - One (relatively) cheap FPGA/interposer
  - 96 FO pairs per board to/from FE
  - 12 FO pairs/board to/from central DAQ

- **TPG boards** use only one interposer
  - One high-end FPGA
  - Up to 96 FO pairs in/out per board for TPG data transmission
  - 2 FO pairs/board to/from central DAQ

- **Baseboard and DAQ daughterboard:**
  - Prototype PCBs submitted for fabrication - expected in Q1 2018
The Phase-2 Upgrade of the CMS Muon Detectors
TECHNICAL DESIGN REPORT

https://cds.cern.ch/record/2283189
Muon system upgrades

- Drift Tubes barrel chambers: 40 MHz readout with improved z/t-precision
- Resistive Plate Chambers barrel: readout with improved t-precision
- Cathod Strip Chambers Endcap: readout with higher bandwidth and latency in ME234/1 using current ME1 and replace ME1 with higher rad. tol. components
- New stations: GEM1-2, iRPC3-4, 1.6 ≤ η ≤ 2.4, GEM0 extended coverage 1.15 ≤ η ≤ 3
Drift Tubes electronics upgrades

- **New OBDT minicrates**
  - Concept validate with demonstrator
  - 4 FPGA - 64 ch TDC 1 ns sampling - Microsemi PolarFile (SEU robust) - lpGBT 10 Gbps
  - Prototype design being finalized - production in summer - sector test installed in LS2

- Back-End boards common development with L1-Trigger
Cathod Strip Chambers electronic upgrades

- **Installation during LS2**
  - DCFEB2 (cathod) similar upgrade as LS1, new VTTr/x, PROM - final prototype delivery in 2 months
  - ALCT (anod) more OL, final prototype test almost completed
  - LVDB final prototype test almost completed
  - OTMB (trigger board) and HV upgrade on schedule

- **Installation during LS3**
  - ODMB - Artix-7 FPGA
  - BE board common development with L1-Trigger
Resistive Plate Chambers electronics upgrade

- **New off detector link and control boards for barrel RPCs**
  - FPGA (Virtex 7) replaces ASIC - 640 MHz clock for 1.5 ns time resolution - lpGBT 10 Gbps to BE
  - First prototype board ready to receive GBT

- **iRPC readout**
  - Readout both sides of strips for improved radial resolution through time measurement
  - RPCROC ASIC based on existing PETIROC - final implementation in TSMC 130 nm
  - TDC implemented in FPGA for 50-100 ps resolution - GBT to BE electronics
  - Prototype validation this summer
GEM chambers electronic upgrade

- FE based on VFAT3 ASIC developed for GEM1 Chambers (installation during LS2)
- GEBs route signals to Opto-Hybrid with lpGBT 10 Gbps to BE
- BE boards common development with L1-Trigger

Back-end will use ATCA board, R&D with CTP7
TECHNICAL PROPOSAL FOR A MIP TIMING DETECTOR IN THE CMS EXPERIMENT PHASE 2 UPGRADE

https://cds.cern.ch/record/2296612
MIP Timing Detector: ~ 30 ps resolution Time of Flight measurement

**MTD design overview**

- Thin layer between tracker and calorimeters
- MIP sensitivity with time resolution of ~30 ps
- Hermetic coverage for |η|<3

- **Barrel Timing Layer installed in the Tracker Support Tube**
  - Lyso Crystals 11x11mm² + SiPM 4x4mm², ~250k channels, 40m²

- **Endcap Timing Layer in front of Calorimeter Endcap**
  - Silicon LGAD 1x3mm² pads, ~250k ch, 12 m²

L. Grey’s presentation
MIP Timing Detector electronics

❖ **Barrel Timing Layer**
- TOFHIR FE based on TOFPET2 target ≤ 20 ps resolution, 4-TAC, 10 bit ADC, 20 mW/ch
  - Submission in UMC technology this summer
  - Radiation tolerant version in TSCMC 130 nm this fall
- lpGBT 10 Gpbs to BE

Test beam with TOFPET2 chip achieved ≃ 30 ps resolution

❖ **Endcap Timing Layer**
- FE TSMC 65nm, based on TOFFEE, TT-PET, use experience of RD53
  - Matrix of 4x24 LGAD pixel (3.125 x 1.042 mm²) → ~25 x 12.5 mm² ASIC
  - 8 bit ADC - TDC with 20ps binning
  - 3mW/ch, 12.5 µs storing capability
  - Submission of analog and digital prototypes end of this year
- Concentrator chip based on Calorimeter Endcap design

❖ **BE boards** common with other systems - Barrel calorimeters or other
Precise Clock distribution for Calorimeters and MTD

- Target ≈ 10 ps resolution - two path investigated
  - Through BE boards and GBT or Through additional OL directly to FE

- On going tests of resolution through BE - FE path - single/multiple channel(s) and crates
  - Encouraging results need IpGBT to confirm by spring next year
  - Calibration/monitoring system needed
The Phase-2 Upgrade of the CMS Level-1 Trigger
Interim Technical Design Report
CMS Collaboration

The Phase-2 Upgrade of the CMS DAQ
Interim Technical Design Report
CMS Collaboration

https://cds.cern.ch/record/2283192

https://cds.cern.ch/record/2283193
L1-Trigger upgrade

- Tracks in trigger at 40 MHz
- \( \geq 50 \) Tbps input
- 12.5 \( \mu \)s latency
- Accept rate 500/750 kHz at 140/200 PU

- ATCA two types of boards being investigated in UK and US
  - 60 or 96 I/O, 16-25Gb/s optics
  - 3 Xilinx KU115, or 1 VU9P FPGA - implementation on interposers
  - Embedded Linux (COM Express, Zynq), IPMC (CERN)
  - First prototypes foreseen Q3 2018

- Algorithms integrated into L1 emulator sequence
  - Including EC trigger primitives, L1 tracks, PFlow for track candidates

- Initial FW implementation of PFlow algorithms in demonstrators
  - Use 30% of LUTs- Work starting on Machine Learning implementation
**DAQ/HLT upgrade**

- New TCDS high speed serial distribution of precise clock and multiple triggers data steam
- Systems interface with DTH ATCA boards
- HLT output at 7.5 kHz, 4.5 MHS06 for 500 kHz (140 PU) in LS3 plus 4.7 MHS06 for 750 kHz (200 PU) staged to LS4

- **ATCA DTH (Daq and TCDS Hub)**
  - 16 inputs up to 25 Gbps, output: 4 x 100 Gps Ethernet
  - Modular board to optimize cost versus needs
    - DTH-400 - 1 TCDS module - 1 DAQ module (16 duplex lanes)
    - DTH-1200 - 1 TCDS module - 3 DAQ module (48 duplex lanes)

- 1st prototype Q4 2018
Summary

- CMS phase-2 upgrades have been approved recently by LHCC/UCG and CERN RB
  - L1-Trigger, DAQ/HLT and MIP Timing Detector TDRs still to come
- Funding agreement expected at Oct. 2018 RRB to proceed with production MoUs
- Several progress in developing electronic systems
  - FE ASICS
    - MPA/SSA and RD53A 65 nm success indicate that only 2 iterations toward final chip submissions is achievable
    - RD53A will allow to proceed with Pixel sensors R&D and serial power system test, interesting to clarify soon rad. tol. beyond 500 Mrad, discussion with LHCC in May to plan final chips
    - DC/DC FEAST issue observed with Phase-1 pixel is still to be understood - in situ test of systems are important where possible
    - IpGBT availability is critical for most systems to proceed with system tests
  - Optical modules have substantial cost, production approach needs attention
  - Back-End boards approach is to have common hardware platforms to minimize maintenance effort, but adapted to cost versus performance needs and allowing compatibility for different FPGA implementation (cost optimization with quantities)
  - Power Supplies baseline based on legacy systems, but also investigation of conventional commercial systems for cost saving