LHCb Upgrade

.....from the point-of-view of electronics

on behalf of the LHCb collaboration

Many thanks to all my colleagues who provided material

Outline

Reminder of Electronics Architecture

Review of electronics status
- Sub-detector specific
- Common projects

Outlook to installation

Upgrade philosophy

Remove existing L0 hardware trigger (1 MHz)

Read out all detector data from all BXs @ 40 MHz

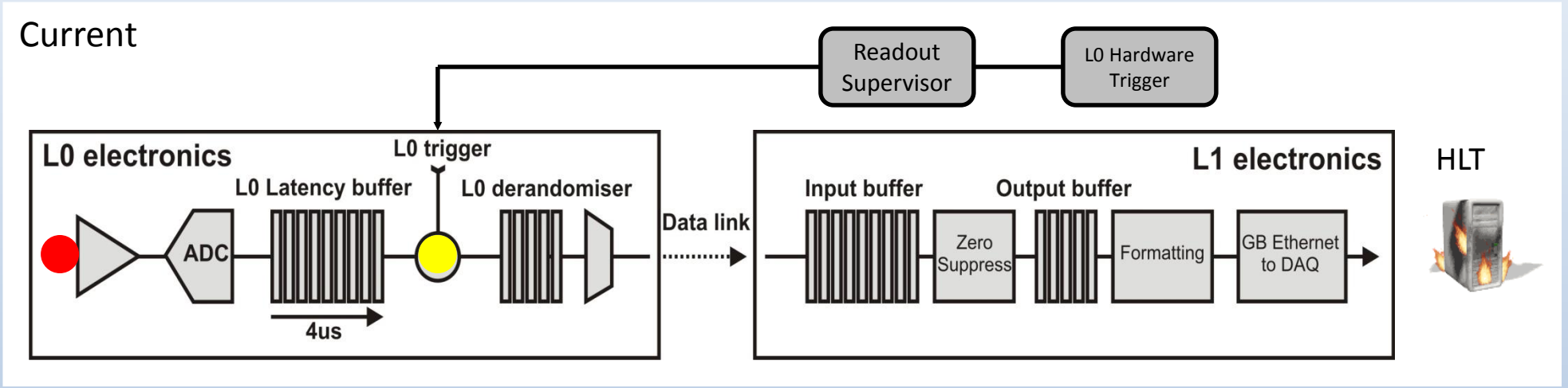
Triggering is 100% in software running in PC farm

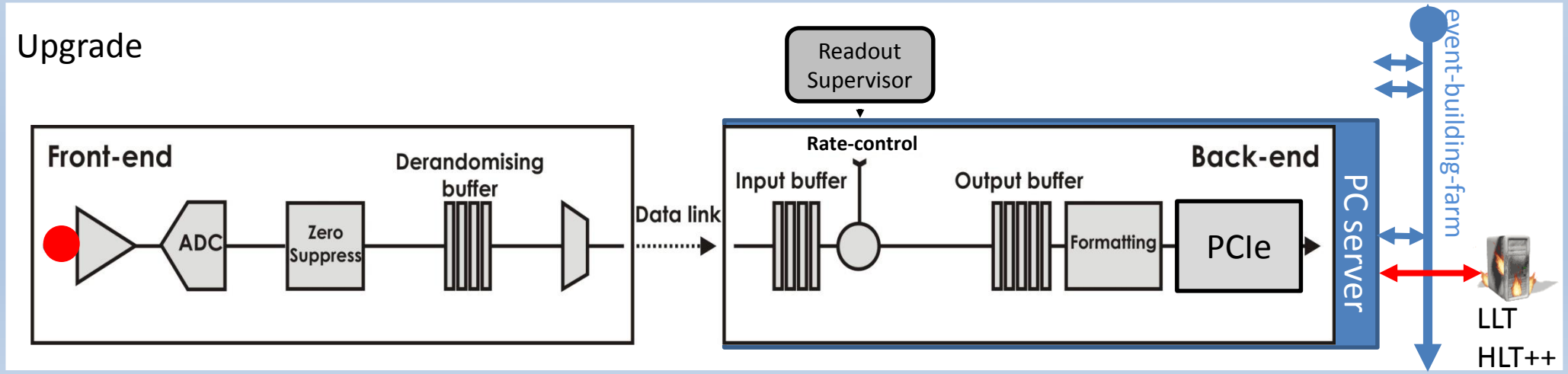
⇒ New electronics & DAQ

Upgrade installation in LS2

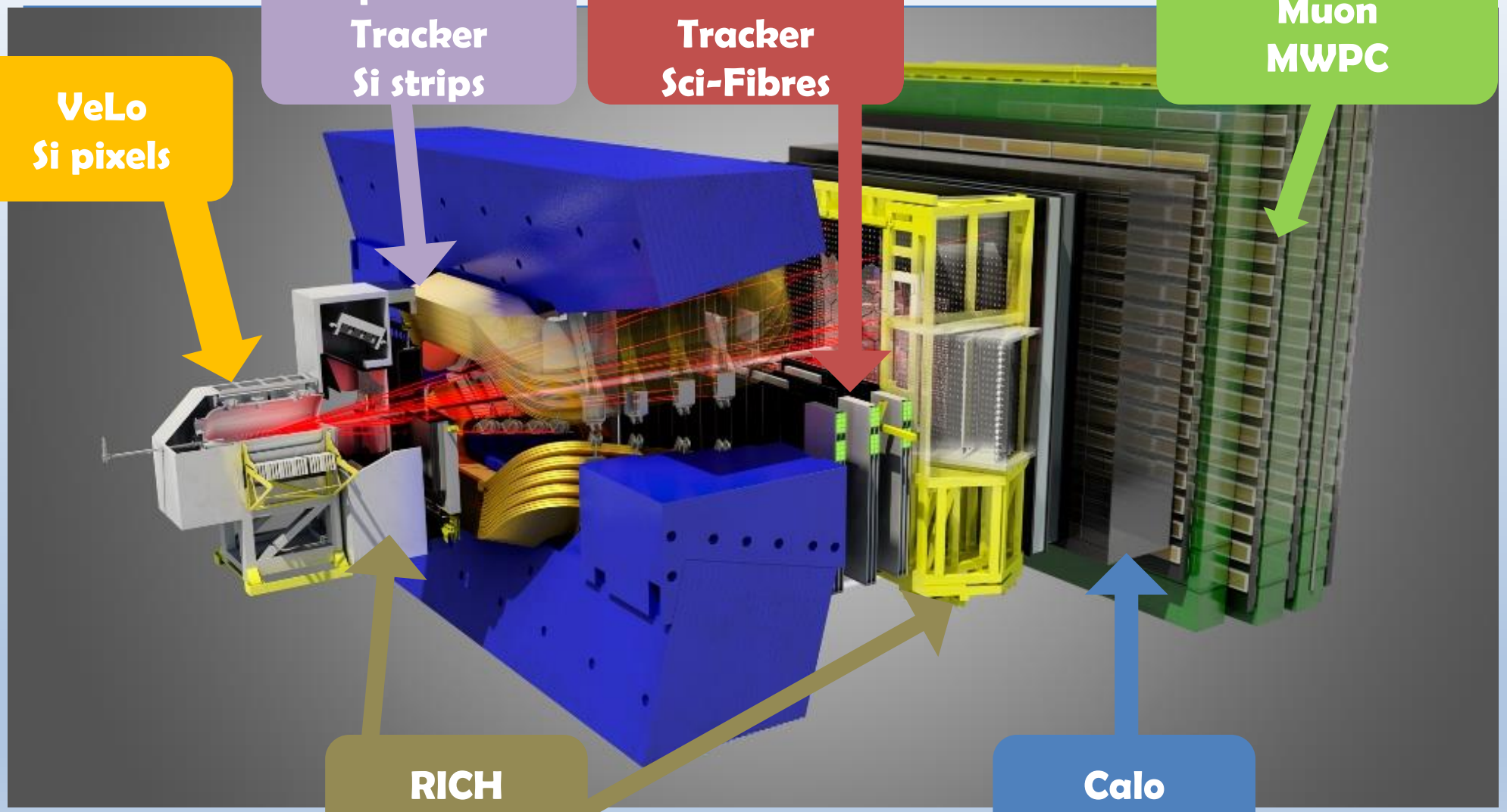
Upgrade architecture

No 'front-end' trigger, Event rate to DAQ nominally 40 MHz





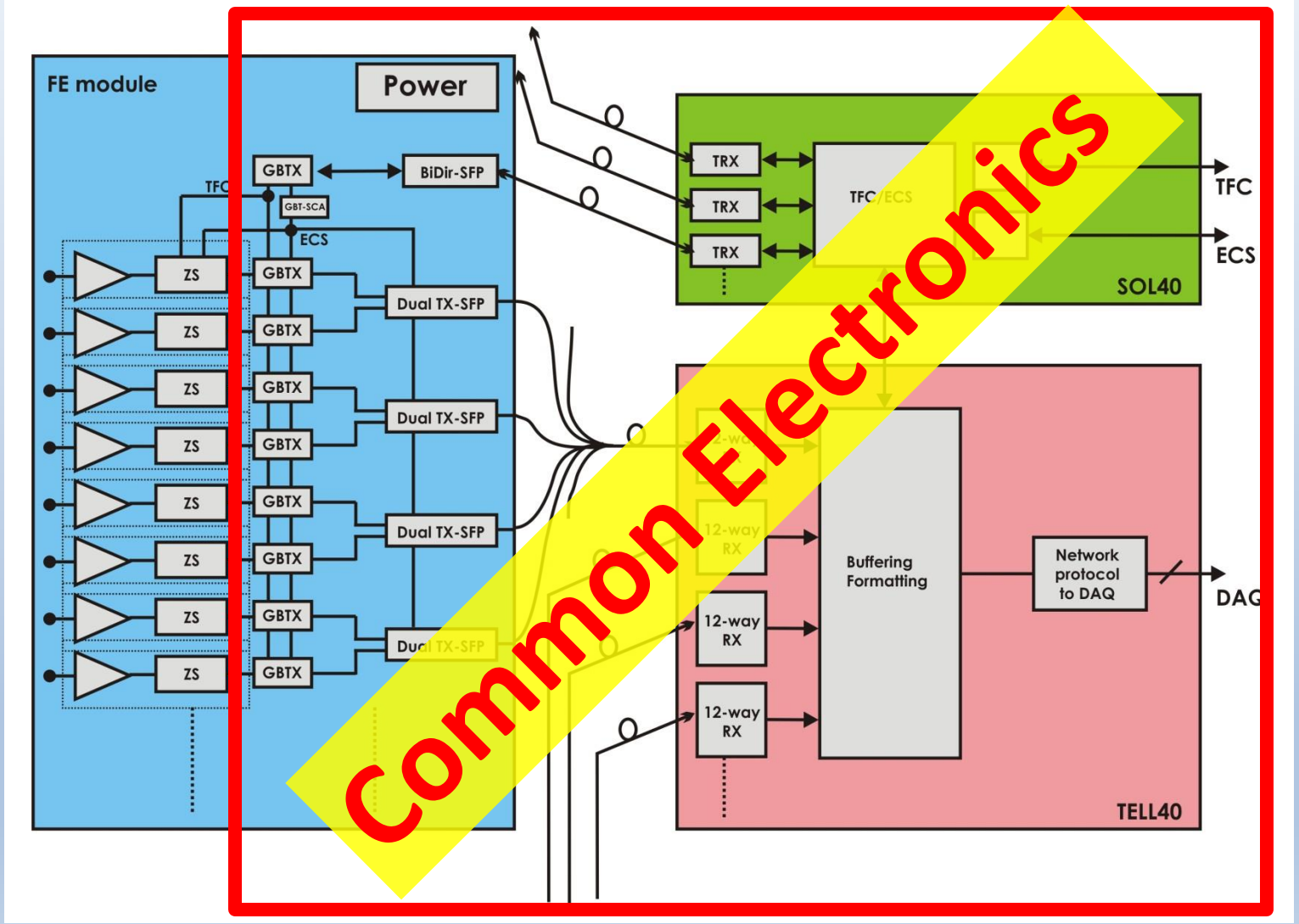
LHCb after 2020



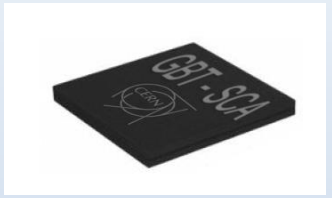
Review of electronics status

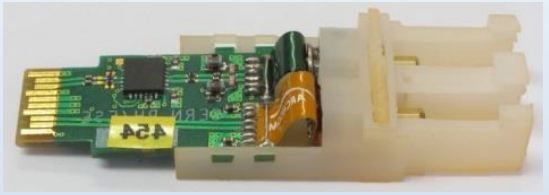
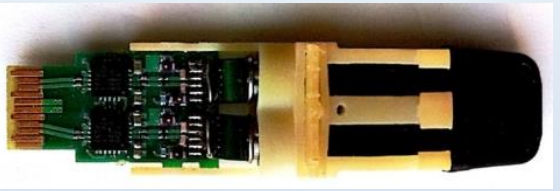
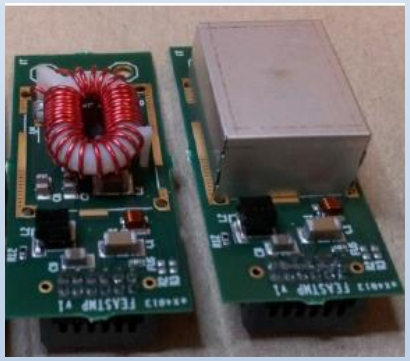
(non-exhaustive)

Generic Implementation



Common front-end components


GBTX
GBT-SCA
VTRX (incl GBTIA + GBLD)
VTTX (incl GBLD)
FEASTMP
VLDB

A huge thank you to the teams for the many man-years of development

And to the management for the 'White Paper' R&D funding starting 2007

The LHCb upgrade would not be possible without this effort

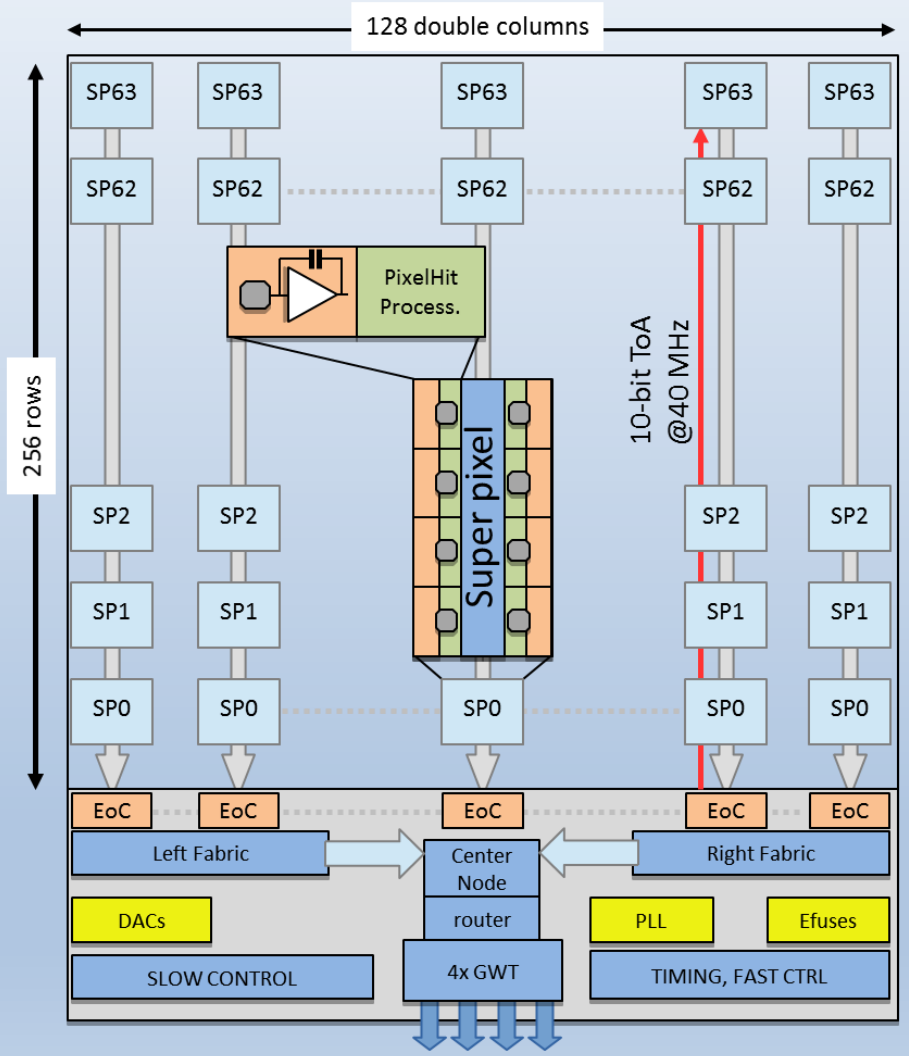
Some words on ASIC technologies

Although not without problems, we have benefited hugely from changing 130nm CMOS technology in 2014

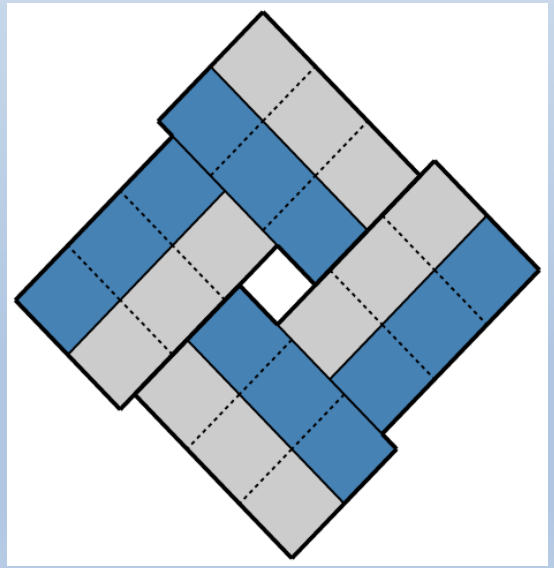
- Fast & reliable turnaround
- Financial savings (& Multi-Layer-Mask option)
- Generous wafer quantities from Engineering Runs
- Sharing of blocks
- Good & stable radiation performance

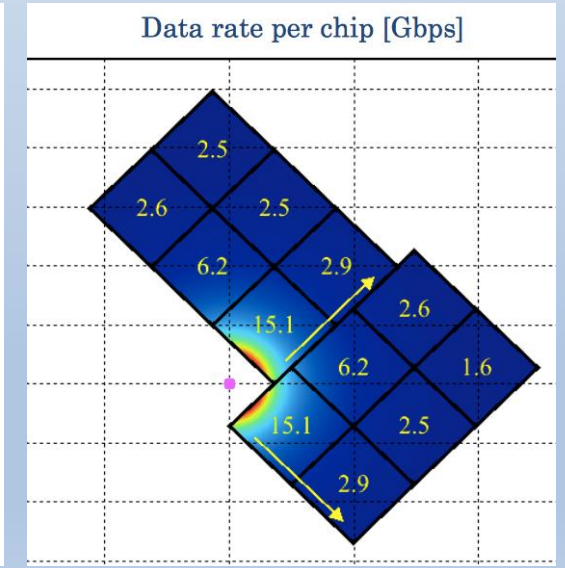
Many thanks for the 'technology support' from CERN

VeLo (Si pixels)



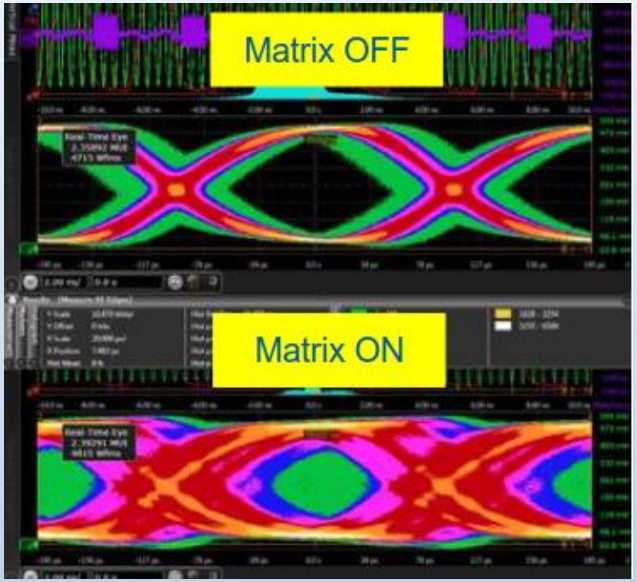
VeloPix readout chip
Big challenge: high data rate





4 x 5.12 Gbps

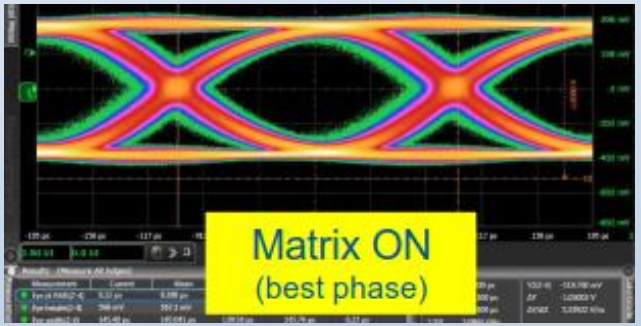
Version 1 worked beautifully….
except for two interesting problems



Power-integrity problem:

Supply noise creates excessive jitter on internal reference clock

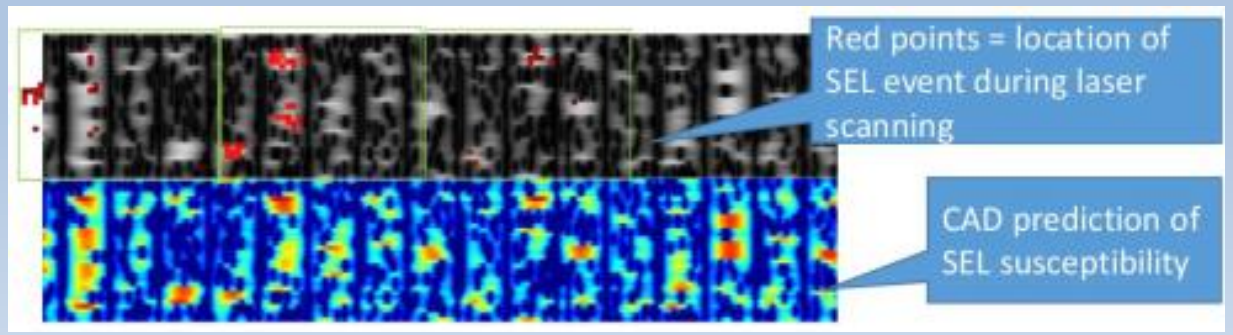
Version 2

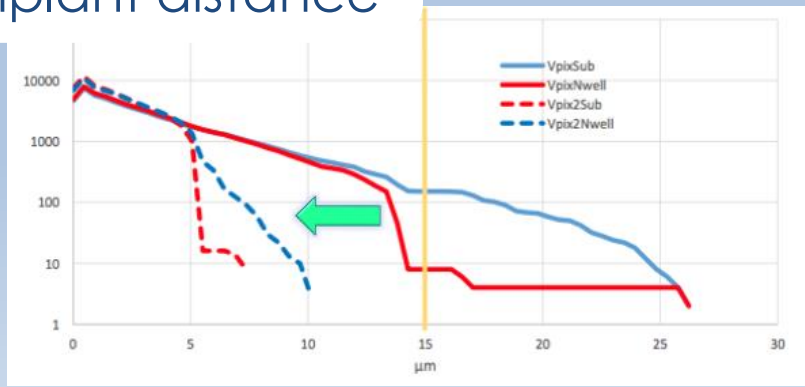


Single-event latch-up (30mA current increases)

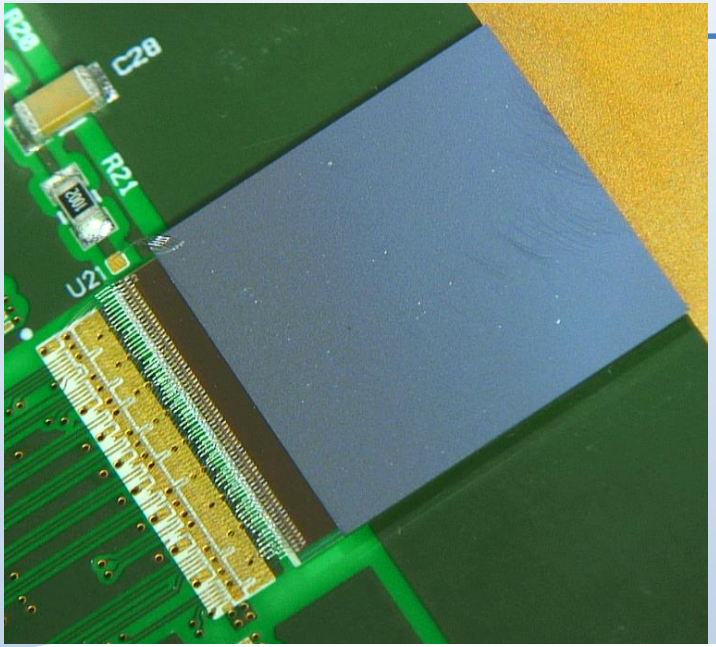
Observed with heavy-ions, confirmed with laser scanning

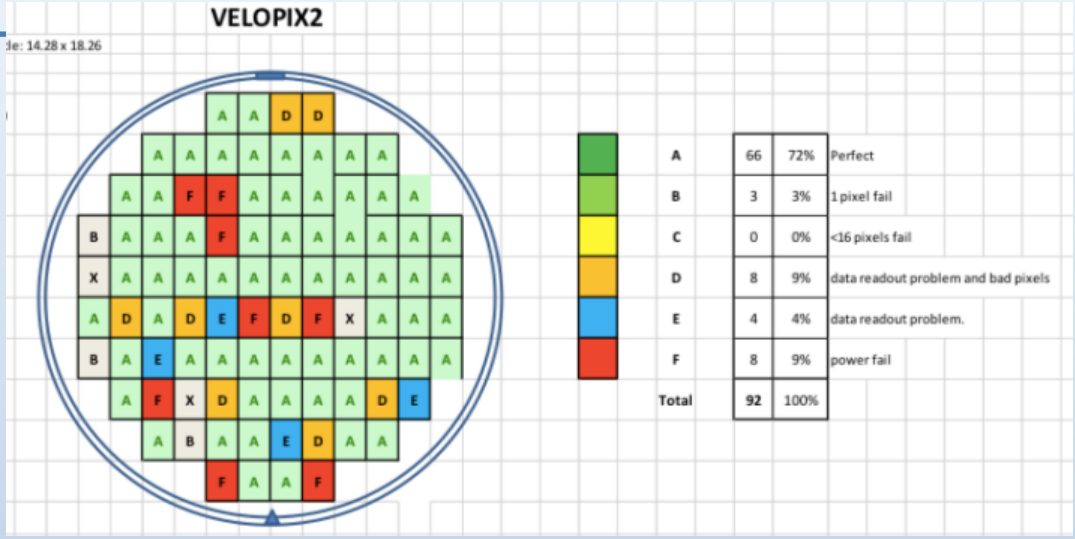
Analysed in layout as function of well/sub-to-implant distance





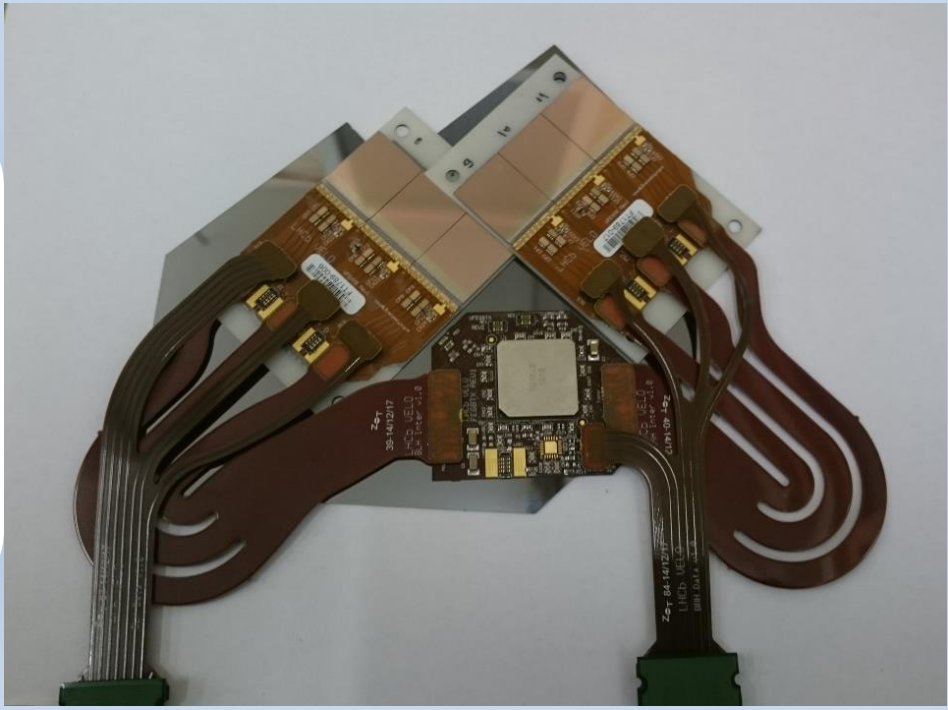
Production started





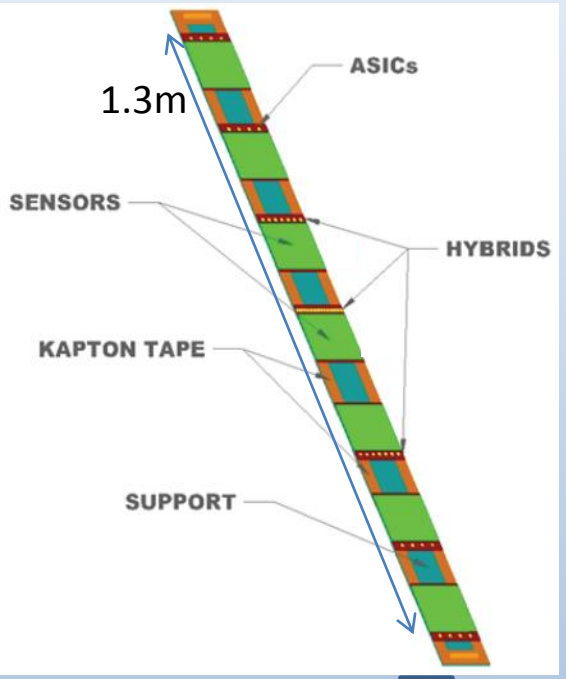
Wafer-probing => bump-bonding

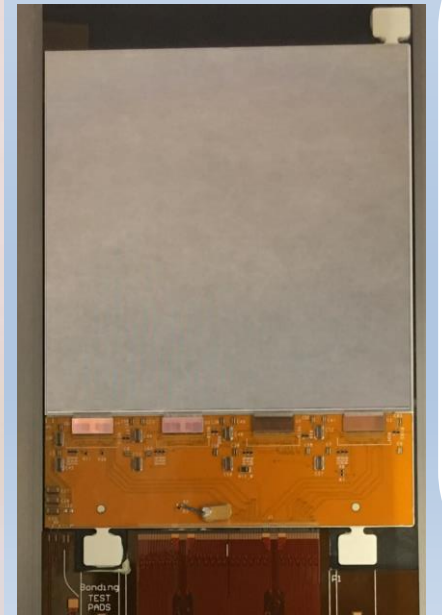
Pre-production of:
hybrids,
data-flex,
power-distribution



Upstream Tracker (Si strips)

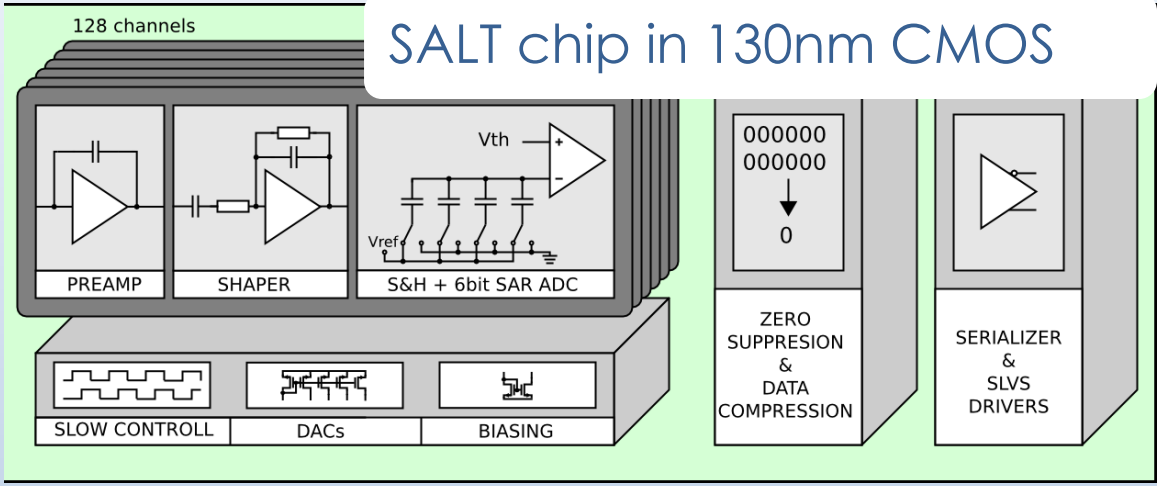
4 planes of 16 staves





Proto tapes
& modules

SALT chip in 130nm CMOS

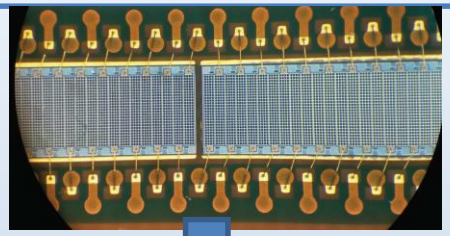


SALT:
Fighting parasitic effects:
New version under test

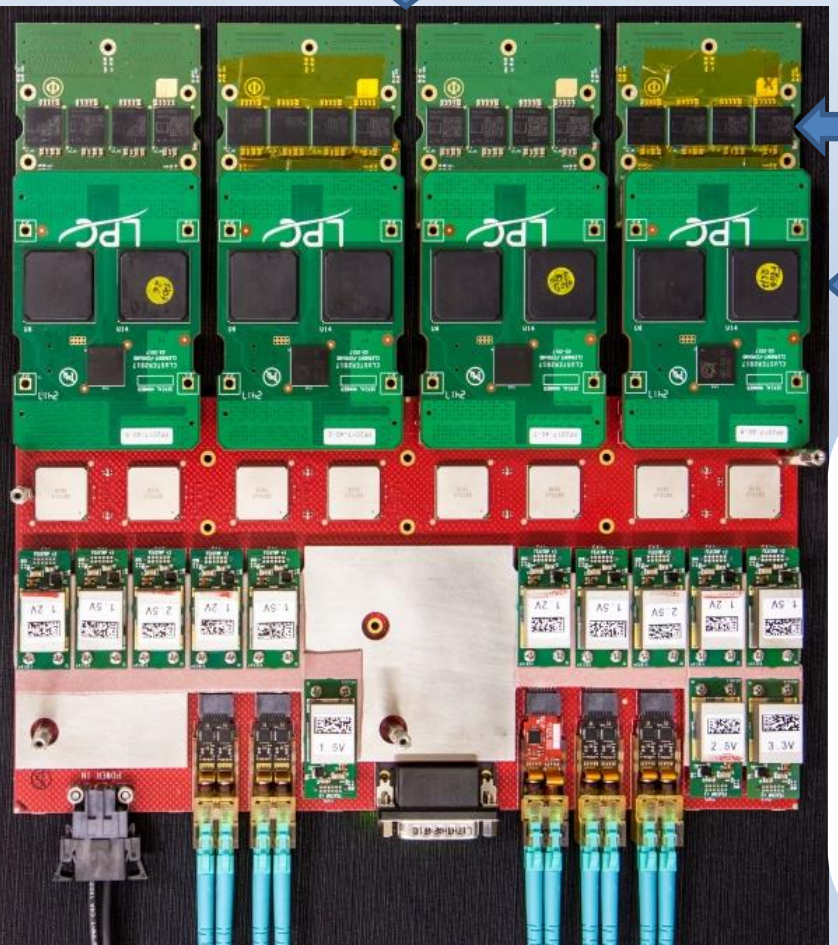
Other parts:
- Hybrids
- Flex tapes
- Data TX boards

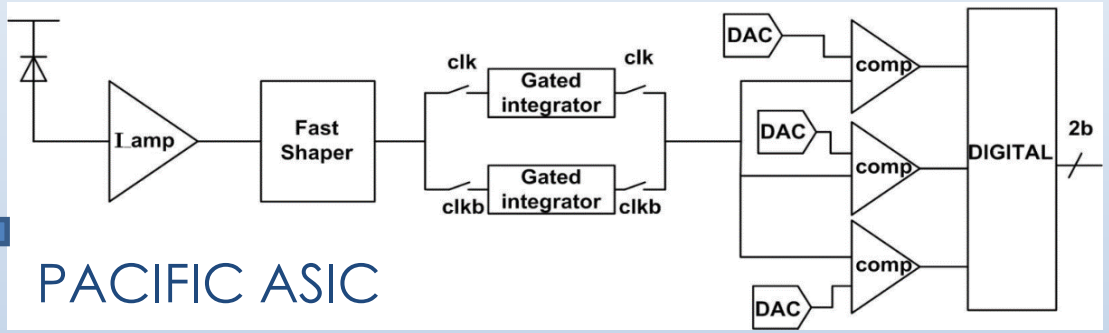
All tendering for production

SciFi Tracker (SiPMs)



SiPM arrays coupled to fibres, 250um pitch





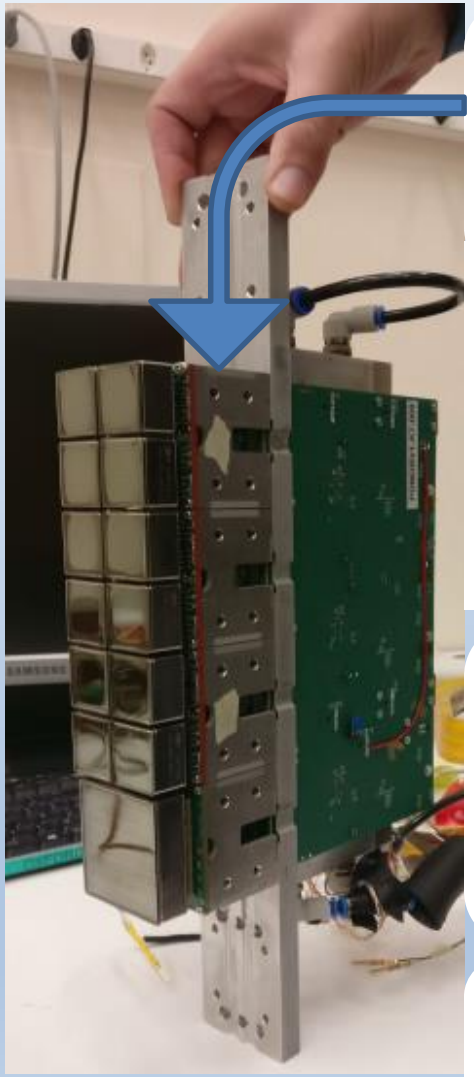
PACIFIC ASIC

IGLOO2 flash FPGA, forms clusters

Radiation tested at CHARM (mixed field)

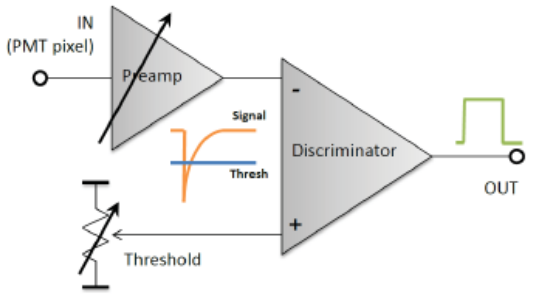
- SEUs corrected by TMR
- No SELs
- No change in power consumption
- Speed degradation as predicted (not critical)
- Lose programmability quite early (~ 20 Gy)

RICH (MAPMTs)

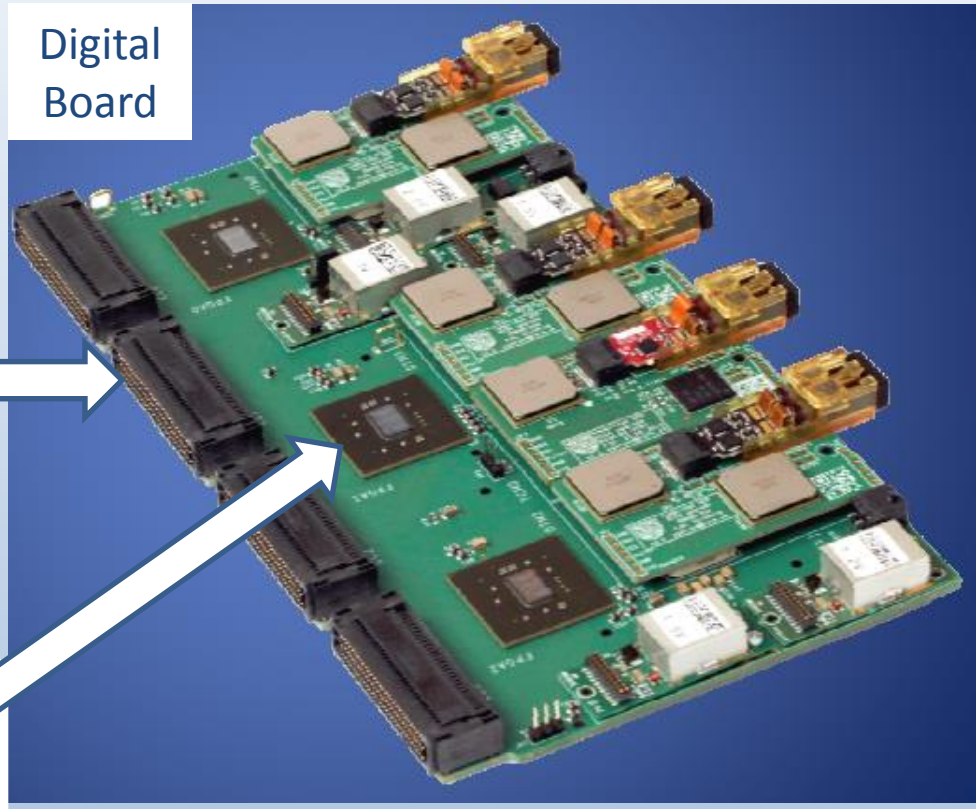


CLARO ASIC

SEL issue resolved by using hardened cells



Digital Board

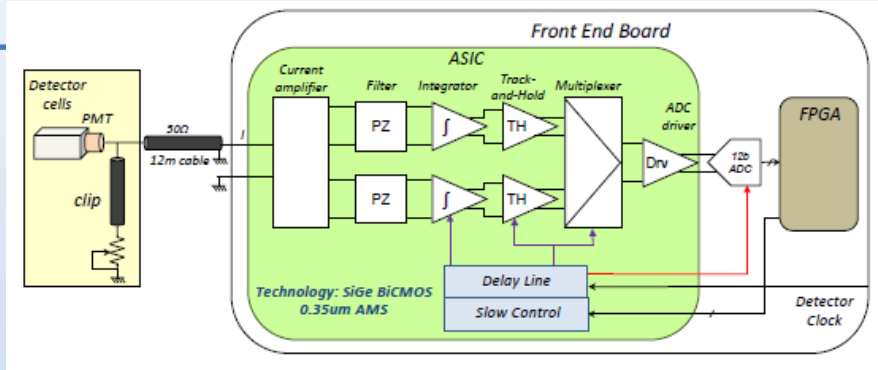


Baseline:
Kintex7 SRAM FPGA
Performed well in CHARM irradiation

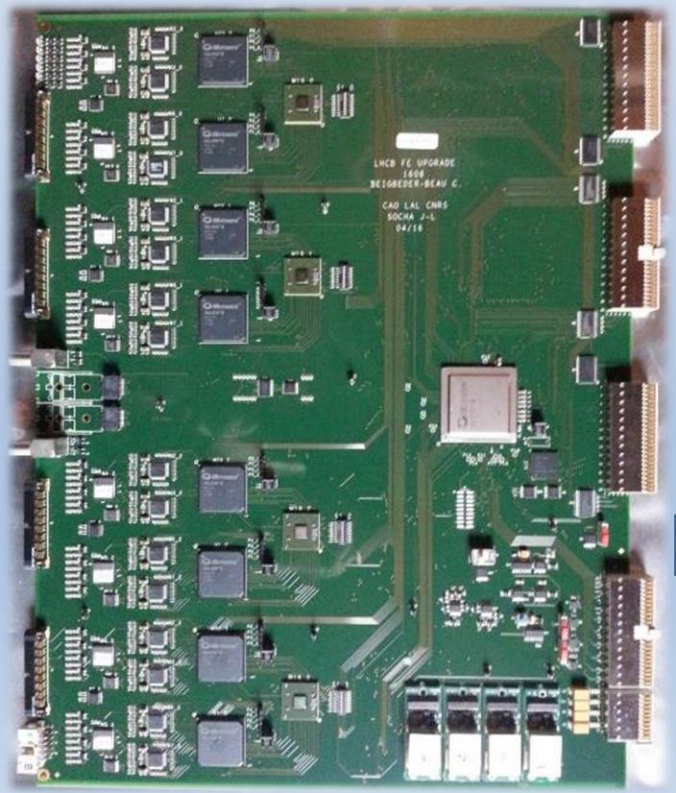
Antifuse device under study as back-up
Mezzanine approach to safeguard special components

Calorimeter (PMTs)

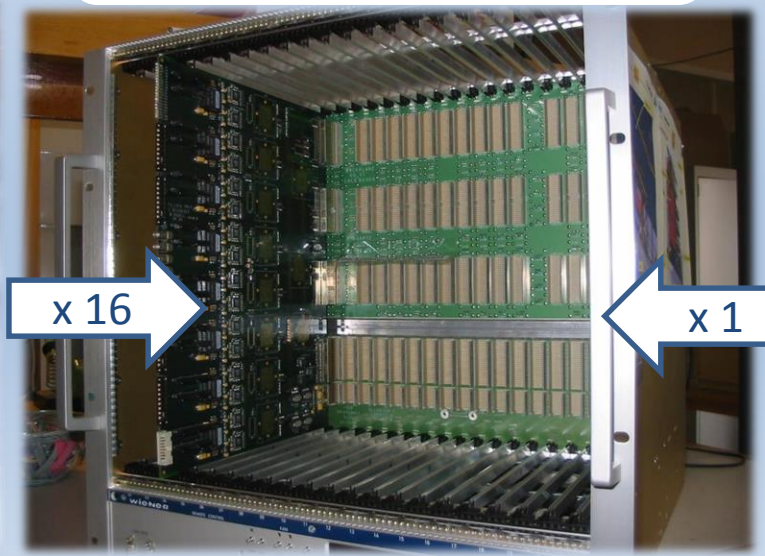
ICECAL ASIC
Production testing ongoing



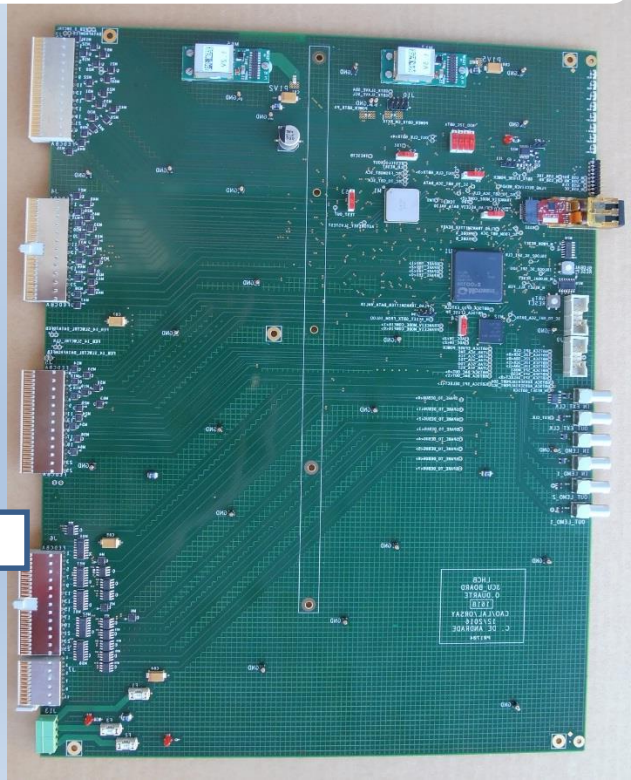
FEB: data TX
IGLOO2 flash FPGAs



eLinks connect via crate backplane



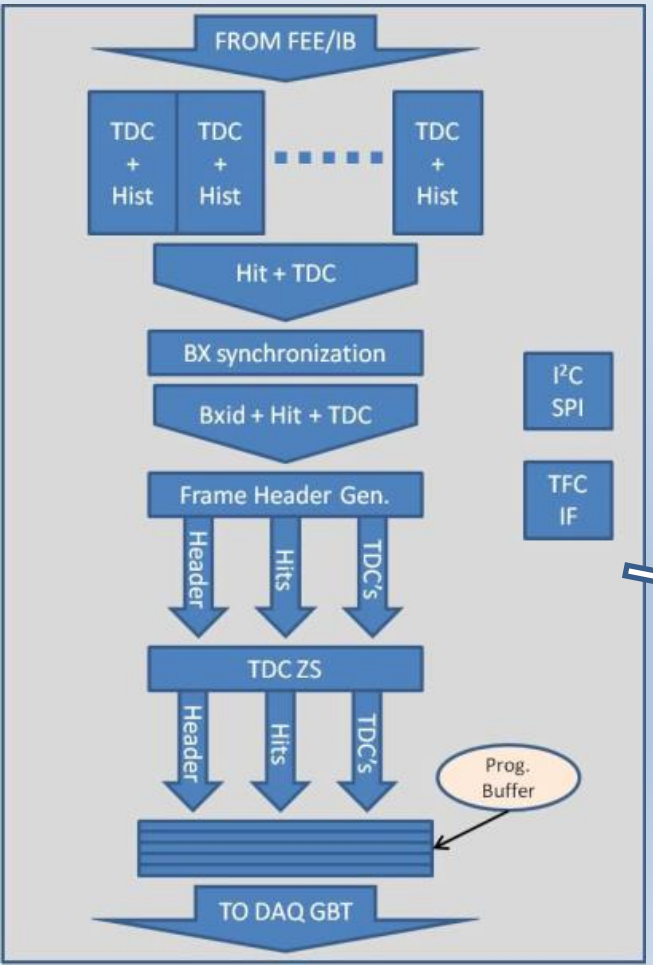
3CU: fast/slow control



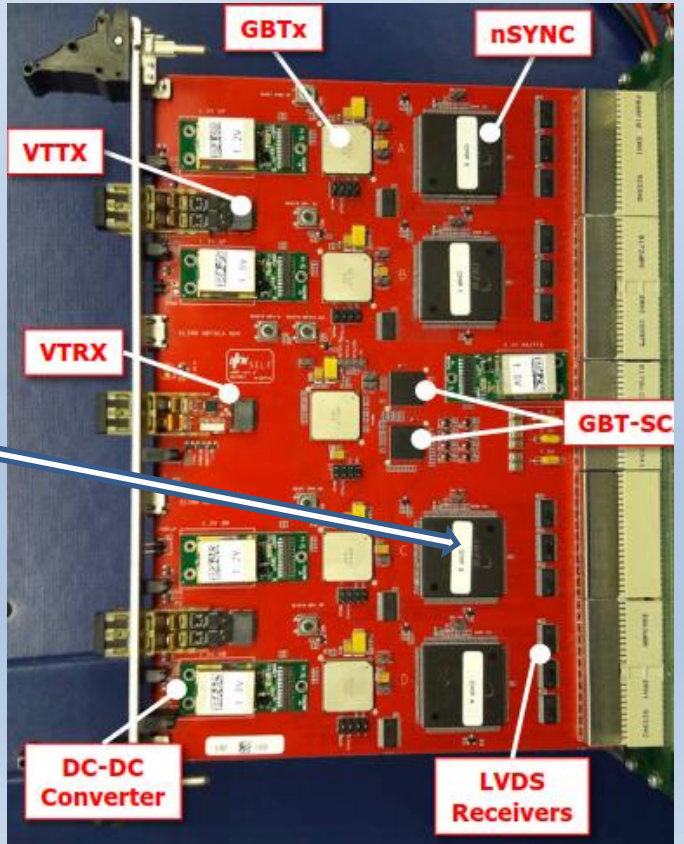
Muons (MWPCs)

Re-use front-end ASICs on chambers

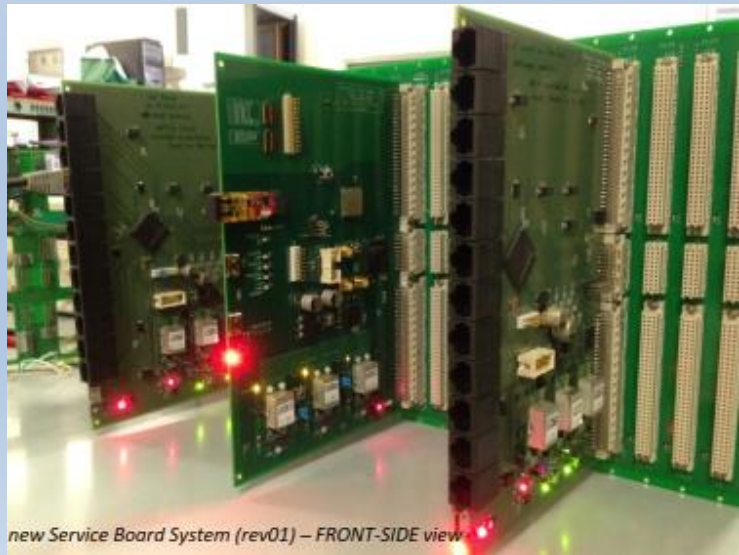
New TDC ASIC: fully digital, 1.56 ns resolution
In production now



New readout modules



New control & calibration modules
Based on IGLOO2



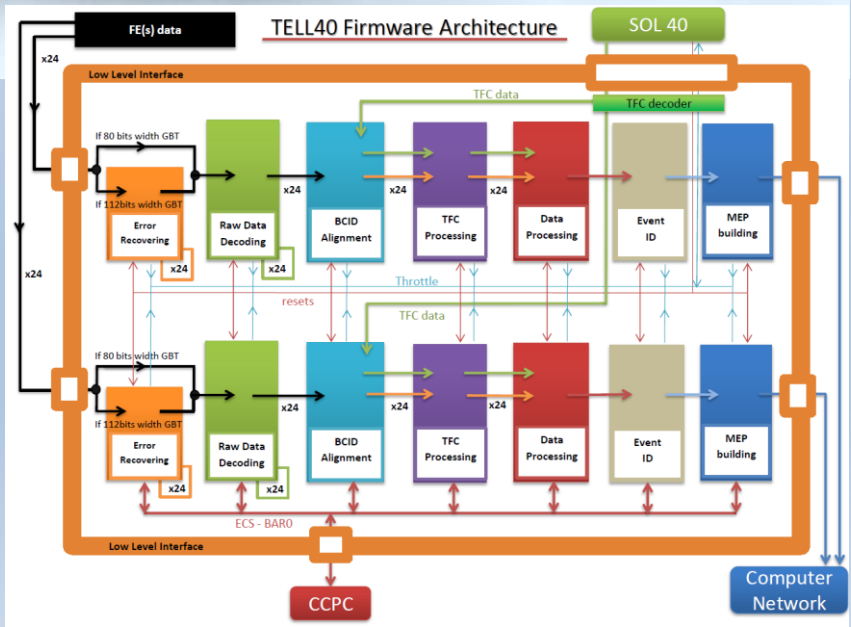
Common module for data readout & controls: PCIe40

Challenges:
new & complex FPGA, power & cooling

Production of ~ 670 modules starting now

See talk by J-P. Cachemiche on Wednesday

Different firmware recipes
Centrally coordinated architecture
+
custom blocks per sub-system

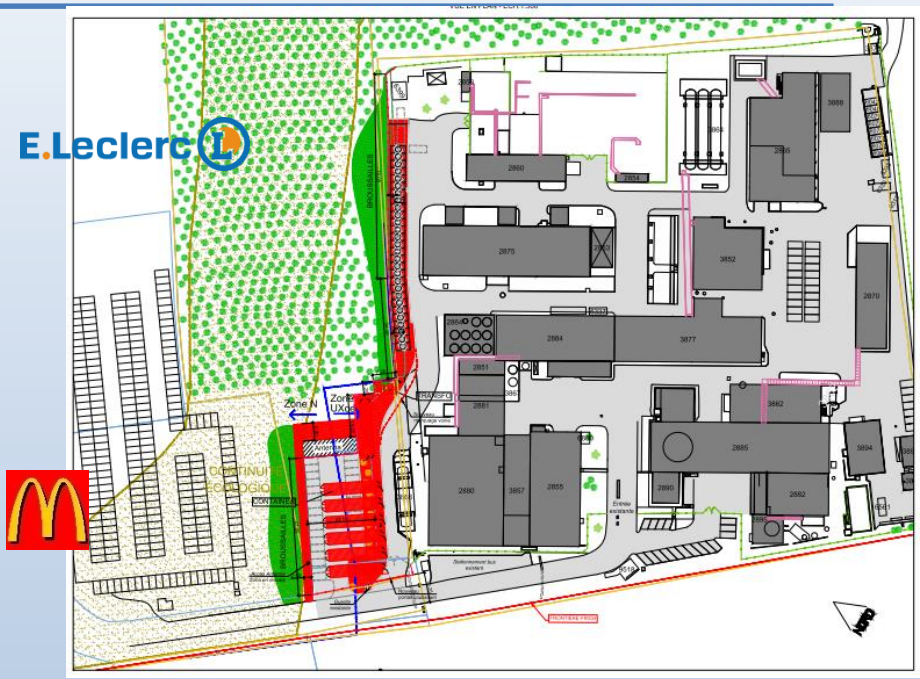


Infrastructure

Farm of PC servers in data-centre on surface (ordered).

350m optical fibres bringing data up from cavern (tendering now).

Long-term BER testing continuing successfully.



Re-use existing power supplies
(hoping for maintenance contract to continue.....)
Re-use existing cabling (minimal additions)
Re-use rack infrastucture

Conclusions

Sub-detectors implemented global architecture

Heavy use of GBT, VL & DC-DC developments

Most ASICs & front-end modules in production

Widespread use of FPGAs in front-ends

Infrastructure in preparation

On target for LS2.....

Discussion started on further upgrades

Back-ups

Motivation for upgrade

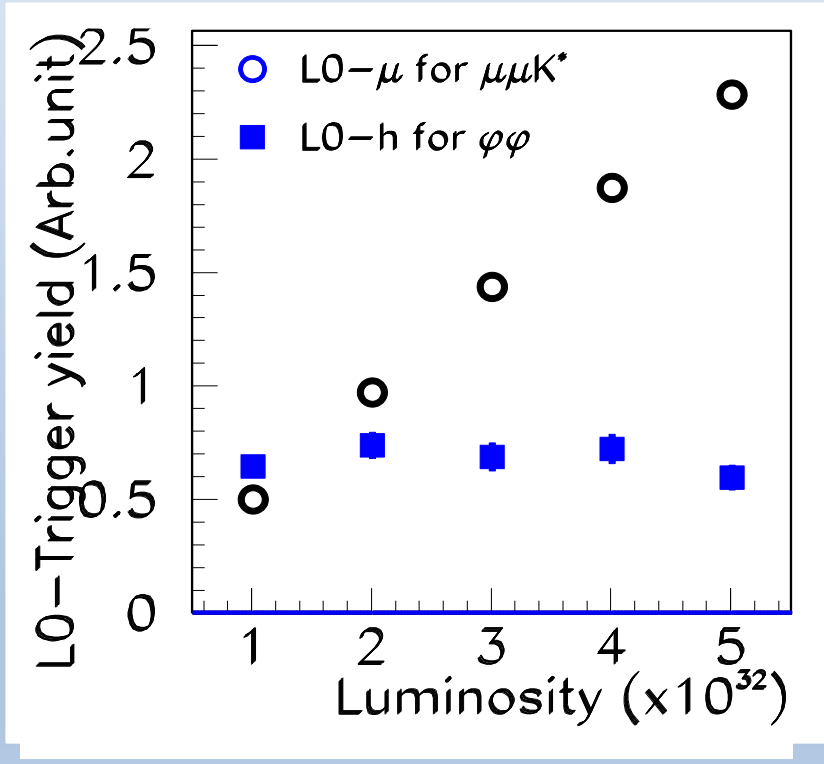
At L = 2(+) x 10^{32} $cm^{-2}s^{-1}$,
beyond 5 fb^{-1}, statistics don't improve much

Big statistical improvement if:

- increase L to 2 x 10^{33}, AND
- improve efficiency of trigger algorithms

BUT ..... with current L0 trigger:

rate & latency limited by electronics
(1 MHz, 4 μs) => saturation



BUT…. efficient trigger decisions require:

- long latencies (>> 4 μs)
- computational power
- data from many (all) sub-detectors (momentum, impact parameter .....)

⇒ Trigger in software

⇒ Use data from every bunch crossing

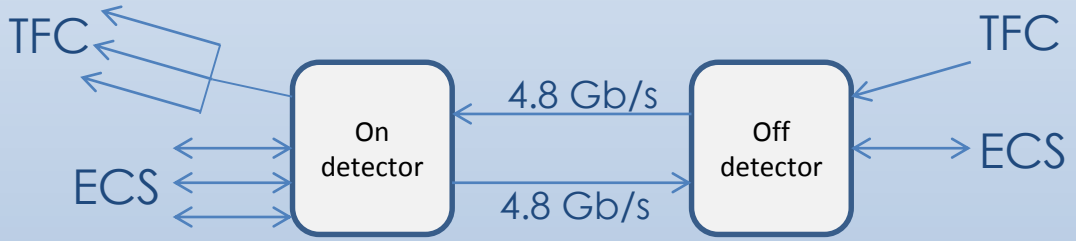
⇒ Upgrade electronics + DAQ **for LS2**

Architectural choices

Data compression on front-end to minimize links:
~ 15,000 links (4.8 Gbit/s)

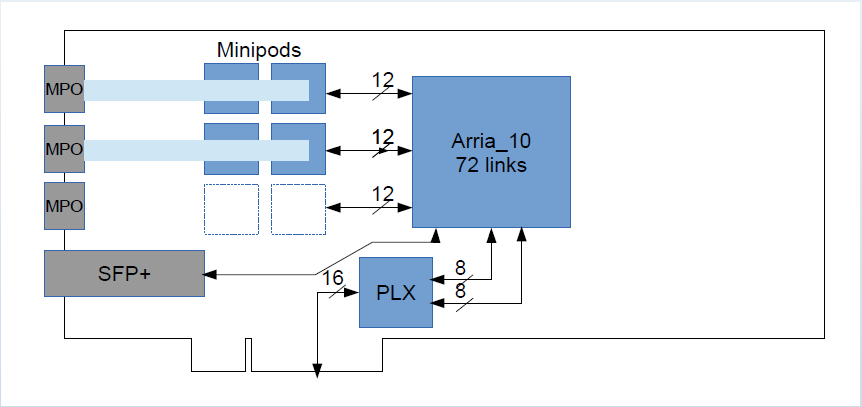
Flexibility:
4 of 6 sub-detectors will use FPGAs in front-ends

Combine slow & fast controls (ECS & TFC) in duplex links



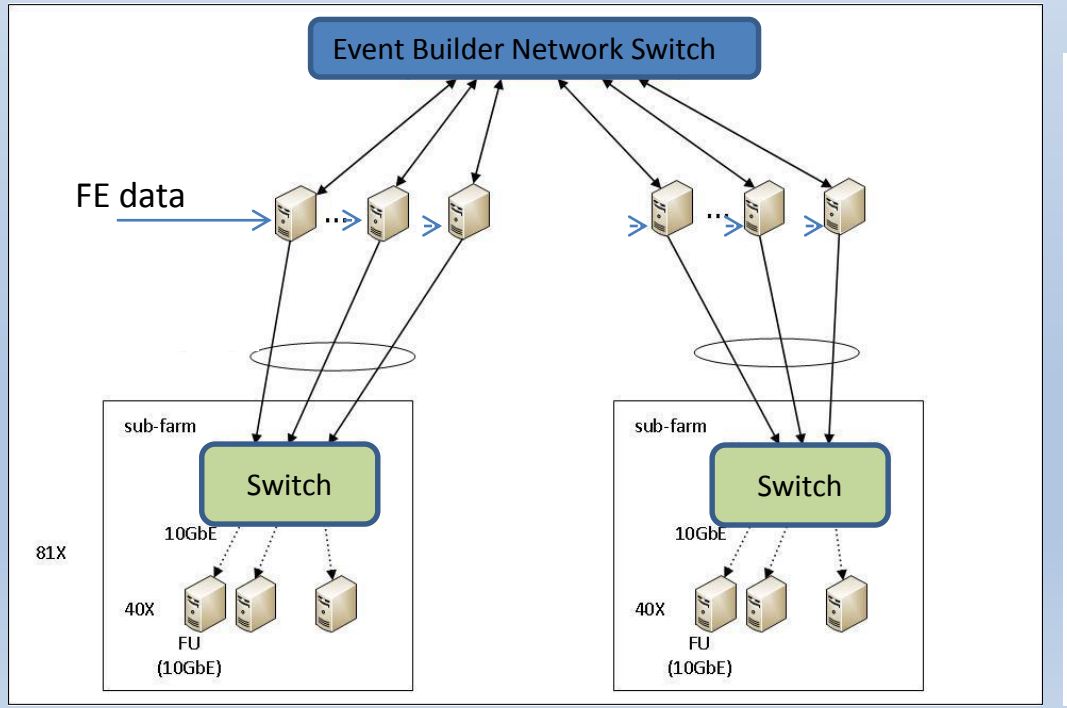
Simplex data links

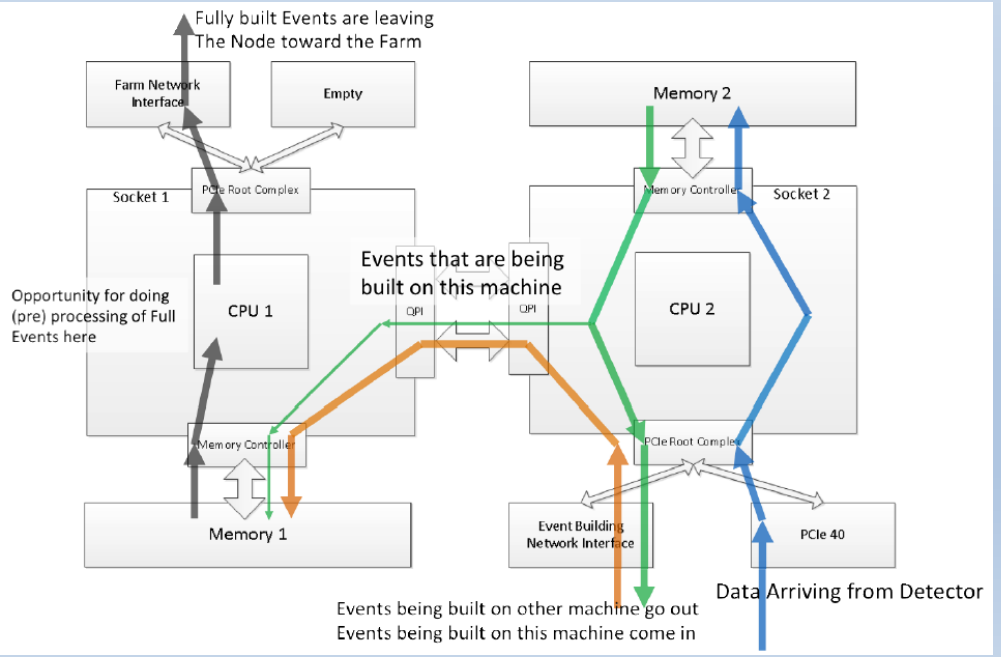
Backend is PCIe form factor in event-building farm



Use PC memory & processors for event building

Choose network interface at last moment (cheapest)





All data in a box