GigaRadMOST
Total Ionizing Dose Effects on 28 nm Bulk CMOS Technology

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Outline

- Introduction
- Measurement campaign
- TID effects on 28 nm bulk MOSFETs
- Characterization of TID effects on analog performance
- Modeling of TID-induced drain leakage current
- Comparison between TSMC 28 nm and 65 nm bulk CMOS technologies
- Conclusion
GigaRadMOST project

- Considering the potential use of **TSMC 28 nm bulk CMOS technology** in the forthcoming HL-LHC, our project aims at
  - characterizing the effects of TID up to 1 Grad on TSMC 28 nm bulk MOSFETs via DC and noise measurements
  - modeling the effects of TID on all aspects of the MOSFET operation including static and noise characteristics
  - implementing the built models into the BSIM6 compact model for radiation-tolerant circuit design

- In collaboration with the ScalTech28 project and the PH-ESE group at CERN, the following has been done
  - structure design with two tape-outs
  - measurement plan
  - non-irradiation and irradiation measurements at room temperature
  - two accepted journal papers, three presented conference papers, one accepted conference paper, and one submitted conference paper
TSMC 28 nm bulk CMOS technology

- This technology comes with different flavors
  - HPM (High-Performance Mobile Computation) → $V_{DD} = 0.9$ V
  - HPL (High-Performance Low-leakage) → $V_{DD} = 1$ V
  - HPC (High-Performance Mobile Compact) → $V_{DD} = 0.9$ V
  - ULP (Ultra-Low Power) → $V_{DD} = 0.7$ V

- The EuroPractice program covers only HPL and HPC
  - HPC also for mini@sic program (2 mm$^2$ area minimum, cost ~ 20 k€, twice per year)
  - NEW Micro-block program (1 mm$^2$ area, cost ~ 10 k€, twice per year)
  - HPL only available with general runs (6 mm$^2$ area minimum, cost ~ 50 k€, nearly every month)

- Our work focuses on a wide range of MOSFETs with standard VT in the HPL flavor
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Device Geometries

- Run 1 in June 2015
- Run 2 in December 2016

Note that we will be only discussing about those four corner MOSFETs.
Test structures

- nMOS with protection diodes at gate

- pMOS with protection diodes at gate

Note that due to the ESD protection at gate, it is not easy to get \( I_G \) for each transistor.
Measurement setup and protocol

- Measurement setup in CERN’s PH-ESE group
  - X-ray tube using a Tungsten target (peak 10 keV)
  - Dose rate is ~9 Mrad/h

- Measurement protocol
  - Bias during irradiation: \(|V_{GB}| = |V_{DS}| = 1.1\ V

<table>
<thead>
<tr>
<th>Pre-Irra. steps of TID</th>
<th>Post-irra. annealing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Room temp.</td>
<td>High temp. (100ºC)</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>...</td>
<td>1 Grad</td>
</tr>
</tbody>
</table>

- Measurement list
  - N1: \(I_D\) vs \(V_G\) @ \(V_S = V_{SUB} = 0\), \(V_{DD} = 1.1\ V\): \(V_D = 0, 0.01, 0.05, 0.1, 0.3, 0.5, 0.7, 0.9, 1, 1\) V, \(V_G = -0.2\)~\(1.1\) V (Step: 0.025 V)
  - N2: \(I_D\) vs \(V_D\) @ \(V_{SUB} = V_S = 0\), \(V_{DD} = 1.1\ V\): \(V_G = 0, 0.3, 0.5, 0.7, 0.9, 1.1\) V, \(V_D = 0\)~\(1.1\) V (Step: 0.025 V)
  - P1: \(I_D\) vs \(V_G\) @ \(V_{SUB} = V_{DD} = 1.1\ V\): \(V_D = 1, 0.8, 0.6, 0.4, 0.2, 0\) V, \(V_G = 0, 1.3\)~\(0\) V (Step: 0.025 V)
  - P2: \(I_D\) vs \(V_D\) @ \(V_{SUB} = V_S = V_{DD} = 1.1\ V\): \(V_G = 0, 0.8, 0.6, 0.4, 0.2, 0\) V, \(V_D = 1.1\)~\(0\) V (Step: 0.025 V)
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Top view and cross sections along W and L

(a) 
Source (S) — Gate (G) — Drain (D)
STI
L
G
GOX
STI
Sub.

(b) 
G
GOX
S
Sub.
D
LDD

(c) 
G
GOX
STI
Sub.

+: $Q_{ot}$ (positive for n&pMOS)
$x$: $Q_{it}$ (negative for nMOS, positive for pMOS)
$|I_{DS}|$-$|V_{GB}|$ of four corner MOSFETs in saturation ($|V_{DS}| = 1.1 \text{ V}$)

$W/L_{n} = 2.75 \mu m/1 \mu m$
$V_{DB} = 1.1 \text{ V}$, $V_{SB} = 0$

$W/L_{n} = 3 \mu m/30nm$
$V_{DB} = 1.1 \text{ V}$, $V_{SB} = 0$

$W/L_{n} = 100nm/1 \mu m$
$V_{DB} = 1.1 \text{ V}$, $V_{SB} = 0$

$W/L_{n} = 100nm/30nm$
$V_{DB} = 1.1 \text{ V}$, $V_{SB} = 0$

\(|I_{DS}| - |V_{GB} - V_{T0}|\) of four corner MOSFETs in saturation (\(|V_{DS}| = 1.1\, \text{V}\))

\(W/(L_n) = 2.75 \mu\text{m}/1\mu\text{m}\)
\(V_{DB} = 1.1\, \text{V}, V_{SB} = 0\)

\(W/(L_n) = 3 \mu\text{m}/30\text{nm}\)
\(V_{DB} = 1.1\, \text{V}, V_{SB} = 0\)

\(W/(L_n) = 100\text{nm}/1\mu\text{m}\)
\(V_{DB} = 1.1\, \text{V}, V_{SB} = 0\)

\(W/(L_n) = 100\text{nm}/30\text{nm}\)
\(V_{DB} = 1.1\, \text{V}, V_{BS} = 0\)

TID effects on 28 nm bulk MOSFETs

Post-irradiation annealing effects on $|I_{DS}| - |V_{GB}|$ of four corner MOSFETs in saturation ($|V_{DS}| = 1.1 \, V$)

Note that the partly recovered device performance is due to the high-temp. annealing of the oxide-trapped charge in STI.
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Introduction to the simplified EKV model

- The inversion coefficient $IC$ or the normalized drain current:

$$\frac{I_D\big|_{\text{total}}}{I_{\text{spec}}} = \frac{I_D\big|_{\text{saturation}}}{I_{\text{spec}}} + \frac{I_{\text{leak}}}{I_{\text{spec}}} = IC + \frac{I_{\text{leak}}}{I_{\text{spec}}} = \frac{4\left(q_s^2 + q_s\right)}{2 + \lambda_c + \sqrt{4\left(1 + \lambda_c\right) + \lambda_c^2 \left(1 + 2q_s^2\right)^2}} + \frac{I_{\text{leak}}}{I_{\text{spec}}}$$

- The specific current $I_{\text{spec}}$ is defined as

$$I_{\text{spec}} = I_{\text{spec}^\square} \cdot \frac{W}{L} \quad \text{with} \quad I_{\text{spec}^\square} = 2n \cdot \mu_0 \cdot C_{\text{ox}} \cdot U_T^2 \quad \text{and} \quad U_T = \frac{kT}{q}$$

- $\lambda_c$ is the velocity saturation (VS) parameter: $\lambda_c = \frac{L_{\text{sat}}}{L}$

- $q_s$ is the normalized inversion charge at source:

$$v_p - v_s = \ln\left(q_s\right) + 2q_s \quad \text{with} \quad v_p = \frac{V_P}{U_T} = \frac{V_G - V_{T0}}{nU_T} \quad v_s = \frac{V_S}{U_T} \quad U_T = \frac{kT}{q}$$

- Only requires five parameters: $n, I_{\text{spec}^\square}, L_{\text{sat}}, V_{T0}, I_{\text{leak}}$. 
Large-signal transfer characteristics validation in saturation ($|V_{DS}| = 1.1\, \text{V}$)

Filled markers – prior to irra.
Empty markers – 1 Grad

Wide nMOS at $V_D=1.1\, \text{V}$, $V_B=V_S=0$

Wide pMOS at $V_D=0$, $V_B=V_S=1.1\, \text{V}$

Wide nMOS at $V_D=1.1\, \text{V}$, $V_B=V_S=0$

Wide pMOS at $V_D=0$, $V_B=V_S=1.1\, \text{V}$

Narrow nMOS at $V_D=1.1\, \text{V}$, $V_B=V_S=0$

Narrow pMOS at $V_D=0$, $V_B=V_S=1.1\, \text{V}$

TID effects on relevant parameters

- **TID effects on analog performance**

- **Equation:**
  \[ SS_{theo.} = (\ln 10) n \cdot U_T \]

- **Graphs:**
  - Ion leakage current vs. Total Ionizing Dose
  - Transconductance vs. Total Ionizing Dose
  - Subthreshold swing vs. Total Ionizing Dose
  - Gate oxide integrity vs. Total Ionizing Dose

- **References:**
TID-independent $G_m \cdot n \cdot U_T/I_D$
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TID-induced drain leakage current in nMOSFETs

- The drain leakage current significantly increases

\[
I_{\text{Dleak}} = I_{\text{Dleak.main}} + 2I_{\text{Dleak.par}}
\]

Modeling the drain leakage current of nMOSFETs

- The drain leakage current is modelled by

\[ I_{D\text{leak}} = I_{D\text{leak0}} \cdot \left[ 1 + \left( \frac{TID}{TID_{\text{crit}}} \right)^k \right] \]

- The parasitic leakage current is modelled by

\[ I_{D\text{leak,par}} = \frac{I_{D\text{leak0}}}{2} \cdot \left( \frac{TID}{TID_{\text{crit}}} \right)^k \]

### TABLE I

<table>
<thead>
<tr>
<th>(W_n/L_n)</th>
<th>(I_{D\text{leak0}}) (A)</th>
<th>(k)</th>
<th>(TID_{crit}) (Mrad)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3 μm/1 μm</td>
<td>(1.3 \times 10^{-10})</td>
<td>0.8</td>
<td>59</td>
</tr>
<tr>
<td>100 nm/1 μm</td>
<td>(8.5 \times 10^{-12})</td>
<td>0.8</td>
<td>1.8</td>
</tr>
<tr>
<td>3 μm/30 nm</td>
<td>(2.2 \times 10^{-10})</td>
<td>1.4</td>
<td>7.4</td>
</tr>
<tr>
<td>100 nm/30 nm</td>
<td>(1.9 \times 10^{-12})</td>
<td>1.4</td>
<td>1.2</td>
</tr>
</tbody>
</table>
Modeling the parasitic parallel n-FETs

- The drain leakage current is independent of gate voltage at a relatively high TID.
- This enables to model the parasitic parallel n-FET as a gate-less charge-controlled device: $Q_{oxeq} = -Q_{si}$.

$$Q_{oxeq}^2 = \Gamma_{bc}^2 \cdot U_T \cdot \left[ \frac{2 \Phi_F}{U_T} + \ln \frac{I_{Dleak0}}{I_{speeq}} + k \cdot \ln \frac{TID}{TID_{crit}} \right]$$

\[ (6.93 \times 10^{12})^2 \]
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Comparison between TSMC 28 nm and 65 nm bulk CMOS technologies

- 1μm/60nm from TSMC 28 nm bulk CMOS
- 1μm/60nm from TSMC 65 nm bulk CMOS

<table>
<thead>
<tr>
<th>1μm/60nm</th>
<th>$V_{DS}=V_{DD}$</th>
<th>$V_T$ Var.</th>
<th>SubS Var.</th>
<th>$I_{off}$ ($V_{GB}=0$)</th>
<th>$I_{on}$ Var. ($V_{GB}=V_{DD}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>28nm</td>
<td>1.1 V</td>
<td>-13%</td>
<td>15%</td>
<td>537x</td>
<td>+15%</td>
</tr>
<tr>
<td>65nm(ref)</td>
<td>1.2 V</td>
<td>+39%</td>
<td>47%</td>
<td>10x</td>
<td>-55%</td>
</tr>
</tbody>
</table>

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Conclusion

- TSMC 28 nm bulk MOSFETs are rather radiation tolerant, except the significant increase in $I_{\text{Dleak}}$ of nMOSFETs.
- A few hours of high-temp. annealing annihilates or neutralizes $Q_{\text{ot}}$ in the thick STI oxides that reduces $I_{\text{Dleak}}$ and recovers $I_{\text{on}}$.
- TSMC 28 nm bulk CMOS process seems to be more radiation-tolerant than TSMC 65 nm.
- The normalized $G_m/I_D$ is TID-independent that makes this EKV-based model as a favorable design methodology.
- The parasitic leakage current is modelled well with a semi-empirical physical model and the parasitic n-FET is modeled as a gate-less charged-based device.
Acknowledgement

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Publications

- **Journal papers**

- **Conference papers**