Plans for the evaluation of the TID tolerance in 65nm and below

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65nm

The provider of Foundry Services has been selected, and infrastructure has been developed to enable ASIC design (PDK, NDAs, frame contracts, IP blocks, support service, etc.)

Leakage current does not appear in 65nm NMOS transistors consistently in all samples measured so far!

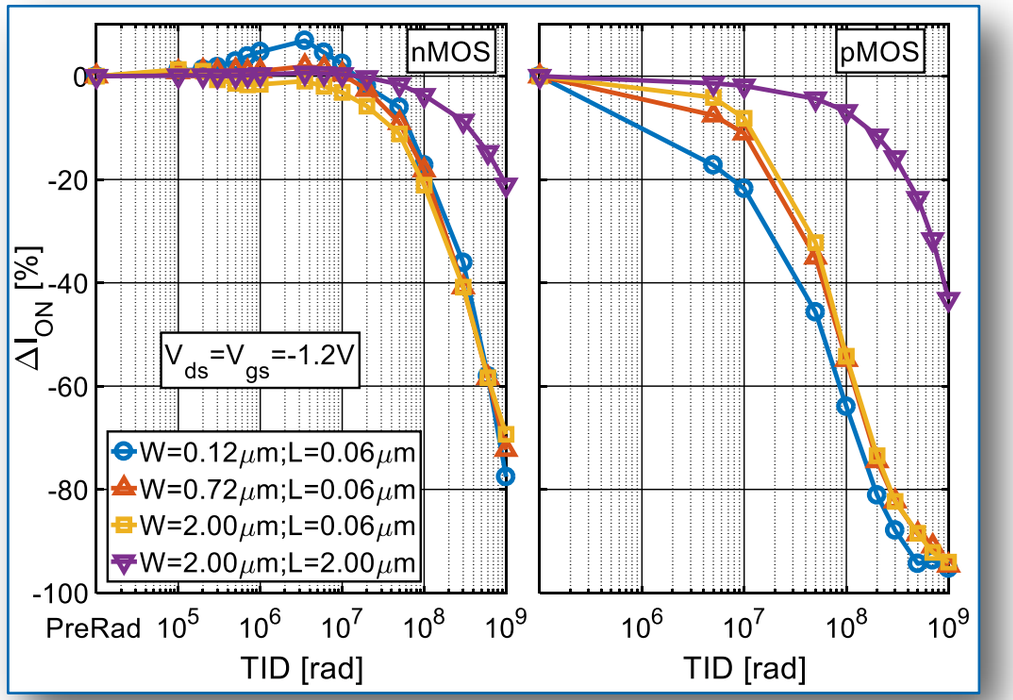
We will monitor this parameter in specific test structures added to all runs, as already in place for 130nm

Radiation damage is severe in short (RISCE) and narrow (RINCE) channel transistors, where it depends on the bias and temperature applied both during and after irradiation

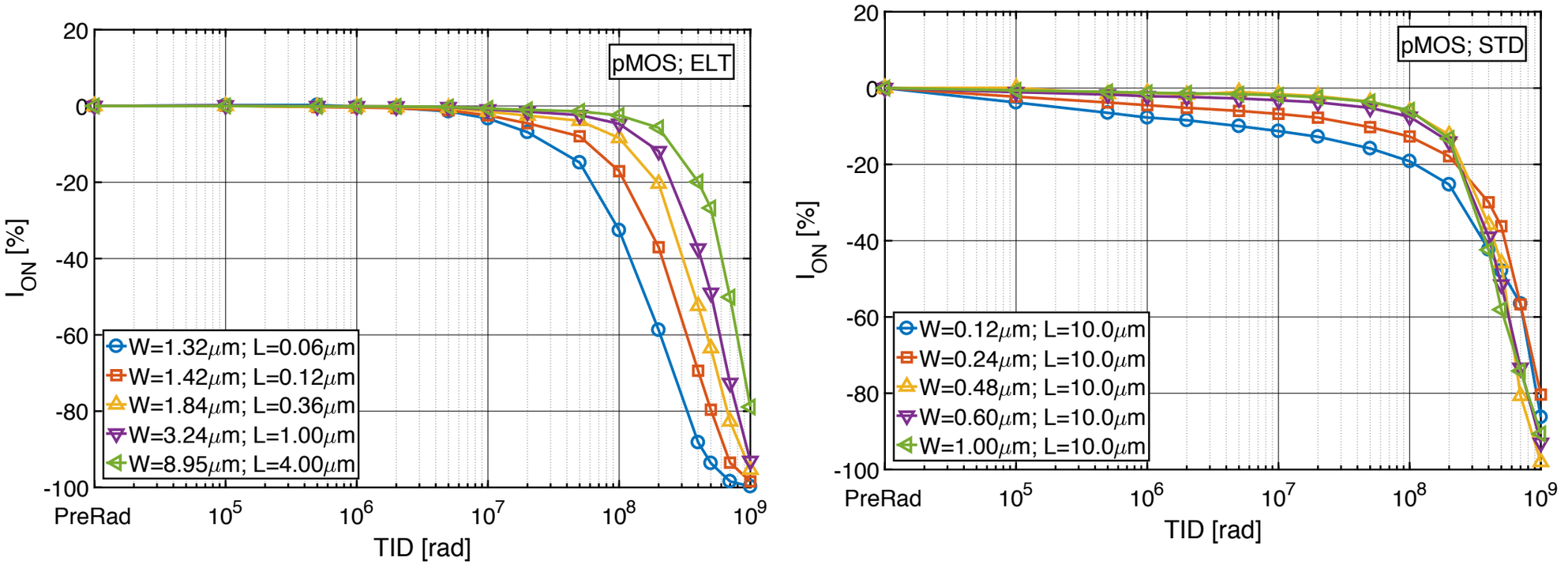
We will also monitor the I_{on} degradation in the same test structures

Measurements on samples from other two 65nm manufacturers showed comparable or even worse damage. There is no reason to reconsider the supplier of this technology.

Supplier X (samples courtesy of MOSIS)



Supplier Y (work in collaboration with the University of Sevilla)



Future work in 65nm

Develop a model to enable the SPICE simulation of irradiated circuits

Study the apparent dose-rate dependence of the radiation damage

Confirm the physical model of the damage in short-channel MOSFETs

The development of a SPICE model (BSIM4) for the simulation of irradiated transistors in 65nm has been outsourced to the Technical University of Crete (TUC)

The initial target is to provide models for the following transistors/conditions:

- Core standard-Vt NMOS and PMOS, linear and ELT layout
- TID levels: 100, 200 and 500 Mrad
- Irradiation temperature: -30, 0 and 25 ^{o}C

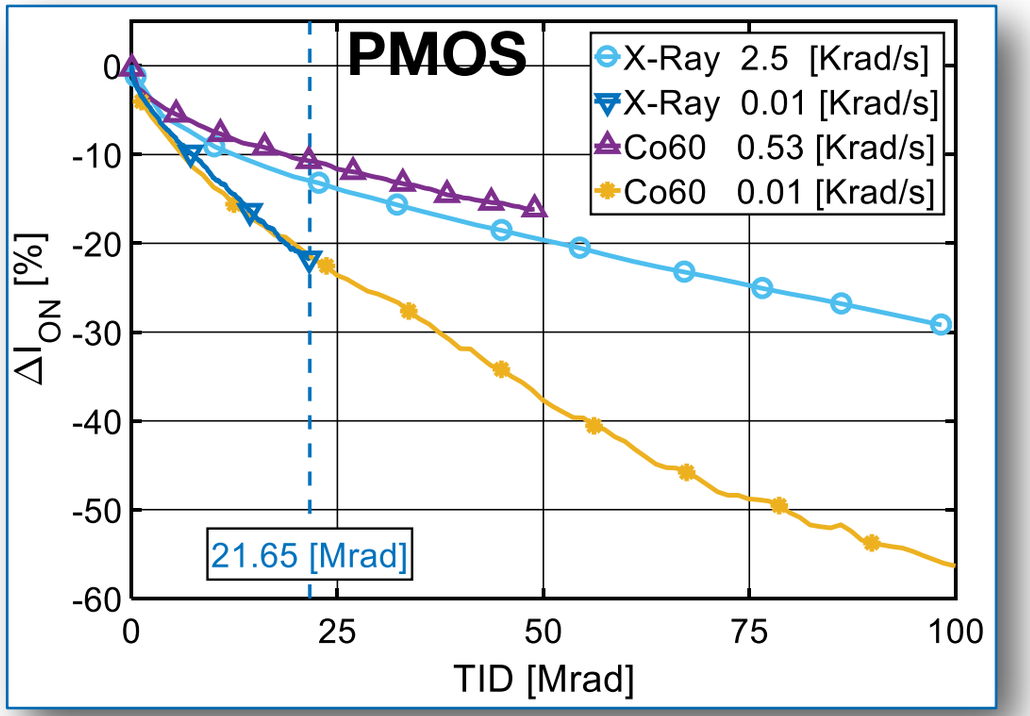
There is the option of repeating the operation, in a somewhat simplified form, for high- and low-Vt devices

The model is only as good as the data used to build it. A very large testing effort was carried on!

(The irradiation time required to provide data at the 3 temperatures is above 60 days)

First set of models is available for a full evaluation, and the complete set should be ready in the next 6 weeks.

Measurements on identical samples in the 65nm technology at different facilities (X-rays and ^{60}Co) show a consistent trend to larger damage at lower dose rate



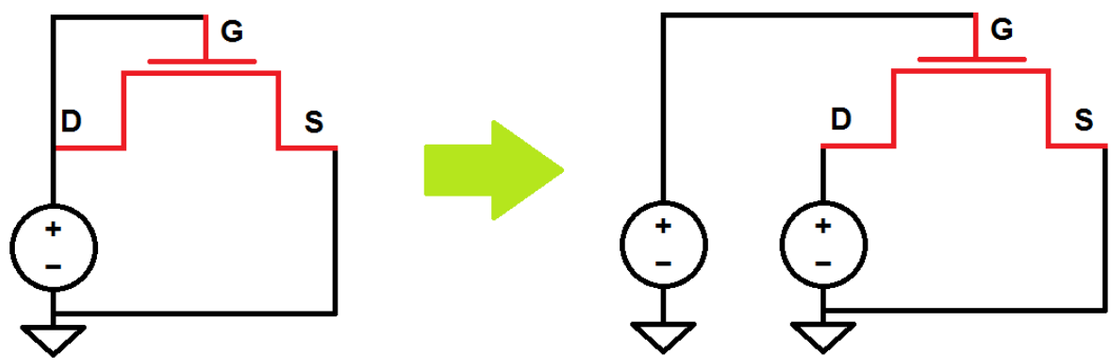
Qualitatively similar results are observed in samples from the 130nm technology

This dose rate dependency of the damage has to be studied:

- bias and temperature dependence
- physical origin (STI? Spacers?)
- influence of the transistor's size

The effect should then be included in our qualification procedure!

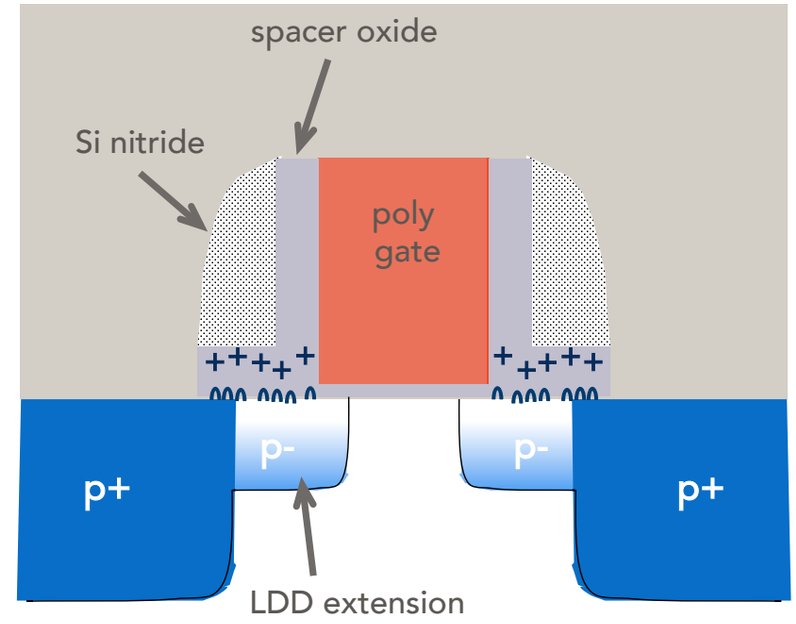
A dedicated test structure has been designed, and the measurement setup modified to allow for the full measurement of the transfer and output characteristics.
Our new X-ray irradiation facility, presently being commissioned, will be used for long-term irradiation runs at different temperatures.

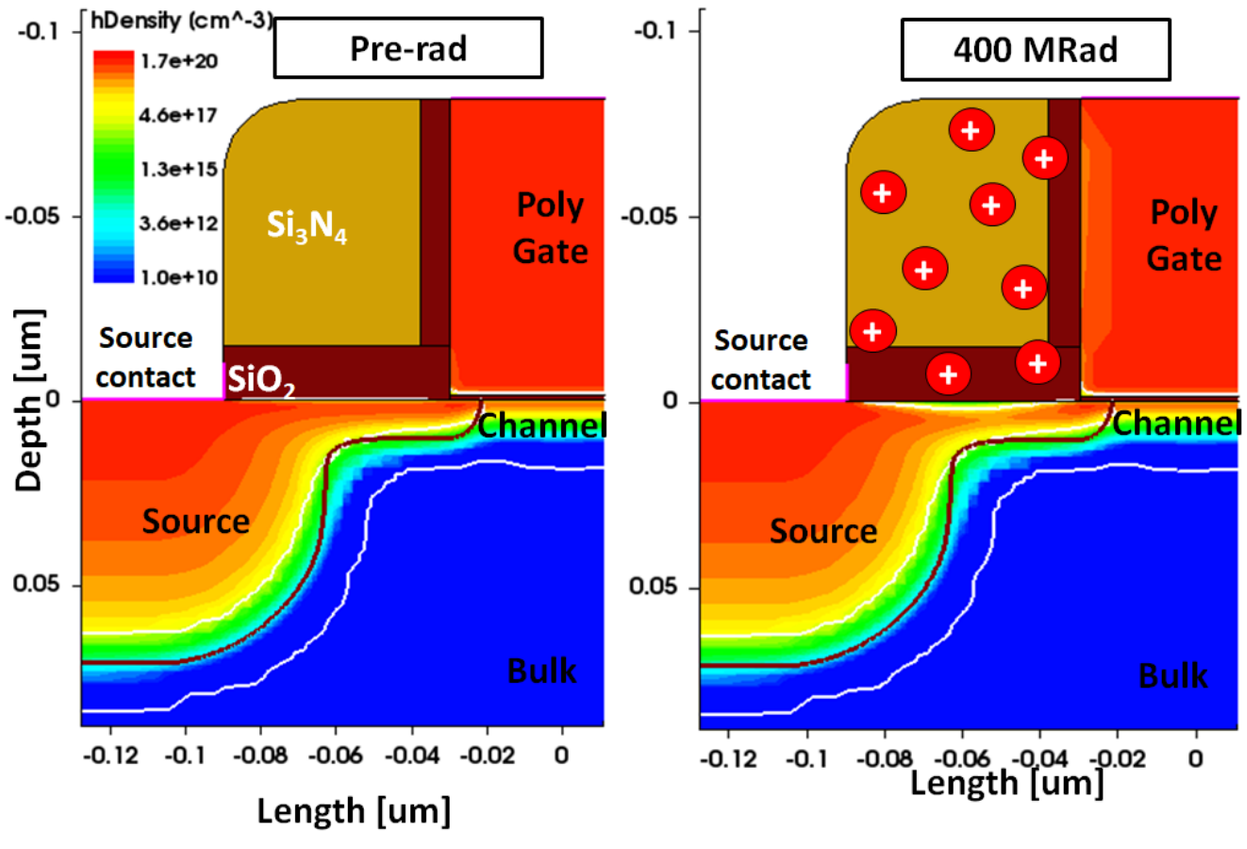


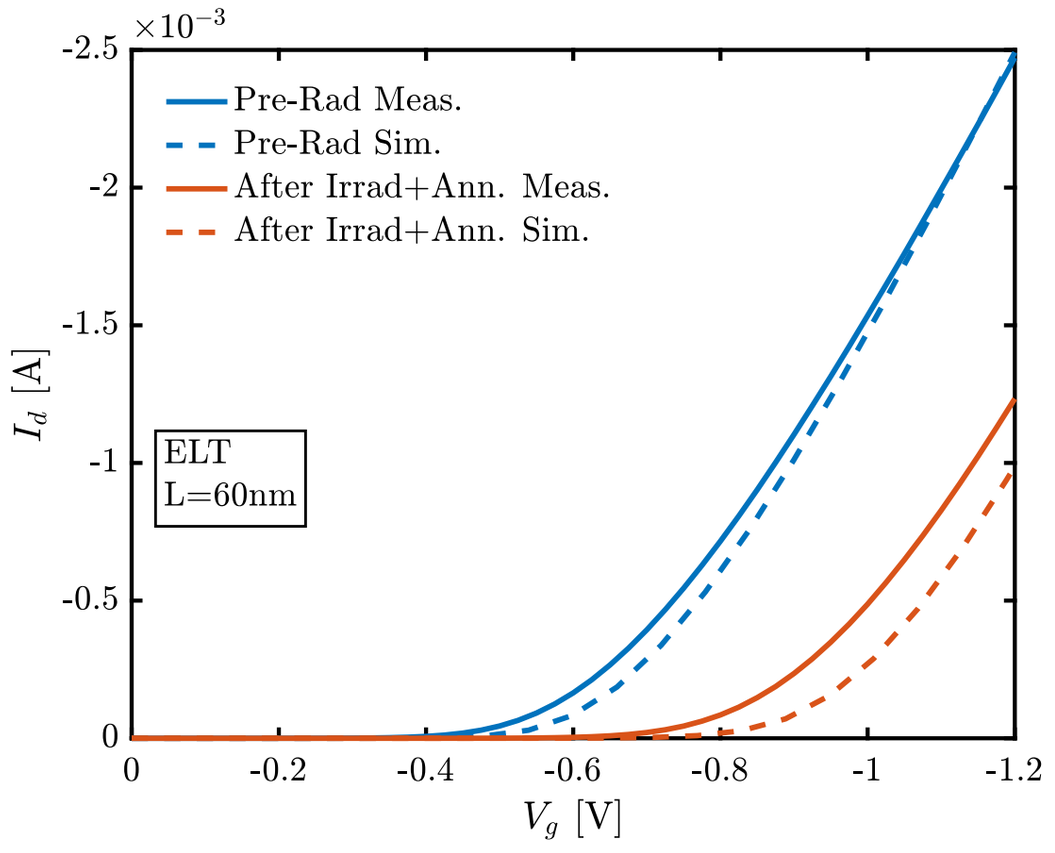
ELT transistors with short channel (L = 60 nm)
⇒ spacers-related effects

Narrow transistors (W=120 nm; L= 10 µm)
⇒ STI-related effects

Charge pumping measurements and 2-D simulations confirm the charge buildup model leading to the performance degradation in short-channel PMOS transistors







Simulation study carried on at DEI, Padova University

… and below 65nm

We are starting the study of the TID tolerance of 40 and 28nm CMOS processes, a work that is financed within the FCC preparatory studies.

Although we are mainly interested in 28nm - this appears to be a good candidate for post-65nm in our applications - it is however very interesting to study also the 40nm node (that still uses conventional SiO_2 as gate insulator).

The study will be done using custom-developed test structure very similar to those conventionally used already in 130 and 65nm: arrays of transistors with a combination of W and L.

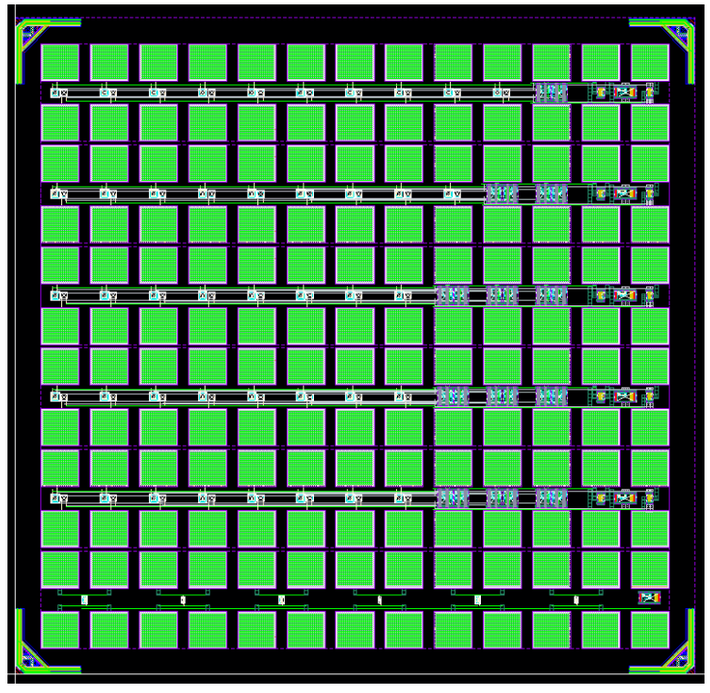
The definition of the test structures is done at CERN, while the design is done by IMEC (to avoid the need for NDAs and installation of Design Kits).

The size of the mini@sic bloc strongly depends on the technology.

The typical transistors included in the test structures are:

Core std Vt	Core LowVt	Core HighVt	I/O transistors
W array (long L)	Mini array of different W and L	Mini array of different W and L	Mini array of different W and L
L array (wide W)			
Blocs to study the effect of bias			
Blocs to study the variability in the response			

Example layout of the test chip (here TSMC 40nm)

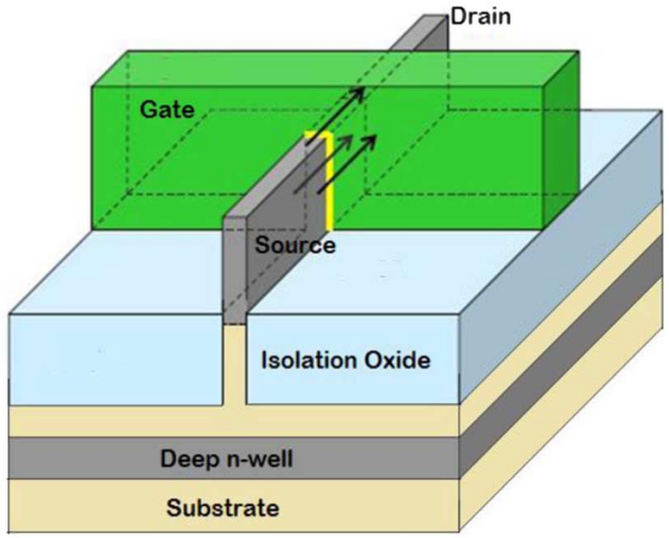


This is the most updated plan to procure the hardware for the study:

Foundry	Node	Target MPW mini@sic	TAT	Design status
GF	40nm	June 4	5 months	completed
	28nm	May 5		completed
TSMC	40nm	March 6	3.5 months	completed
	28nm (HPC)	April 25		completed

We expect to have results available in end 2018 - beginning 2019

Studies of the TID tolerance of FinFETs within the radiation effects community do not show promising results



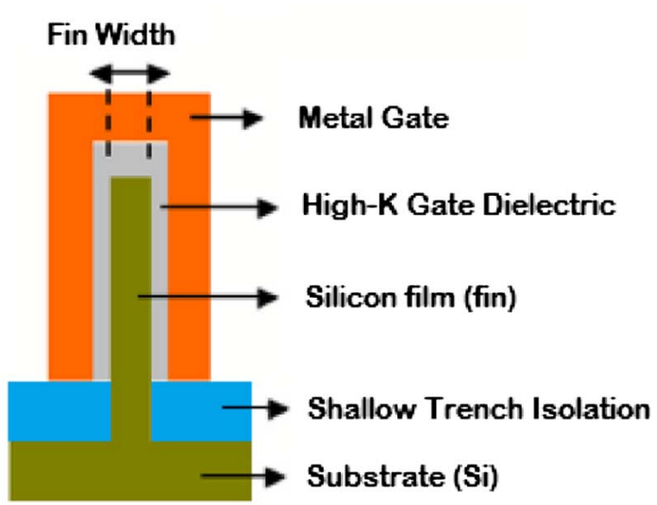
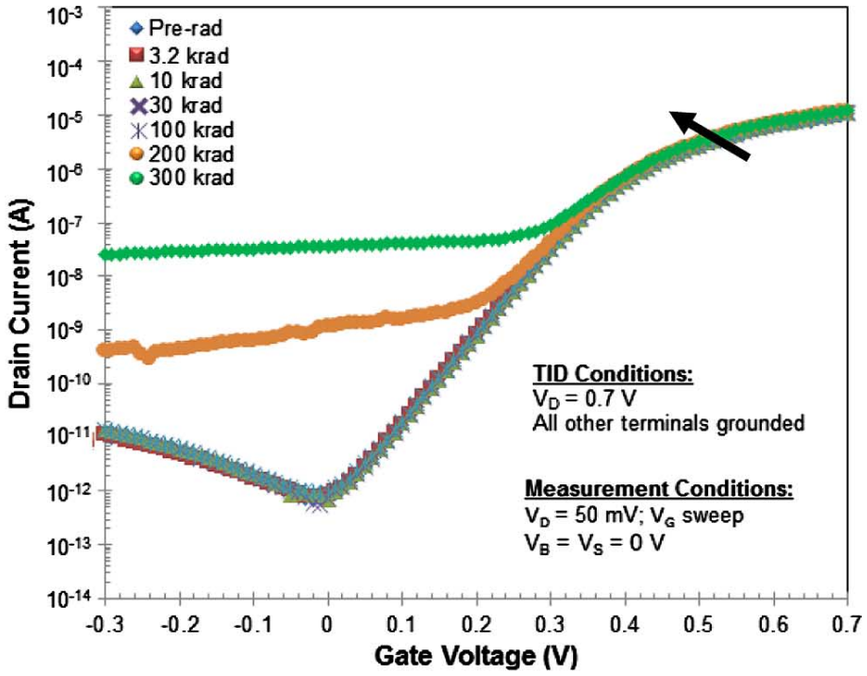
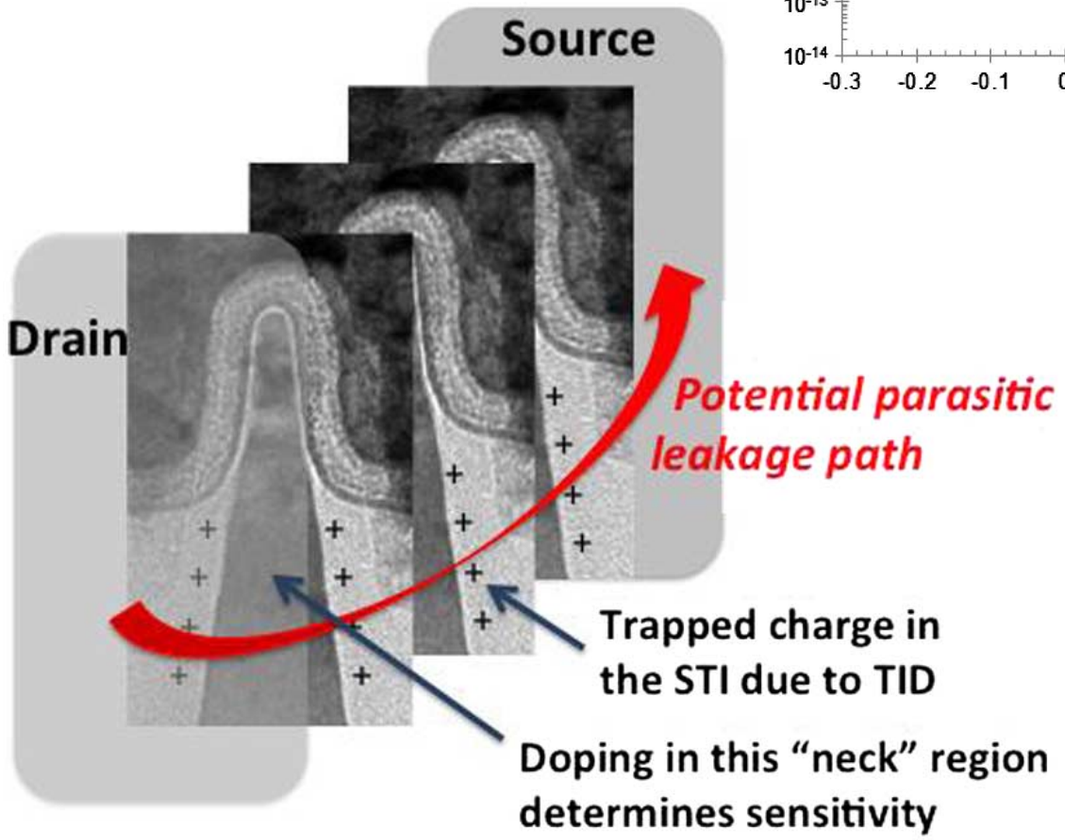


Fig. 1. 3D schematic illustration of a triple-well bulk FinFET.

after I.Chatterjee et al., "Bias Dependence of Total-Dose Effects in Bulk FinFETs", IEEE TNS 60, n.6, 2013





Conclusion

The main focus of the TID study is still in our baseline 65nm technology

- **there is no reason to switch to another supplier**
- **the stability of the radiation response has to be monitored regularly**
- **the dose rate effect has to be studied and accounted for in our qualification procedure**

Our community has to look beyond 65nm in preparation for upgrades/new experiments.