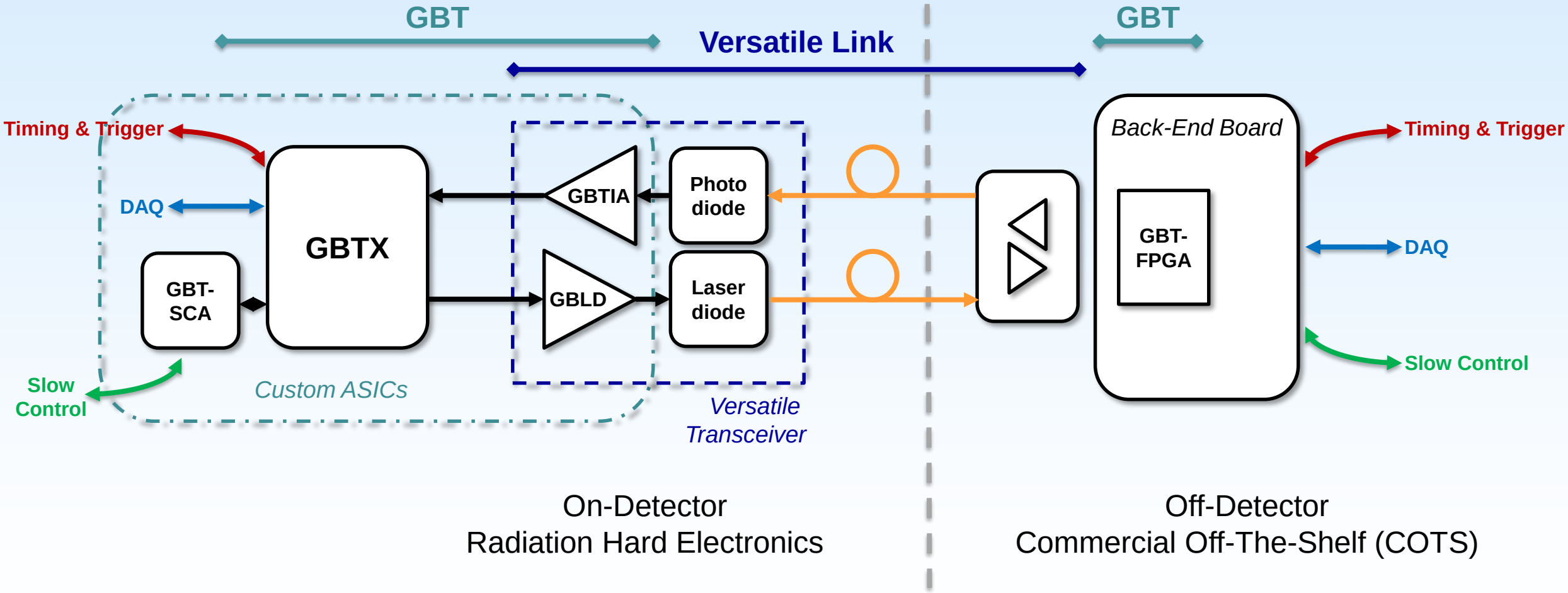
Versatile Link and GBT Chipset Production

Status, Issues Encountered, and Lessons Learned

Lauri Olanterä
on behalf of the Versatile Link and GBT projects

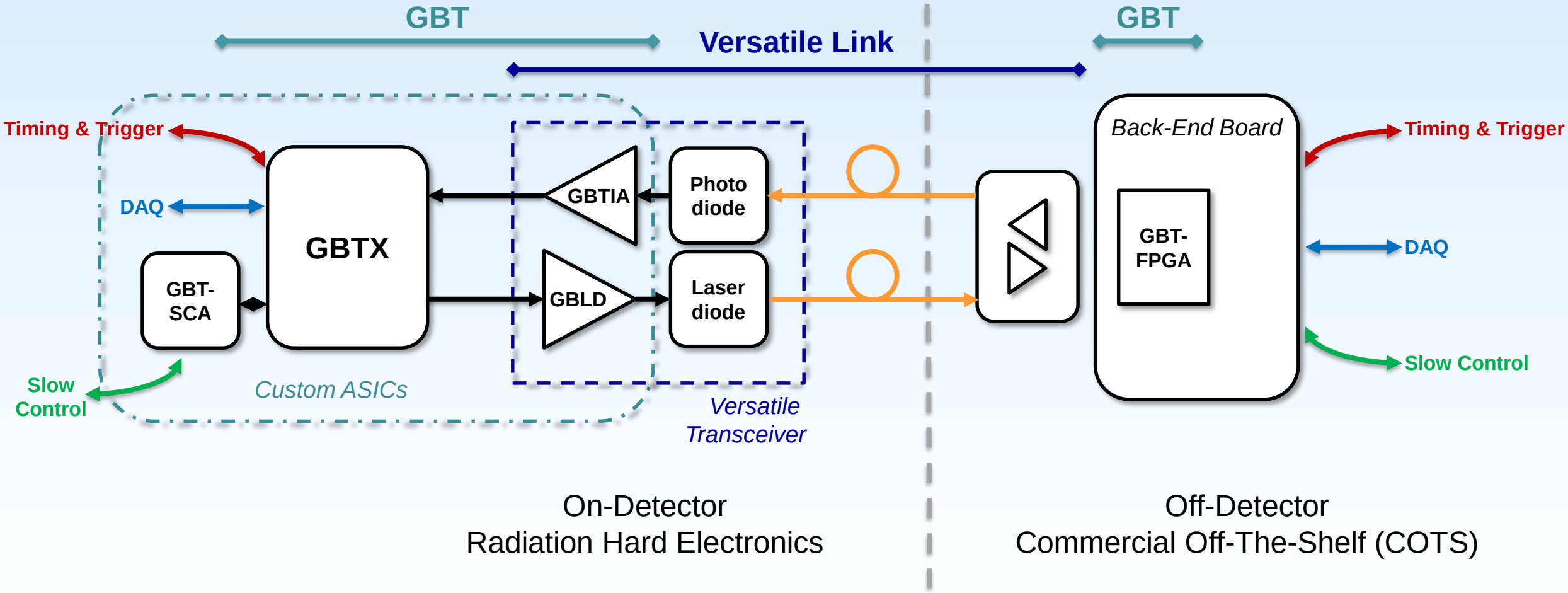
Radiation Hard Optical Link Architecture: VL and GBT



GBT and VL users

	User	GBTX	GBT-SCA	VTTx	VTRx MM	VTRx SM
Four big CERN experiments	LHCb	14442	6357	7098	2076	
	CMS HCAL			2547	370	100
	CMS GEM	510	170	340	510	
	CMS ECAL	230	45	120	55	
	CMS CSC	650		650	650	
	ATLAS NSW	4266	8160	1177	1665	
	ATLAS LArg	775	775			
	ATLAS Tiles	2550				
	ALICE	9755	5089	4267	5166	340
LHC	BE-BI-BL					500
	BE-BI-QP	500				500
External users	CBM@FAIR	6700	2500	2100	2500	
	PANDA1@FAIR	220			220	
	PANDA2@FAIR				500	
	Mu2e@Fermilab				500	
	Totals	**40598**	**23096**	**18299**	**14468**	**1340**

Radiation Hard Optical Link Architecture: VL and GBT



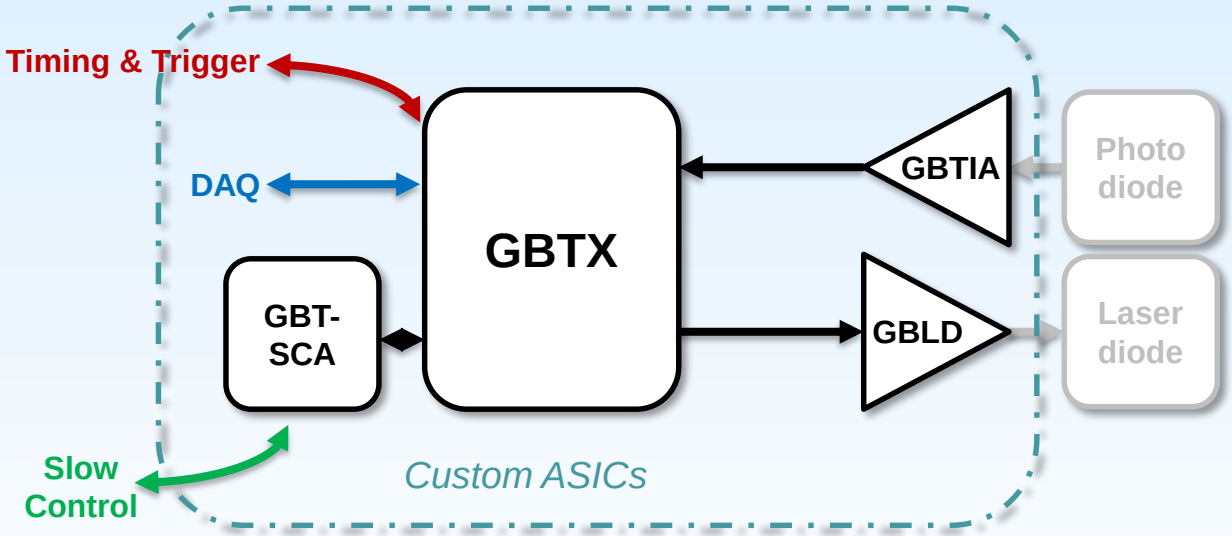
GBT Chipset Production

GBTX

- 4.8 Gb/s Transceiver
- Manages the communications between the counting room and the frontend modules

GBTIA

- 4.8 Gb/s Transimpedance Amplifier
- Amplifies the weak photocurrent generated by the PIN diode



- 168 GBTX wafers, ~**50,000** chips
- 76 GBLD wafers, ~**91,000** chips
- 28 GBTIA wafers, ~**27,000** chips
- GBT-SCA: 28 wafers shared with CBC3, ~**60,000** SCA chips

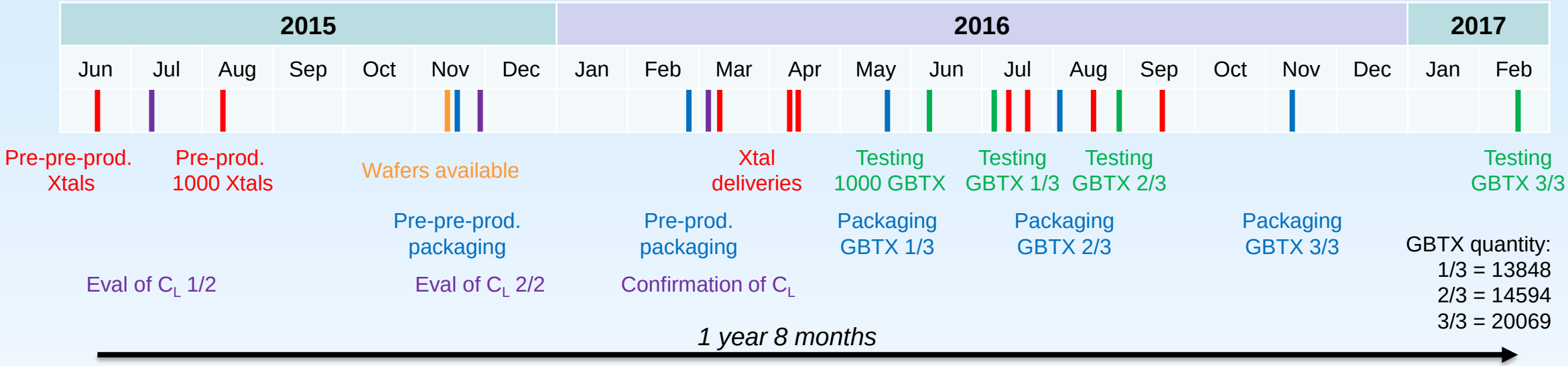
GBT-SCA

- Slow Control Adapter
- Experiment control and environment monitoring

GBLD

- 4.8 Gb/s Laser Driver
- Modulates laser current to achieve electro-optical conversion

GBTX Production and Testing



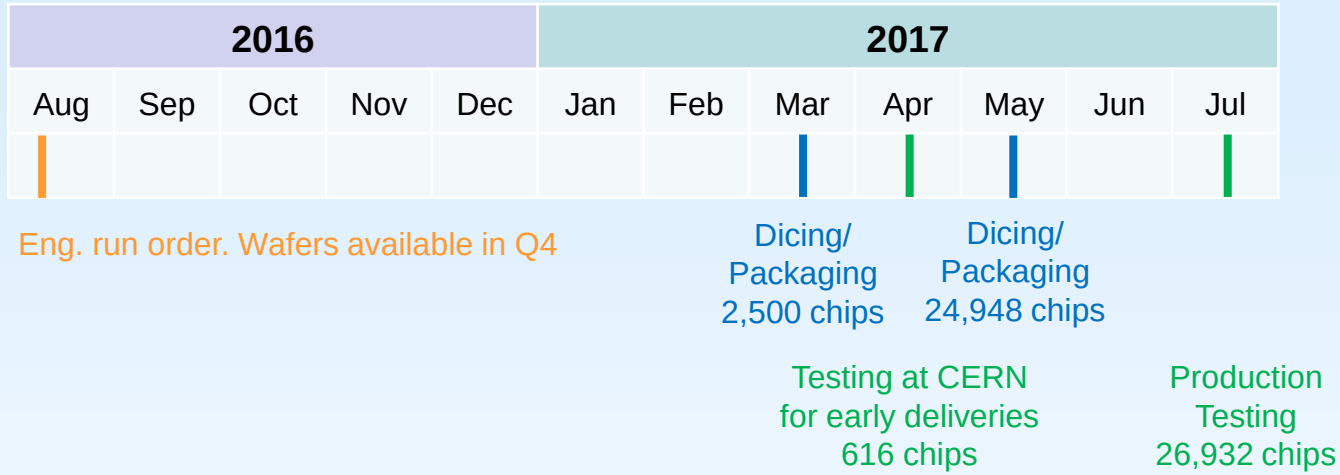
- 48,237 devices tested, 45073 good → **yield 93.4%**
- ~50% of ordered GBTXs delivered to users

Lessons learnt:

- Take purchasing procedures and other delays into account early in the process. This was a significant factor in case of the GBTX packaging. However, to properly plan and start packaging in time, some technical details (e.g. chip pin out) have to be defined early on.

- Crystals: expensive components which require a lot of evaluation and long production. Try to avoid.

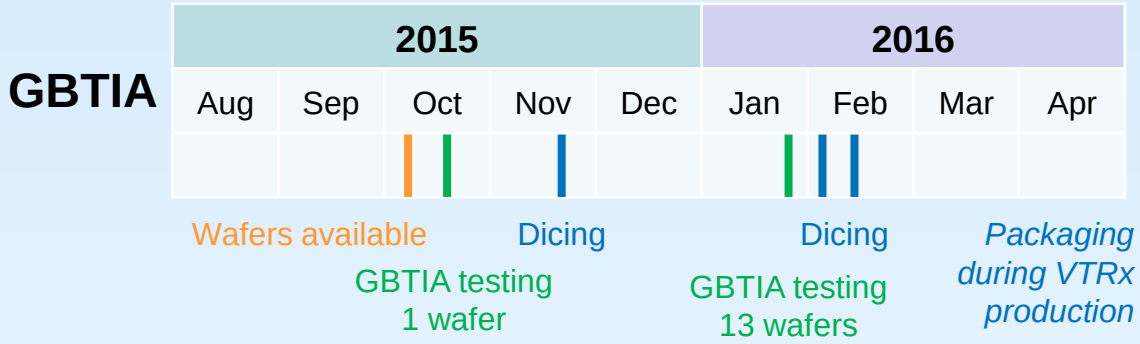
GBT-SCA Production and Testing



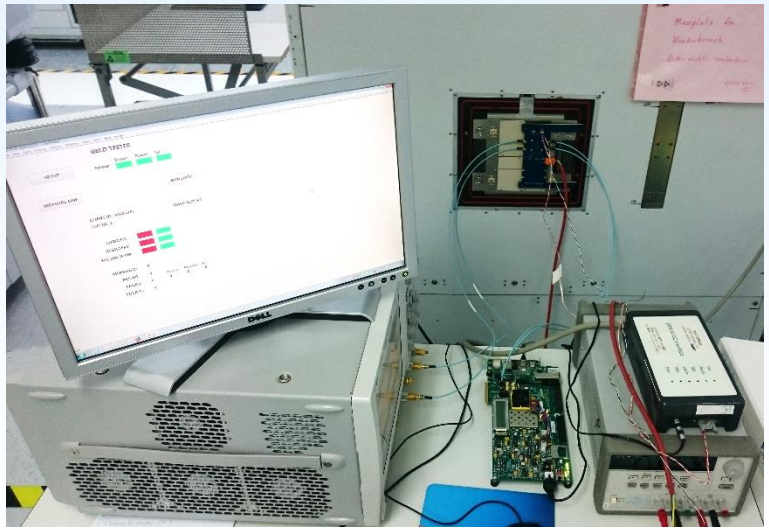
- Production testing yield: **94.4%**. Majority of failures due to
  - Null power consumption (2.9%)
  - E-port or internal control (1.21%)
  - Communication interfaces (0.96%)

- **~75%** of the ordered GBT-SCAs delivered to users

GBLD and GBTIA Production and Testing



- More than 90,000 GBLDs were tested focusing on the important *dynamic* performance
- Yield > 99%
  - More than enough good chips for VTRx production
- Biggest issues were contact problems
  - GBLD package (QFN24) and used test socket were very picky about the contact force
  - All failures were re-tested

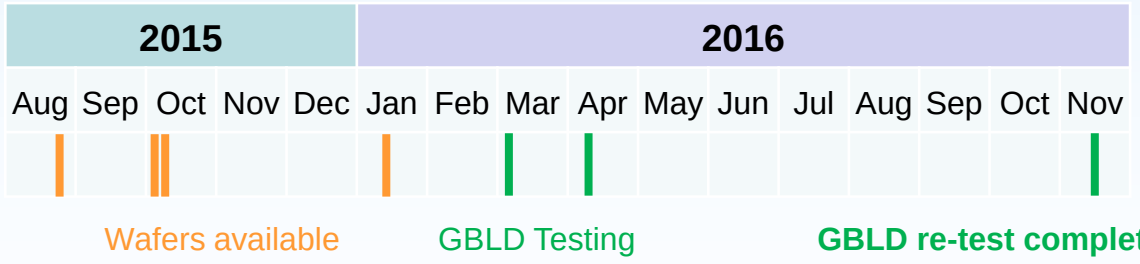


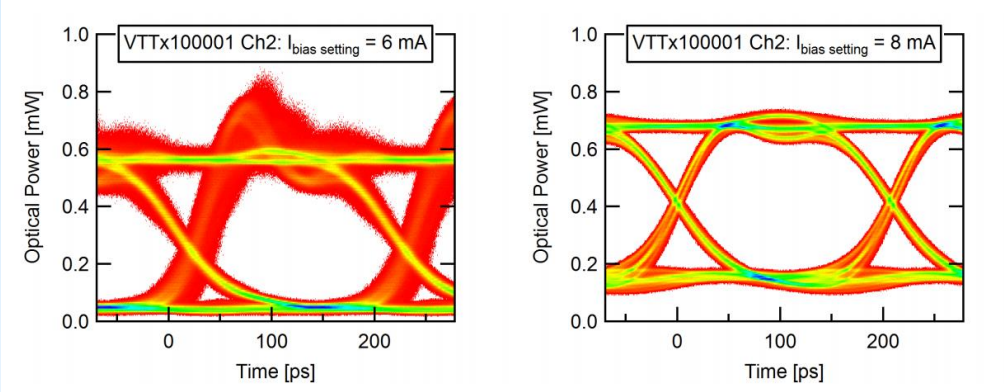
GBLD test setup

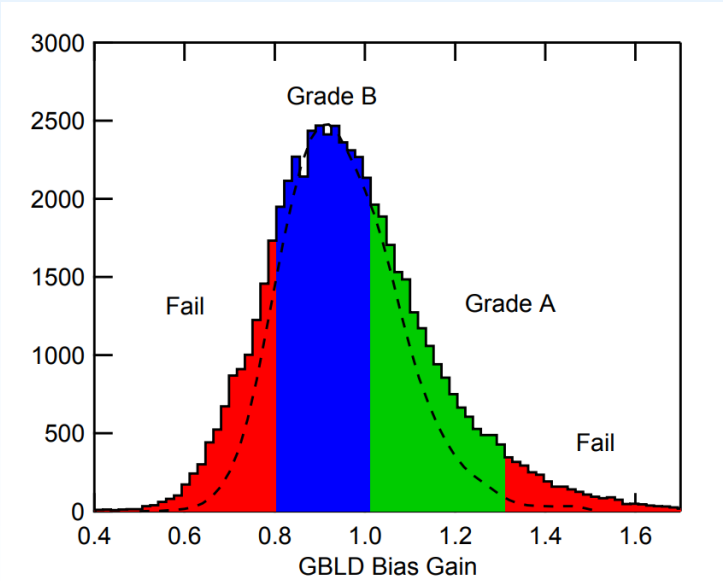
- The first 14 wafers were tested (wafer probed)
  - Already enough good die for VTRx production
- Remaining 14 wafers were tested and diced later in 2016
  - Not used in VTRx production

Encountered Issue: GBLD bias current

- Too many bad eye diagrams measured during VTTx pre-series QA (the first module pre-series)
- Lasers are driven below threshold current?
  - Bad lasers slipped through the QA? Assembly damage?
- None of the above: a large spread in bias currents generated by the GBLD laser drivers
  - Manual testing of ~1000 GBLDs to understand the distribution
  - Define grading system that guarantees correct operation: *Grade A* for VTRx, *Grade B* for VTTx
  - Re-testing all GBLD drivers





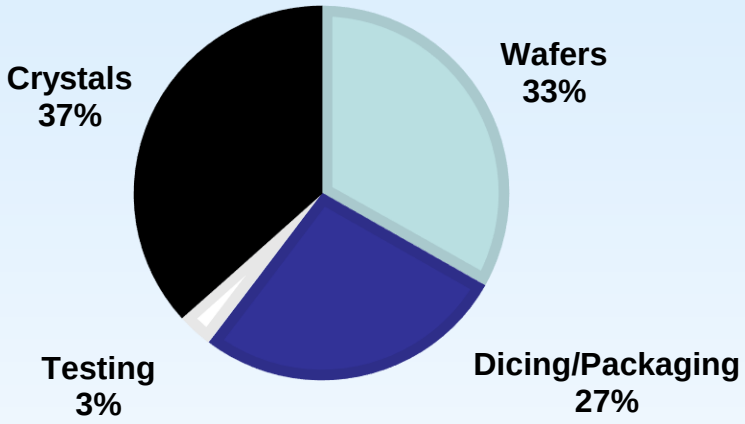


Bias Gain = real bias current / bias current setting
→ ideally always 1

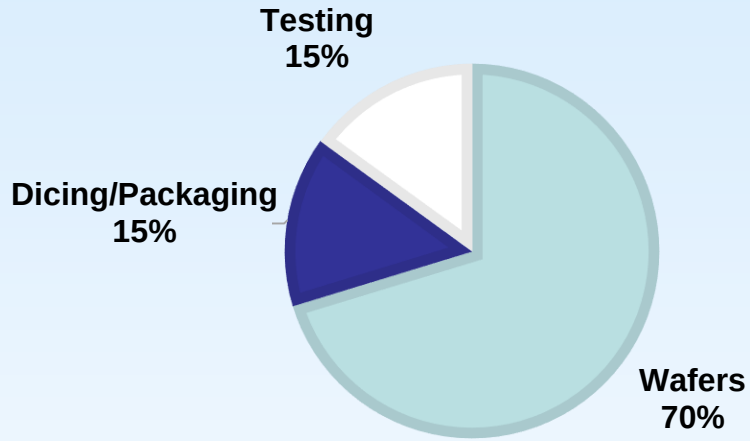
A lesson learnt:
Understand how variations in all parameters, even the “simple” ones, affect the system performance. Simulate and **specify** what can be allowed, so that you have something to test against.

ASIC Cost Breakdown Examples

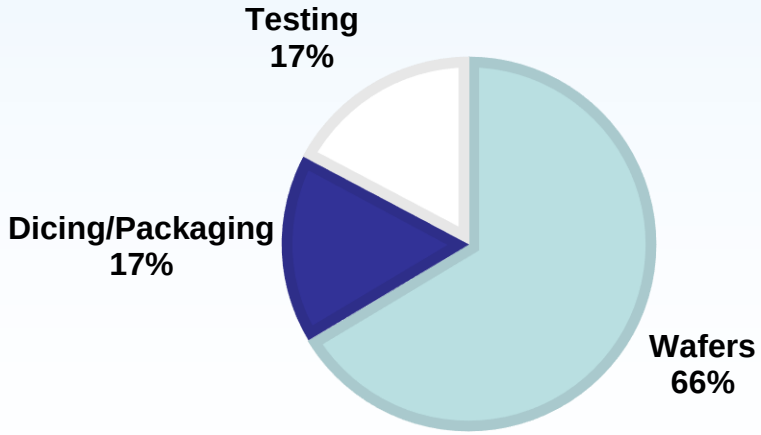
GBTX



GBLD

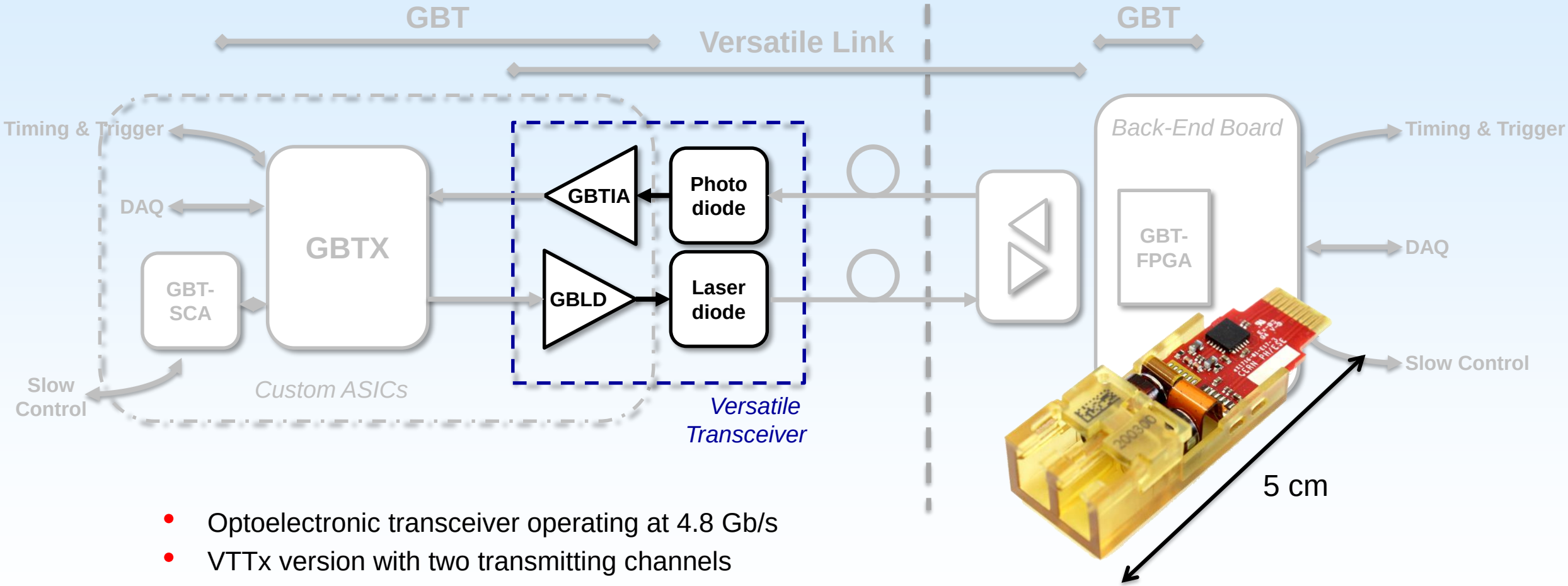


GBT-SCA



- GBT production overall cost: ~2 MCHF

VTRx Production Status



- Optoelectronic transceiver operating at 4.8 Gb/s
- VTTx version with two transmitting channels
- Sources radiation-hard ASICs from GBT project

Versatile Link Project – Planned Timeline

Production planned October 2012

2008				2009				2010				2011				2012				2013				2014				2015			
Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
	Phase 1: Proof of Concept							Phase 2: Feasibility								Phase 3: Pre-prod readiness				MS	Evaluation					IT	Pre	Production			

MS = Market Survey
IT = Invitation to Tender

So, this is a status review after three years of heavy use of VTRx modules?

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	Phase 1: Proof of Concept			Phase 2: Feasibility								Phase 3: Pre-prod readiness					MS	Evaluation					IT	Pre	Production						

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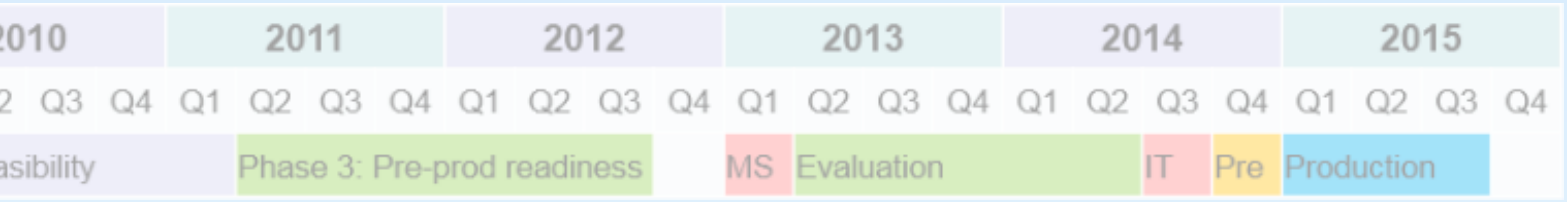
So, this is a status review after three years of heavy use of VTRx modules?

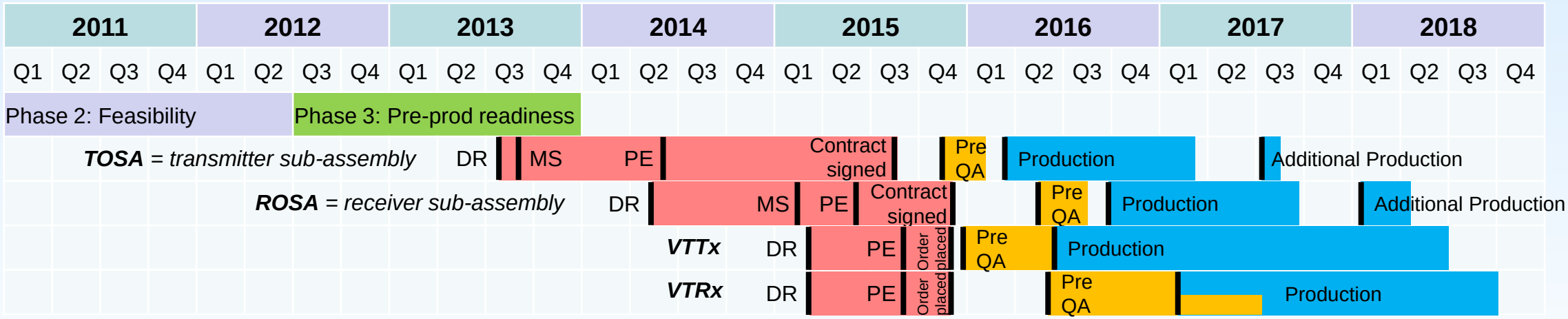
Not quite, but a lot has changed since this plan was drafted:

- VTRx/VTTx total production quantity from 8,900 to 40,000!
- Confirmed users from 4 to 13

…and LS2 was first planned for 2016, then for 2018, then for 2019-2020.

Versatile Link Project – What Actually Happened





DR = Department request
MS = Market Survey
IT = Invitation to Tender
PE = Price Enquiry

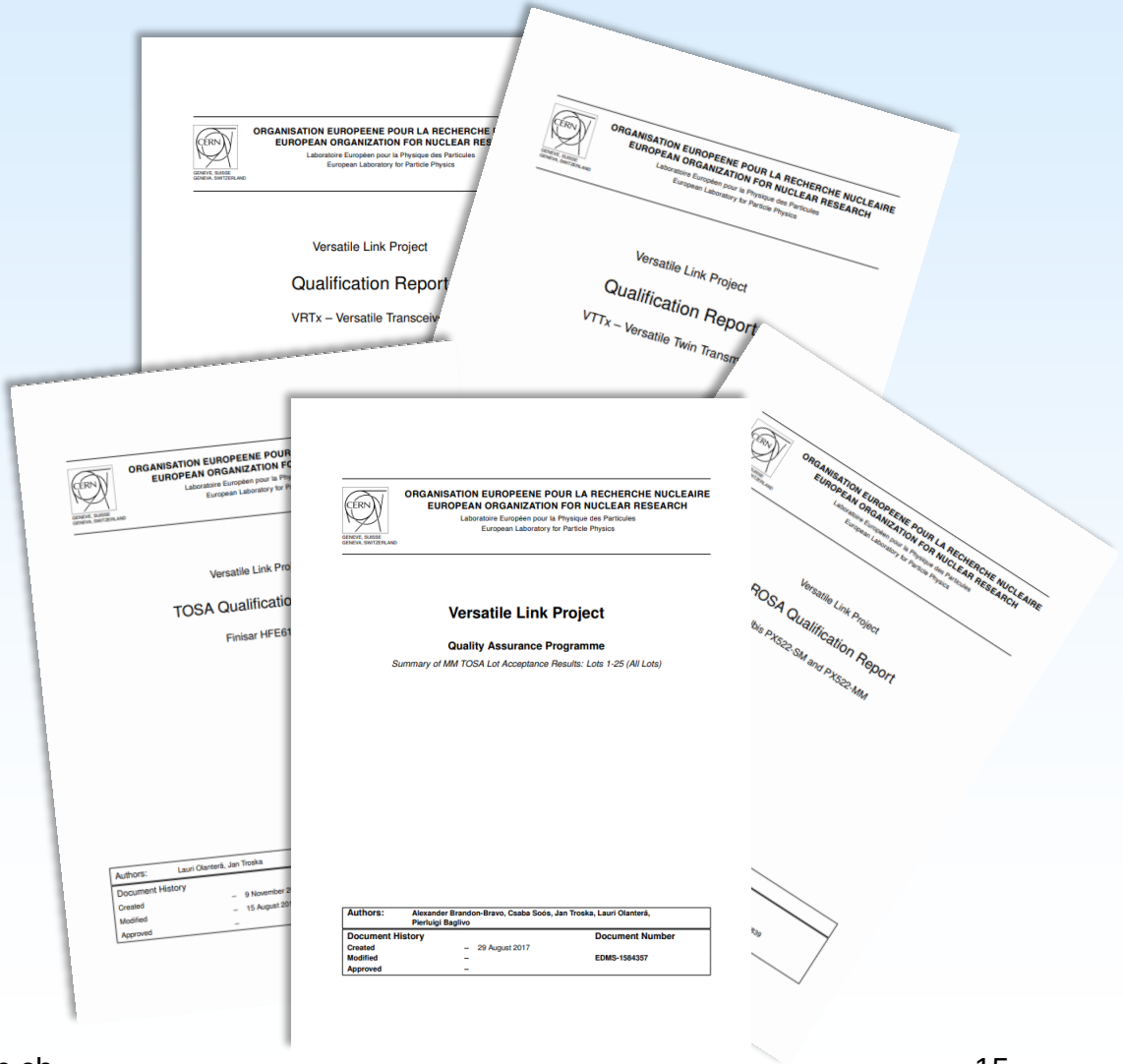
Lessons learnt from this timeline:

- Funding model for common projects needs to be worked out before being able to commit large sums of money
- Commercial actions (in red) can take significant amount of time
- You can't have too much time for QA

What takes time in QA?

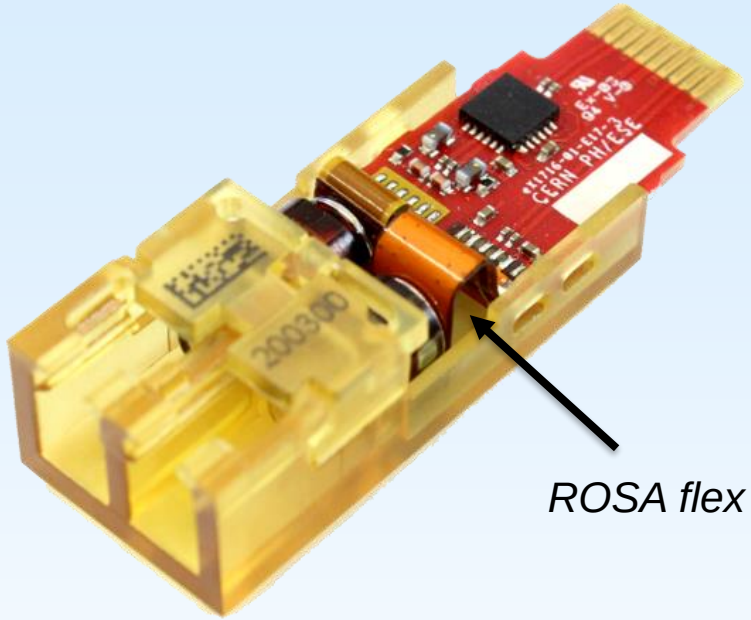
Pre-production Qualification for optical sub-assemblies and VTTx/VTRx modules:

- Functional
  - Room temperature static and dynamic tests
- Temperature
  - Operation across the specified temperature range of -30 to +60°C
- Magnetic field
  - Operation tested in 7 T magnetic field
- Irradiation up to 5×10^{14} n/cm^2
  - Laser and photodiode samples from all production wafers
  - Fully assembled modules
- Module Reliability
  - Temperature cycling: 500 cycles -40 to +85°C
  - High temperature storage test: 2000h in +85°C



Encountered Issue: VTRx pre-series example

- Bad yield due to problems with the receiver side
  - Not acceptable for series production
- Investigations showed that the problem was in the flexible circuit board. Not as flexible as TOSA's.
- Assembly becomes more difficult and the flex is more easily broken when bent.
- A mold had to be developed to guide the flex into the right shape, which minimized variations in the manual assembly process.
- Testing the mold, testing that it really reduced the failures.



A lesson learnt:
Make big enough pre-pre-series with the final parts, so that you understand the difficult steps in the assembly process and have time to modify the process or to change the component specifications.

… or be prepared to have several post-pre-series trials, when small changes may already be expensive.

VTTx/VTRx QA During Series Production

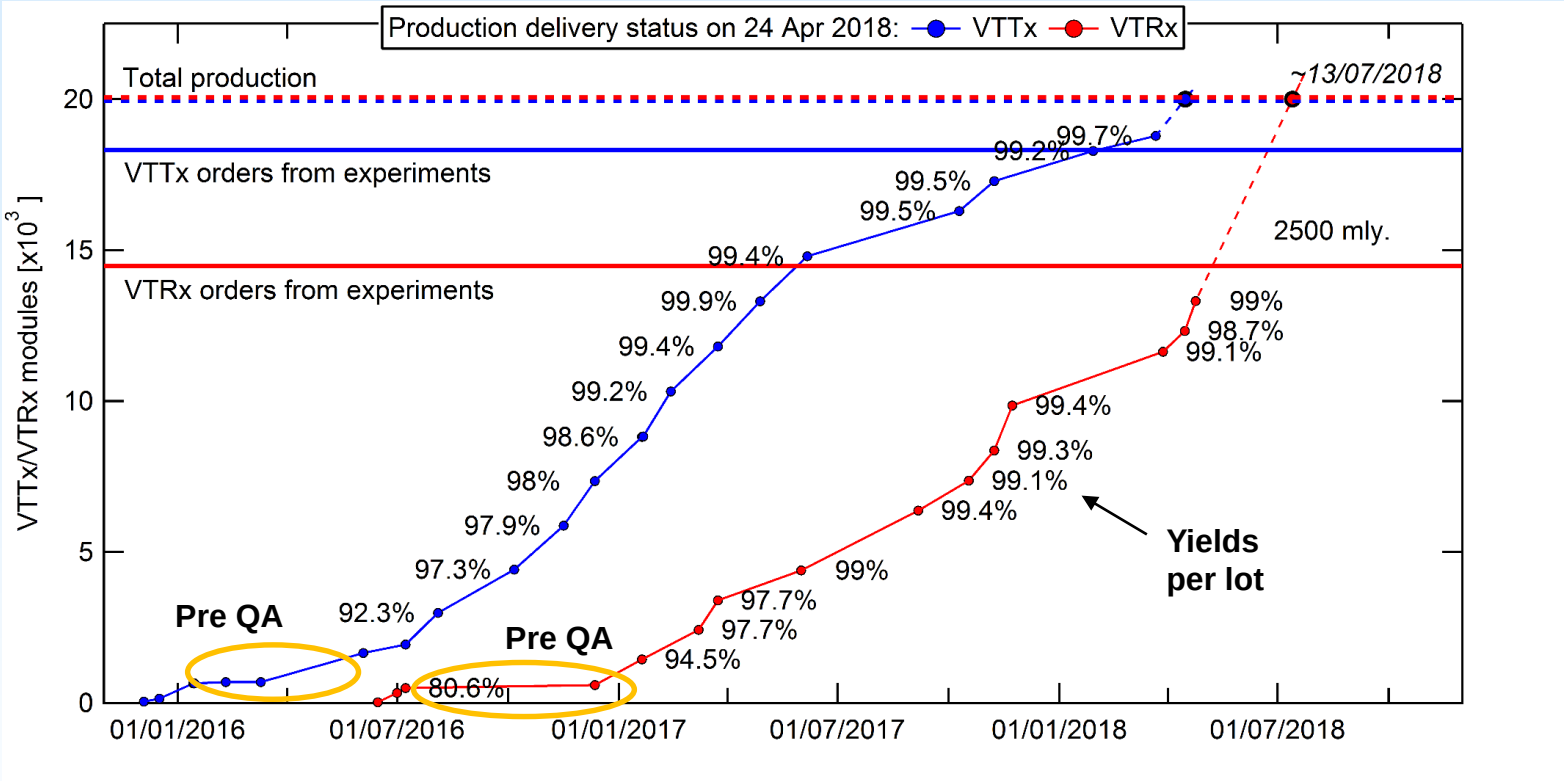
Versatile Link

Reception of component lots → Sampling and acceptance testing → Shipping to assembly house → Module assembly → Production testing → Shipping to CERN → Sampling and acceptance testing → Final packaging

- All assembled modules are tested at the assembly house
- All received component- and module lots go through lot acceptance at CERN
- Some “VTRx testing at CERN” -numbers:
  - TOSA: 64,600 received, **1,361** tested (2.1%)
  - ROSA: 22,976 received, **554** tested (2.4%)
  - VTTx/VTRx: 30,750 received, **1,032** tested (3.4%) so far…
- Lot of unpacking, sampling, testing, packing, labeling, shipping, reporting…

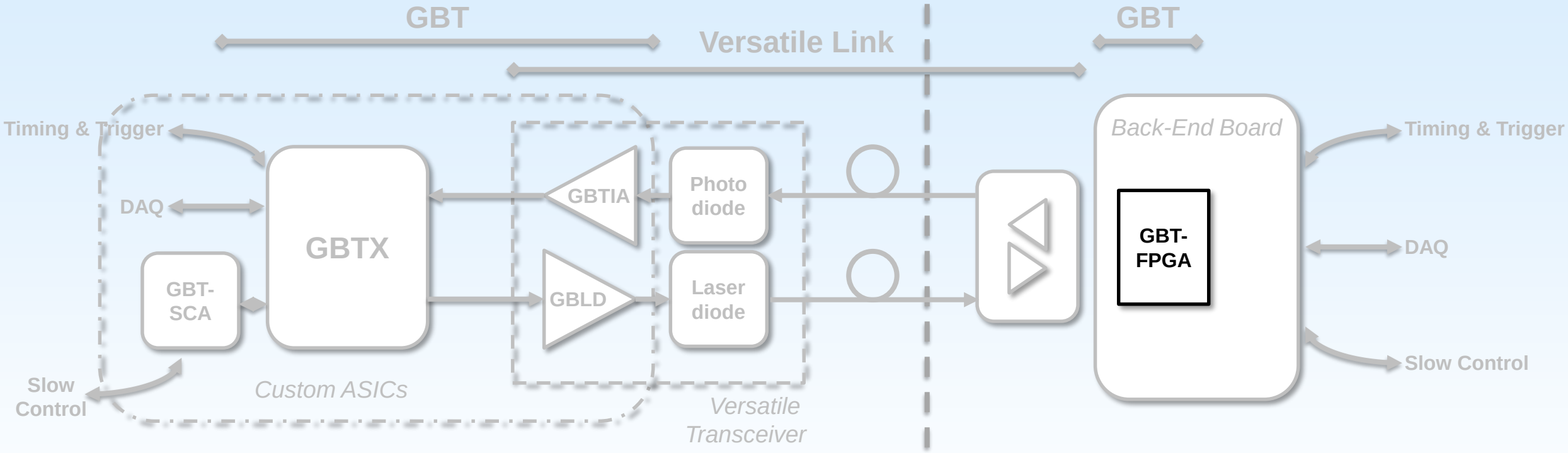
A lesson learnt:
Outsource, or get awesome technical students…
(work represents 1 FTE for the duration of the project)

VTTx and VTRx Production Rate and Yield



- We have reached the ordered quantity with VTTx and about to reach it with VTRx.
- 66% of VTTx orders and 44% VTRx MM orders delivered.
- We have a good stock of modules (>10,000) ready waiting for the users.

GBT-FPGA

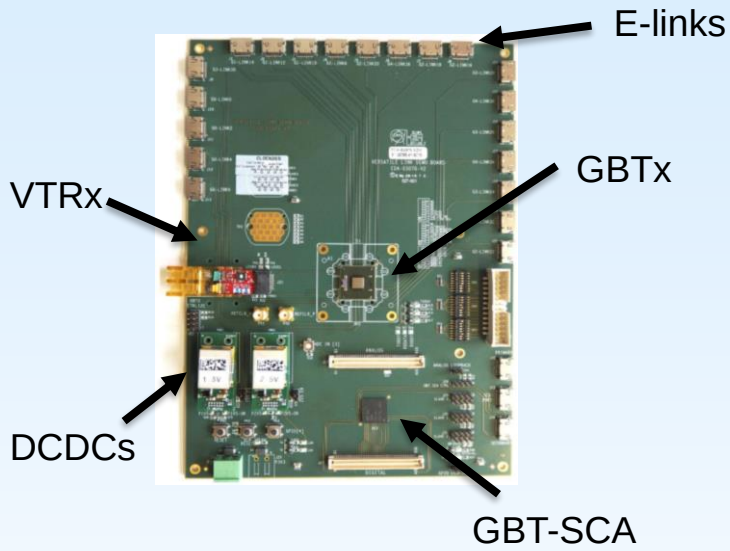


- Gigabit transceiver IP (@4.8Gbs) with encoding
- Targets FPGA from Altera and Xilinx
- Transmits TTC and EC data to the on-detector electronics as well as receives and forwards detector data to the central DAQ

GBT-FPGA

- The GBT-FPGA core development has been completed
  - Latest release 6.0.0 in March 2018 with improvements and bug fixes
  - Very likely the last major release (resources focused now on lpGBT)
- Majority of users access front-end through GBT-FPGA
- Plenty of users for the library
  - ~150 users in the GBT-FPGA user e-group
- A lot of work still goes into the user support

Versatile Link Demo Board (VLDB):



Lessons learnt:

- High level model for front end needed for simulations
  - Especially because the next generation link is not symmetric → no simple loop-backs
- The IP must be as generic as possible
- High performance options, such as optimized latency, require deep FPGA design understanding from the users. Not to think as plug-and-play solutions!

Summary

- GBT chipset production has been completed and we are ready to deliver all ordered ASICs

- Versatile Link production is running smoothly
  - About to reach the ordered module quantities
  - Production will run for few more months

- A lot of valuable experience for the new productions:
  - lpGBT Status and Plans: *Szymon Kulis 14:30*
  - Versatile Link Plus Status and Plans: *Francois Vasey 15:00*

Useful Links

- The GBT and Versatile Link teams have created a forum on GBT chipset and Versatile Link, allowing **users to exchange views and experience** related to GBTx, GBT-SCA or VTRx:

  GBT-VL-forum@cern.ch

- GBT support:

  https://its.cern.ch/jira/projects/GBTSUPPORT

- More information about the projects can be found from:

  https://espace.cern.ch/GBT-Project/

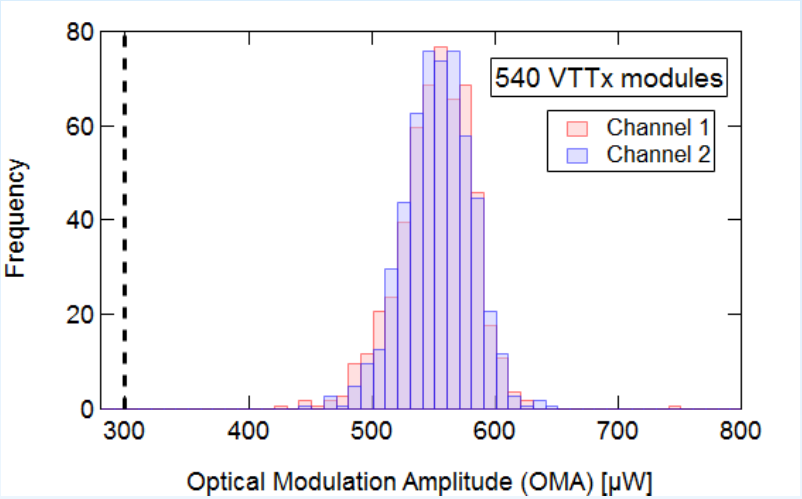
  https://espace.cern.ch/project-versatile-link/public/

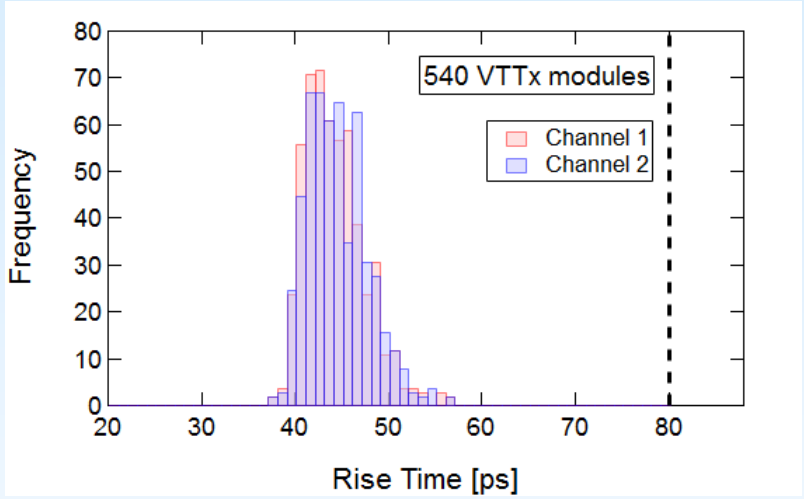
- How to order GBT & Versatile Link components:

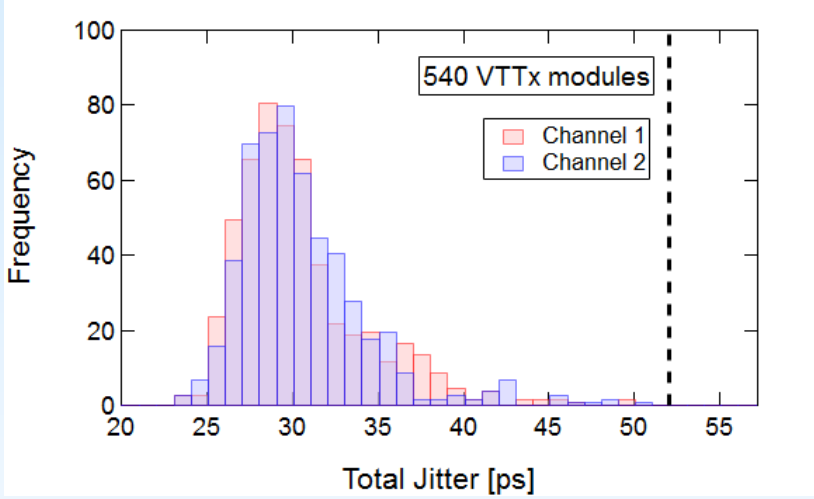
  https://ep-ese.web.cern.ch/content/gbt-versatile-link

Lot acceptance data examples

- The main transmitter side parameters from VTTx lot acceptance tests (94% completed production):







- Sensitivity and total jitter as examples of receiver side performance. VTRx lot acceptance (58% complete production):