



University of Glasgow | Department of  
Physics & Astronomy



# High Speed Links on low Mass Cables

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ACES WORKSHOP AT CERN

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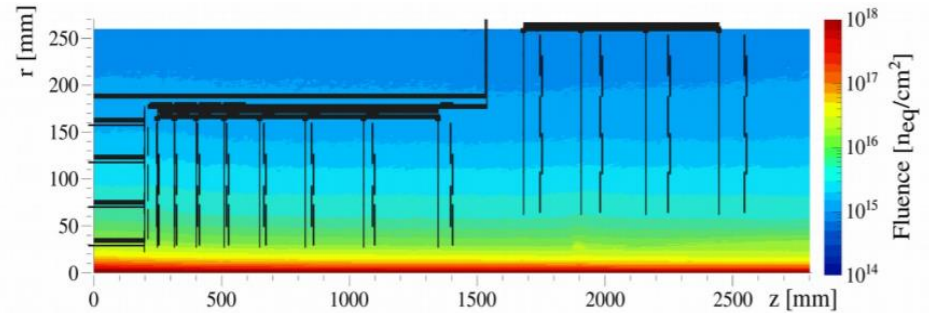


- **Introduction**
- **CMS system overview**
- **ATLAS system overview**
- **High Speed Low Mass cable designs and measurements**
- **Summary**

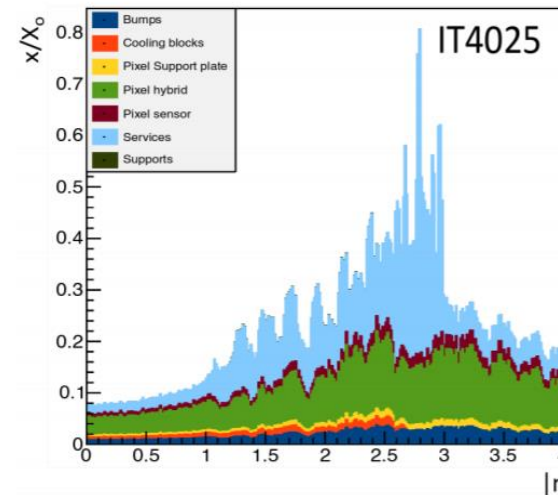


- With the current upgrades in the LHC detectors in order to achieve higher luminosity vertex and tracking subdetectors of HEP experiments will deliver data rates in the Gigabit orders
- The commercial solution to deal with such high rates for long distances will be: Data transmitted optically
- However Physics solution: Due to the high radiation environment and low radiation length requirements electrical transmission with custom designs needed
  - In low radiation regions the transmission is done optically (strips)
- This talk will present the different solutions chosen by the two Upgrades programs of ATLAS and CMS pixels to succeed in this issue

- **High-data rates**
  - More current per FE chip so more cooling needed
- **Very high radiation levels:**
  - Up to  $2.3 \times 10^{16} \text{ n}_{\text{eq}}/\text{cm}^2$
  - Choice of technologies and materials
- **Material budget considerations:**
  - Direct impact on tracking performance

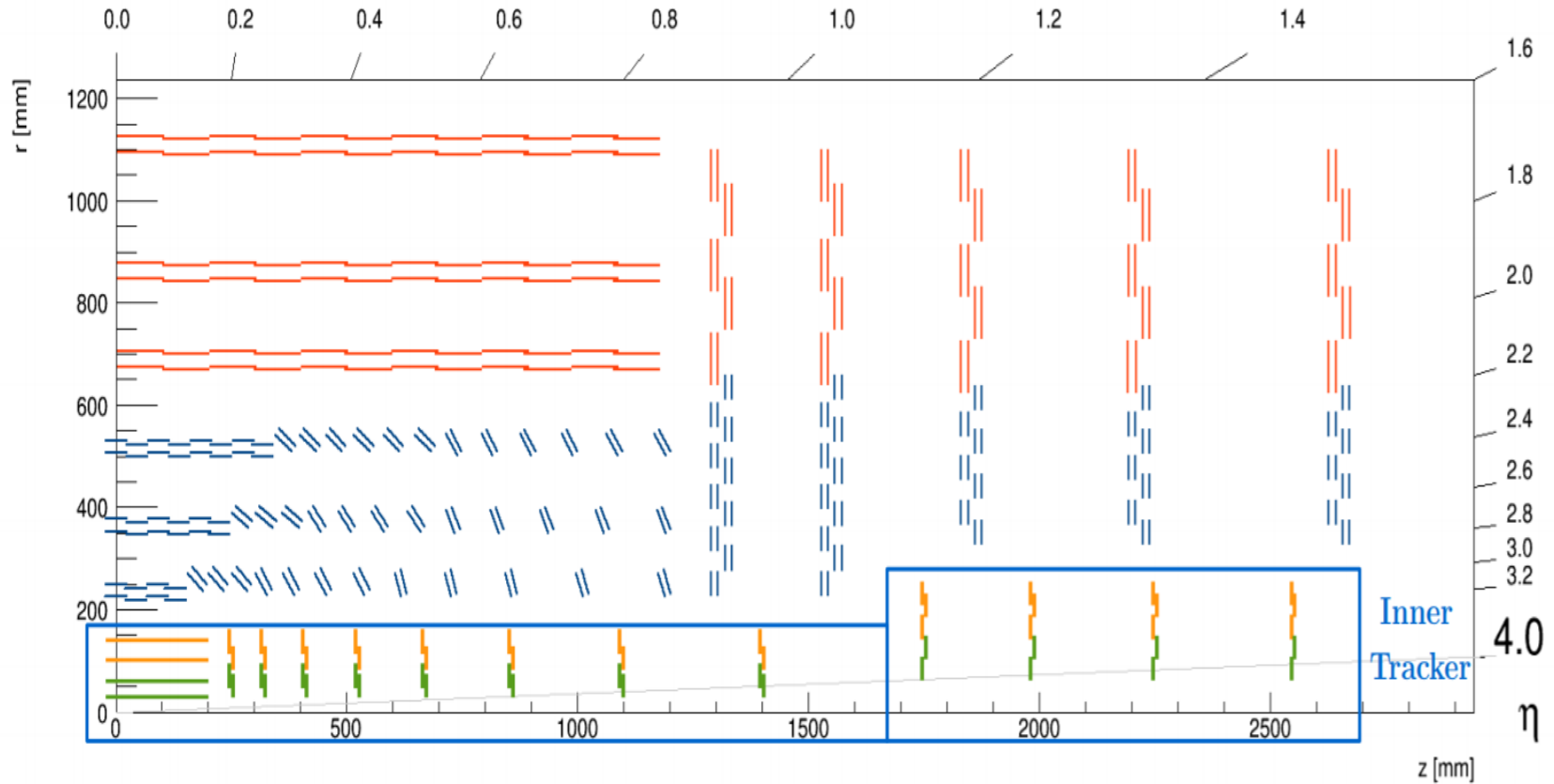


Integrated particle fluence in 1 MeV neutron equivalent in silicon per  $\text{cm}^2$ , for the region of the CMS Inner Tracker. The estimates shown correspond to a total integrated luminosity of  $3000 \text{ fb}^{-1}$  of pp collisions at  $\sqrt{s} = 14 \text{ TeV}$ .



Material budget between first and last active hits in the Inner Tracker, estimated in units of radiation lengths.

## CMS Phase-II Inner Tracker Upgrade

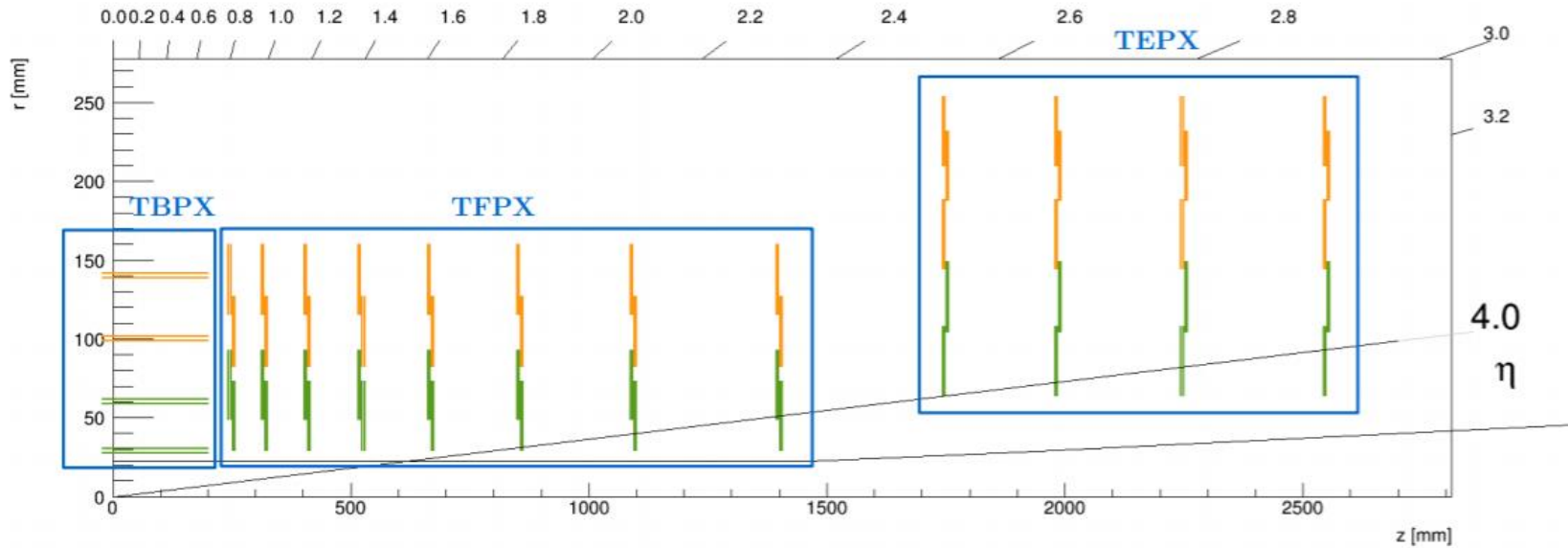


*CMS Phase 2 Tracker layout*



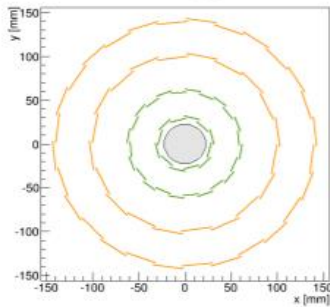


## CMS Phase-II Inner Tracker Upgrade



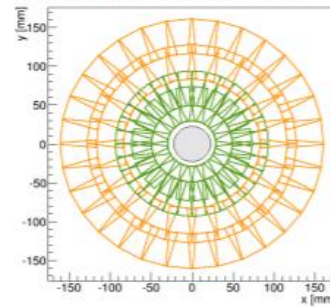
**TBPX**

4 cylindrical layers.  
Arranged in ladders staggered in radius,  $r$ - $\phi$  overlap.



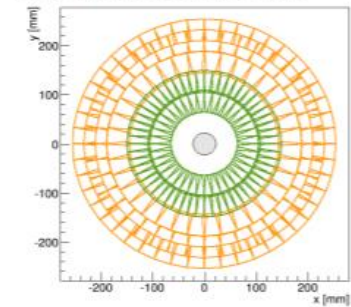
**TFPX**

8 double-disks per (Z) end.  
4 rings per double-disk.







**TEPX**



4 double-disks per (Z) end.  
5 rings per double-disk.



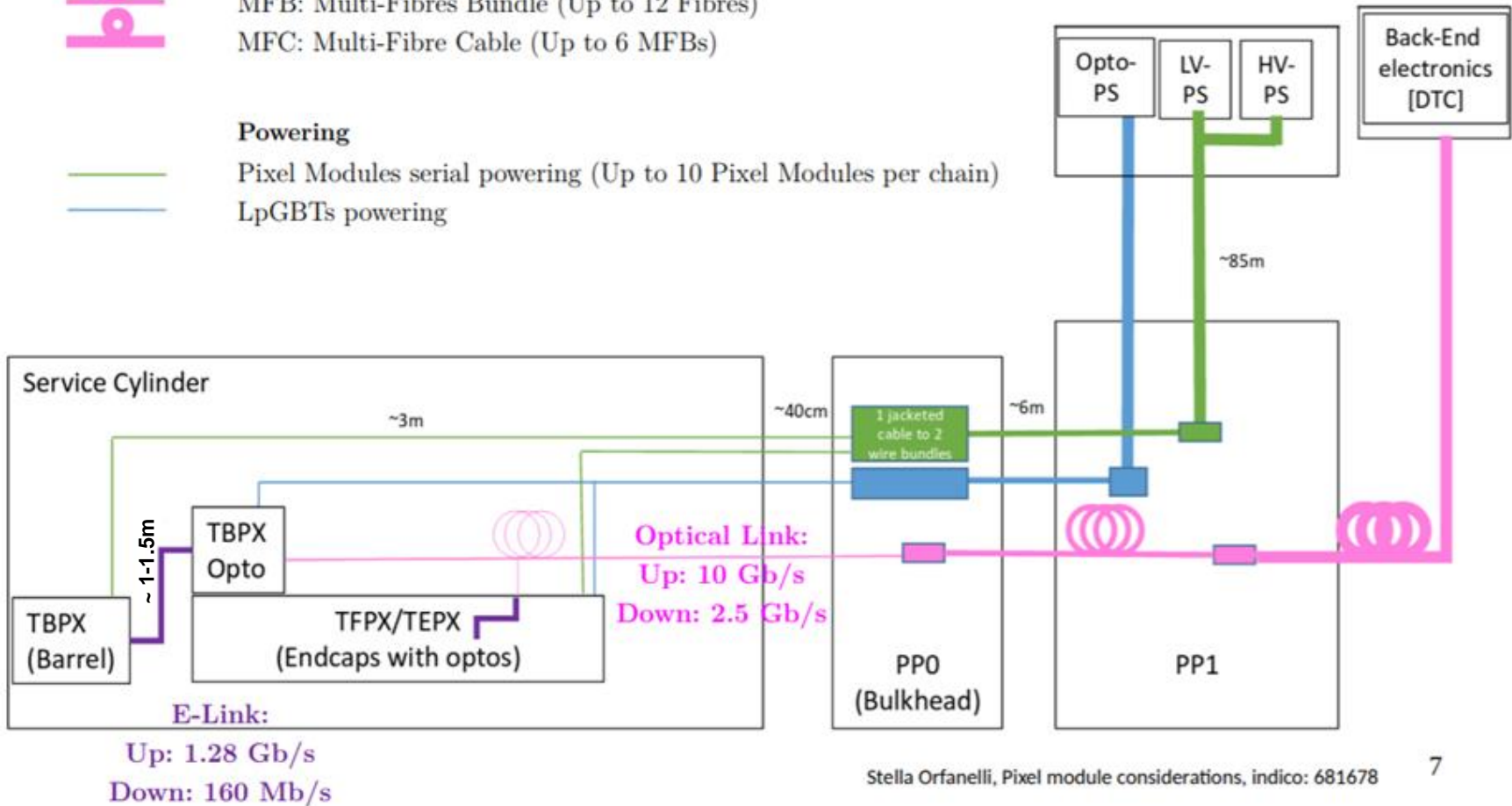
## Readout

-  E-Link (1 Pixel Module is connected to up to 6 E-Links)
-  Optical Fibre (1 LpGBT converts up to 7 E-Links into 1 Optical Fibre)
-  MFB: Multi-Fibres Bundle (Up to 12 Fibres)
-  MFC: Multi-Fibre Cable (Up to 6 MFBs)

## Powering

-  Pixel Modules serial powering (Up to 10 Pixel Modules per chain)
-  LpGBTs powering

## Services cavern





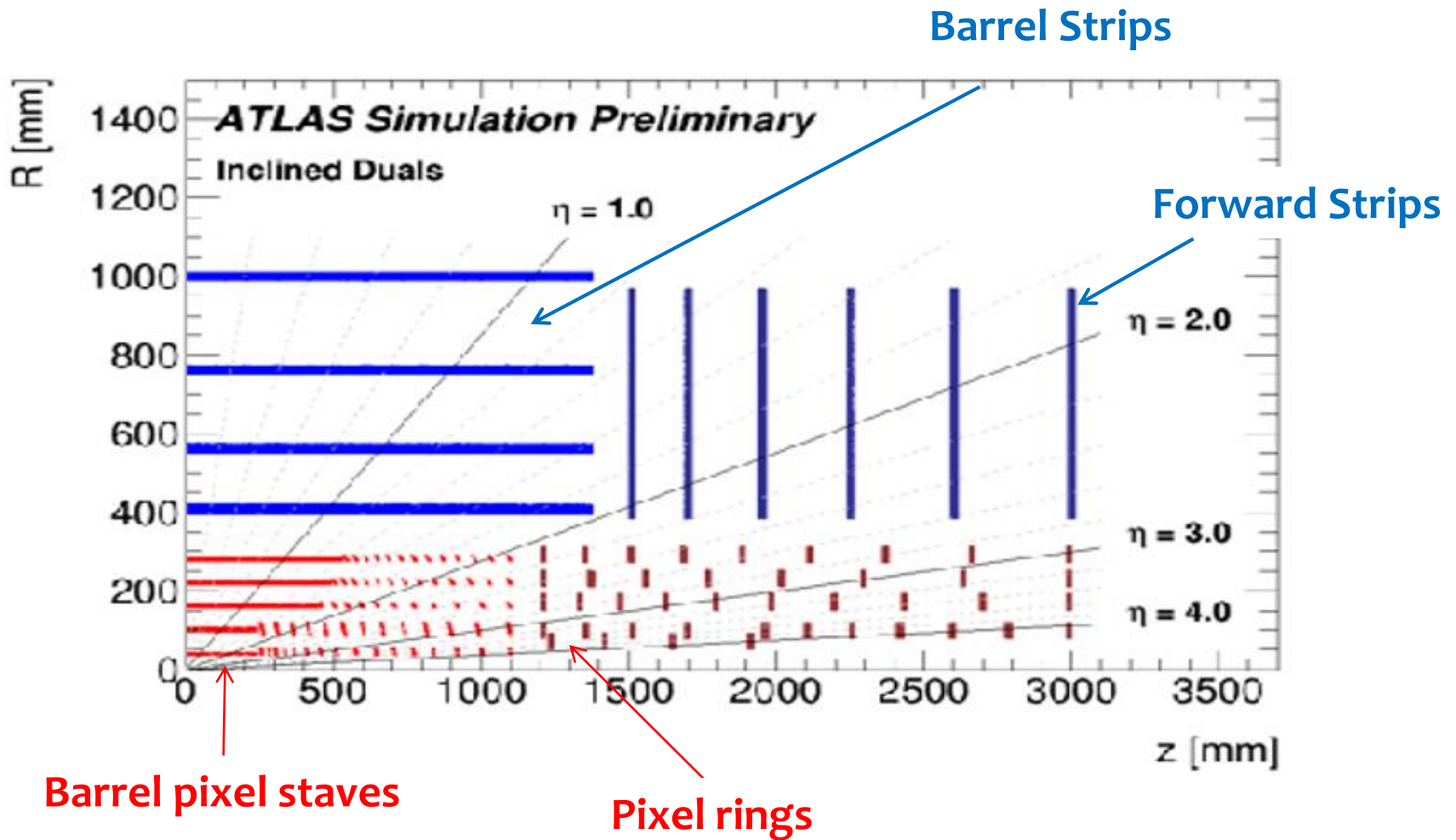
- Bi-directional link: uplink at 1.28 Gbps and downlink at 160 Mbps
- The conversion of readout data to optical links at 10.24 Gbps will be done by LpGBT and it is constrained to the fluence stood by this ASIC (approx.  $1 \times 10^{15} n_{eq}/cm^2$  )
- The conversion of the downlink will be done in the LpGBT from 2.56 Gbps to 160 Mbps
- Therefore the LpGBTs will be located in a support at a higher radius around 200 mm



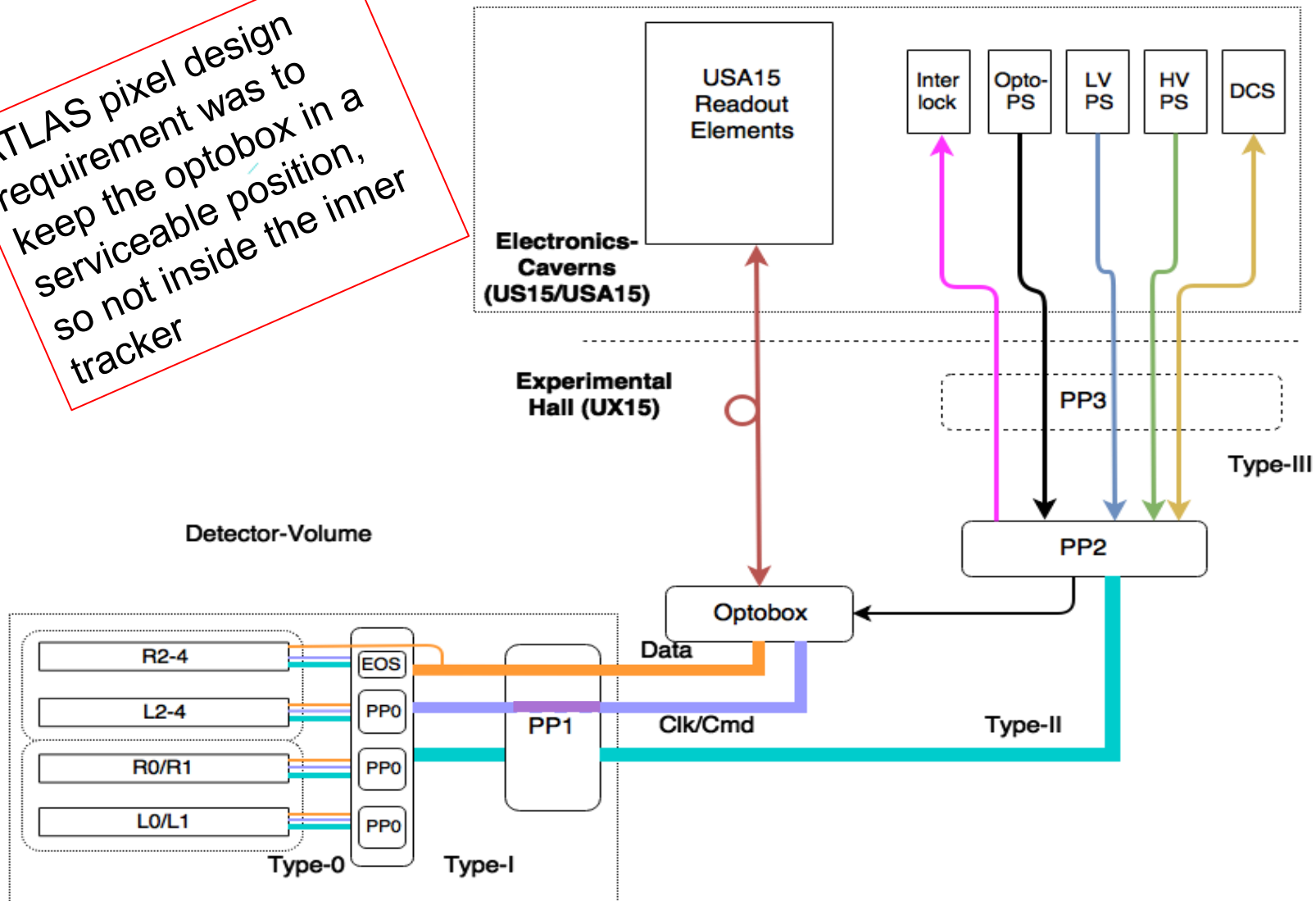


- LpGBTs will drive data coming from one module in the inner layers were they are double chips so will have 3 outputs per FE or from two modules in the outer layers as they are single chips, 3 outputs per module
- The E-links will have to take the data for a short distance approx 1.5m at 1.28 Gbps
  - Research on going to decide what type is the e-link going to be: twinax cable, data flex, etc.
- LpGBT output fiber will be grouped in a MFB bundle that will serve 12 modules in PP0 and in PP1 6 of this MFB will be put together in a MFC

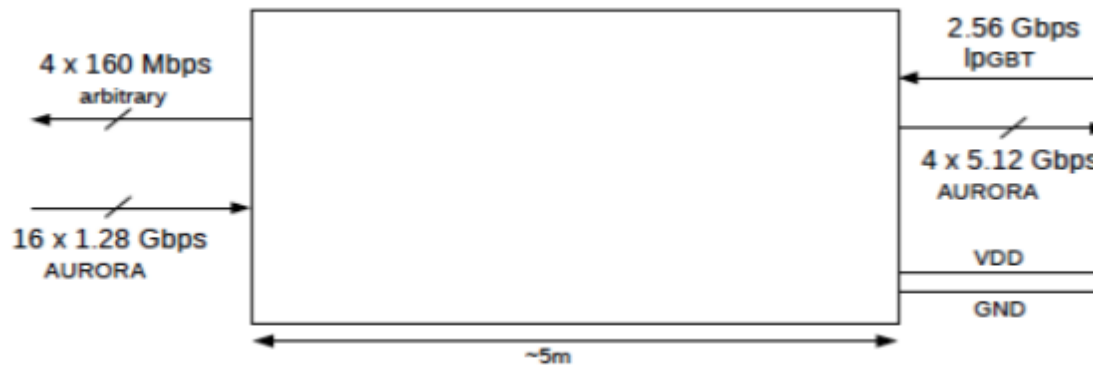
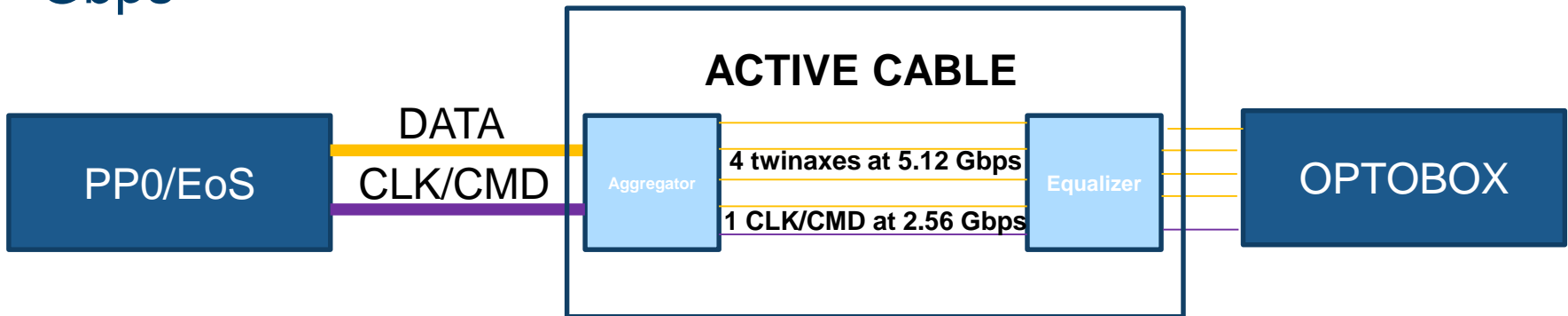
## ATLAS Phase-II Tracker Upgrade



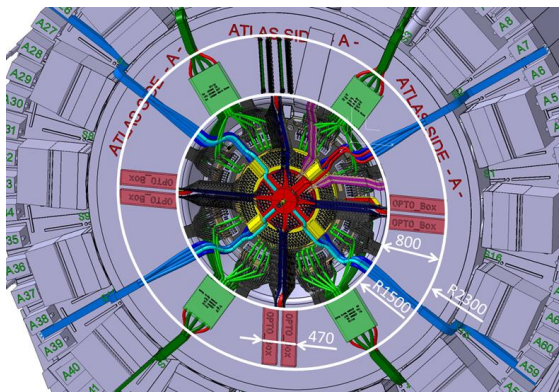
ATLAS pixel design requirement was to keep the optobox in a serviceable position, so not inside the inner tracker



- Connection scheme for the E-Links between PP0 and the Optobox for data transmission
- Bi-directional link: uplink at 5.12 Gbps and downlink at 2.56 Gbps



- Data/ Uplink cables characteristics (cables can be flexes, twinax , or twisted pair):
  - Low mass, low activation, radiation hard and halogen free
  - Able to transmit differential data at max 5.12 Gbps in Atlas (1.28 Gbps in CMS for approx. 1.5m)
  - Fulfil mechanical constraints to fit in the corresponding envelopes
  - Impedance that matches the rest of the electronics (100 ohms and 70 ohms) investigated so far
  - Should fulfil the 20 dB loss requirement in the full link at 3 GHz (ATLAS)



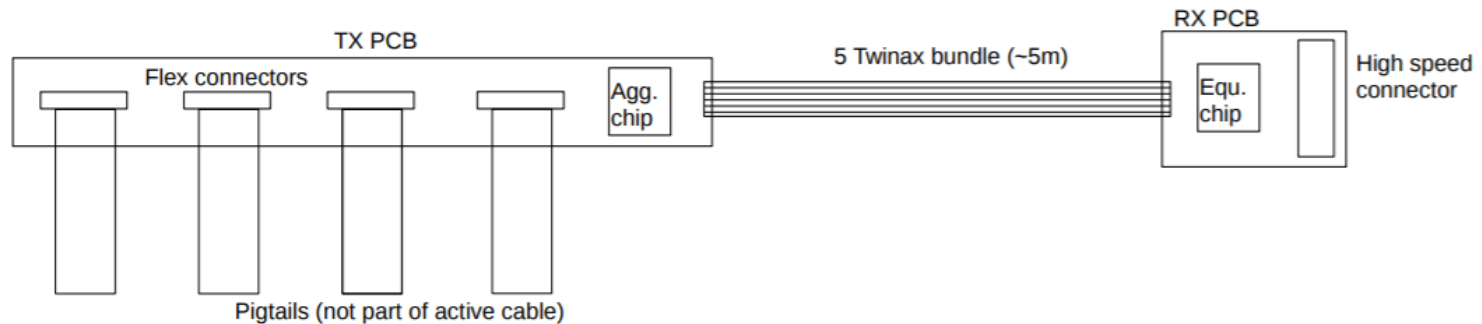
- The optoboxes are at  $\text{PHI} = 0, 90, 180 \text{ and } 270$
- Radius spans like this  $1500 < R < 2300 \text{ mm}$
- Data cable length is 5000mm maximum





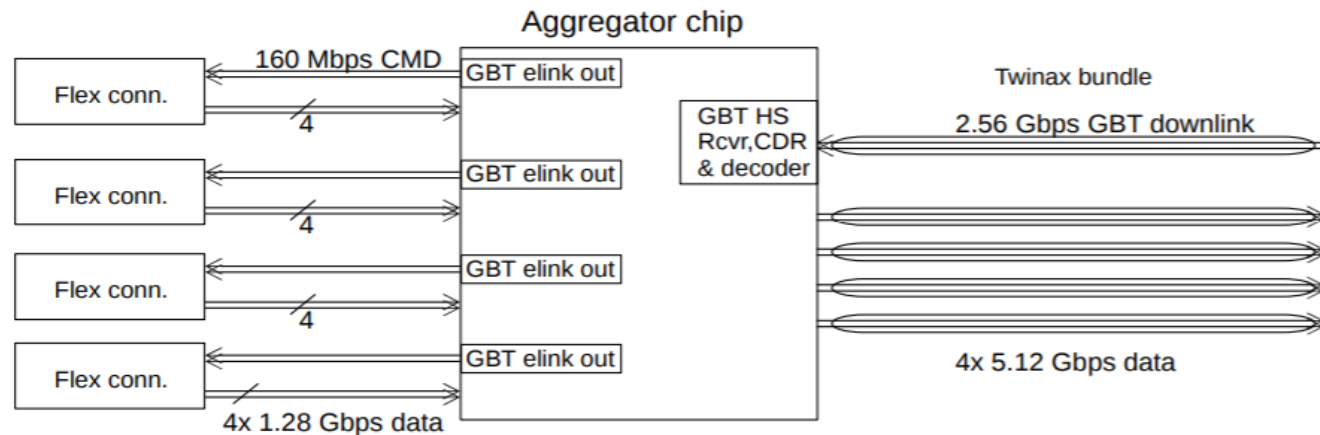
- Several modules will be combined in the optical path and split up in the detector area
- The splitting will happen in the aggregator using LpGBTx chips
- The data input link of the Front-End chip needs to be compatible with the LpGBTx e-link in terms of electrical format and data rate
- Downlink un-broken, following up-link
- Low mass, radiation hard and halogen free
- Should fulfil the 20 dB loss in the whole link
  - Able to transmit differential data at 2.56 Gbps for several meters
  - Single differential pair connection to the module
  - The downlink data is sent to the Front-End chip on the TTC-link
  - The bandwidth for this link will be 160 Mb/s
  - Impedance that matches the rest of the electronics

## Multi-twinax active cable concept

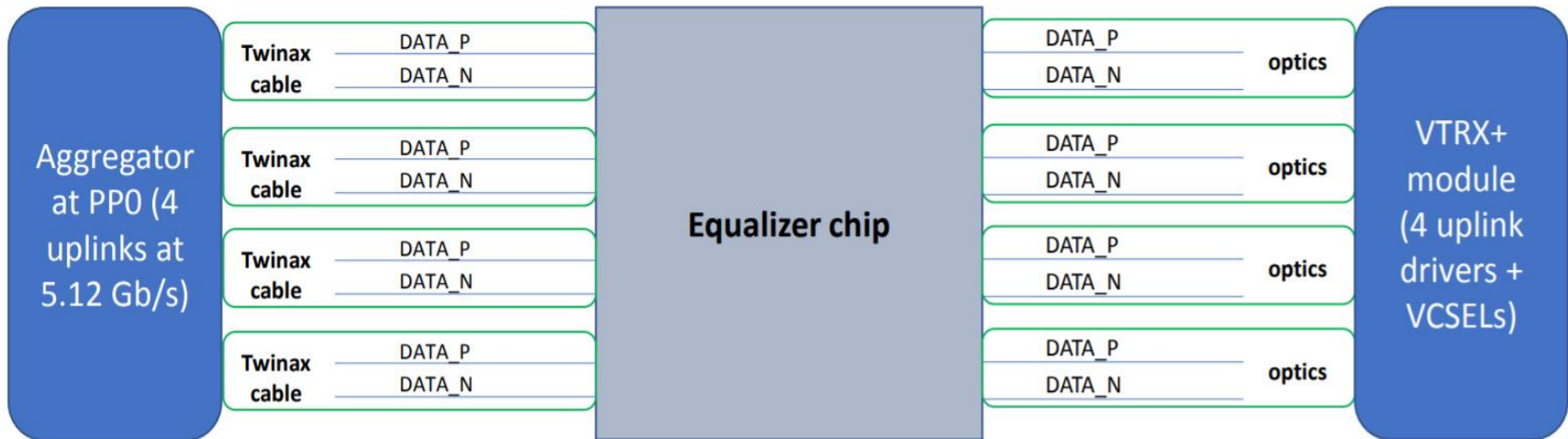


- 1 Down link at 2.56 Gbps, this downlink is shared over several modules
- 4 Up links at 5.12 Gbps each
- Multiple versions of TX PCB to support different parts of detector
- Power to chip? Probably need an extra small diameter cable. Power will run via the optobox
- The TX and RX PCBs will be custom designs and they might serve as PP0
- The equalizer might be located in the optoboard or the carrier board holding the VTRx modules

## Aggregator End



- Aggregator chip: steal down link path unchanged from LpGBT
- Provides low jitter high speed clock needed to drive up links
- Up link protocol likely cannot be that of LpGBT, but studies needed



- The equalizer chip will be located at the optobox side
- There will be one ASIC per active cable
- First prototype end of 2018
- Cable receiver ASIC receives 5.12 Gb/s signal
- CTLE and CDR (for lower jitter) stages included
- Drives signal (at 5.12 Gb/s) to the VTRx+ module inside the optobox.

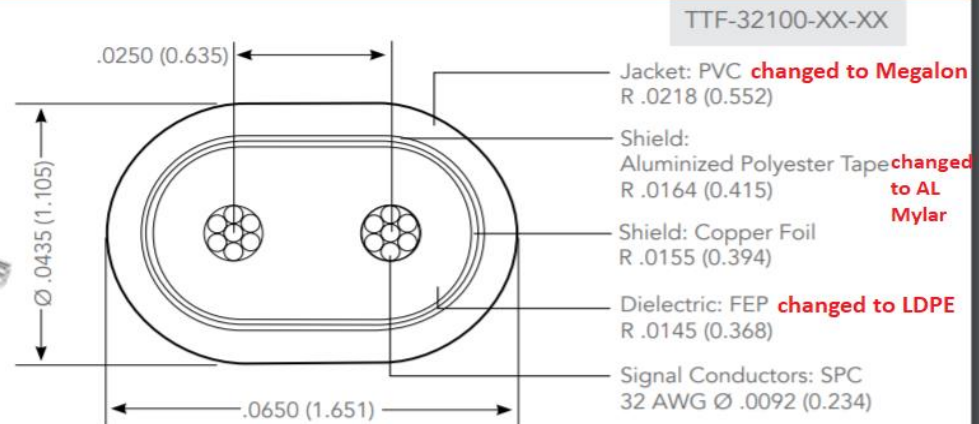


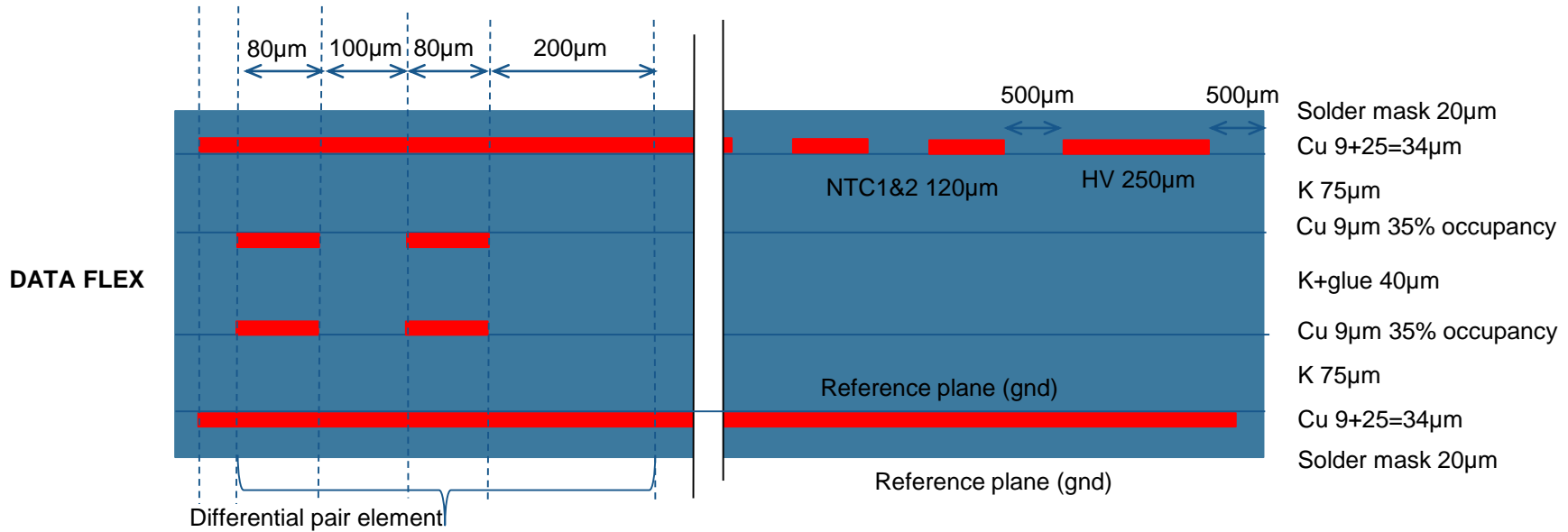
- Why are an aggregator ASIC and an equalizer ASIC needed?
  - Due to the high levels of radiation, 500 MRad, designing a serializer and a CDR with very little jitter working at 5.12 Gbps becomes really challenging. Furthermore traces in PCBs at this speed introduce very high losses in the data link and it is proven that cables perform much better
  - Therefore in order to avoid further complications in the pixel chip, this will have a max data output of 1.28 Gbps and several of this lines will be multiplexed in the aggregator chip to achieve the 5.12 Gbps. Besides we will avoid in the modules traces at this speed.
  - As the distance of the data lines to travel is long, 5m, there is a huge degradation of the information and equalization is required in order to achieve a clean eye diagram and low BER.



- Ongoing discussions with industry to determine the materials we would like to have (rad length) and if the processes to manufacture it in industry are compatible
- Their cable design should perform better than the present Twinax design that has already been tested and was produced by the company Tempflex, now owned by Molex (Thanks to M.Kocian)

## 100 Ω, 32 AWG MICRO TWINAX CABLE



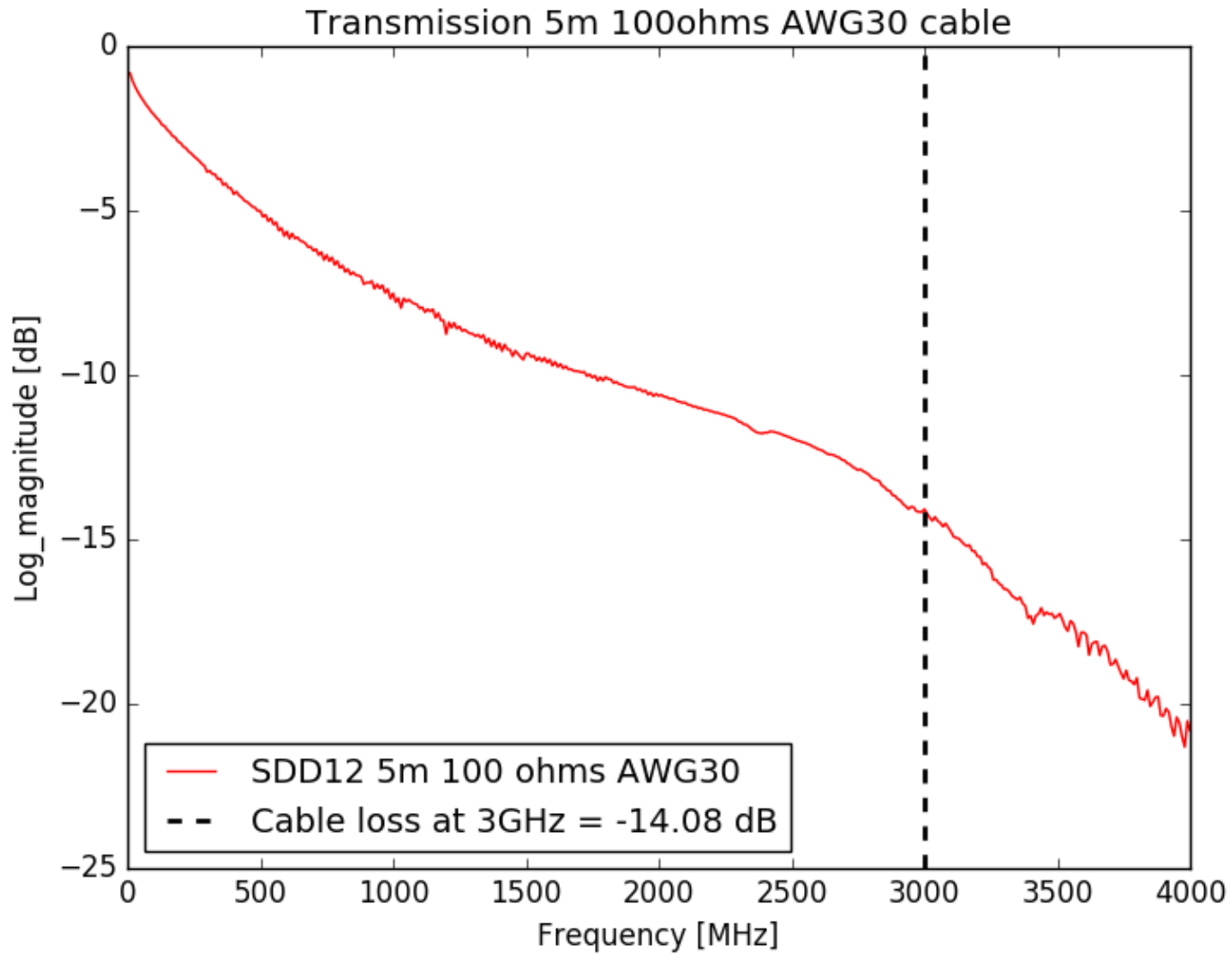


- 4 layers stack up: layers 1 and 4 are ground planes that provided reference to layers 2 and 3 that are the signal layers
- The lines are differential striplines embedded between the two reference planes (1 and 4). This technique allows to control more efficiently the impedance and adds a shielding for EMI
- As a flex (as generally PCBs) is produced with an even number of layers, we took an advantage to embed two layers of signal between the two reference planes

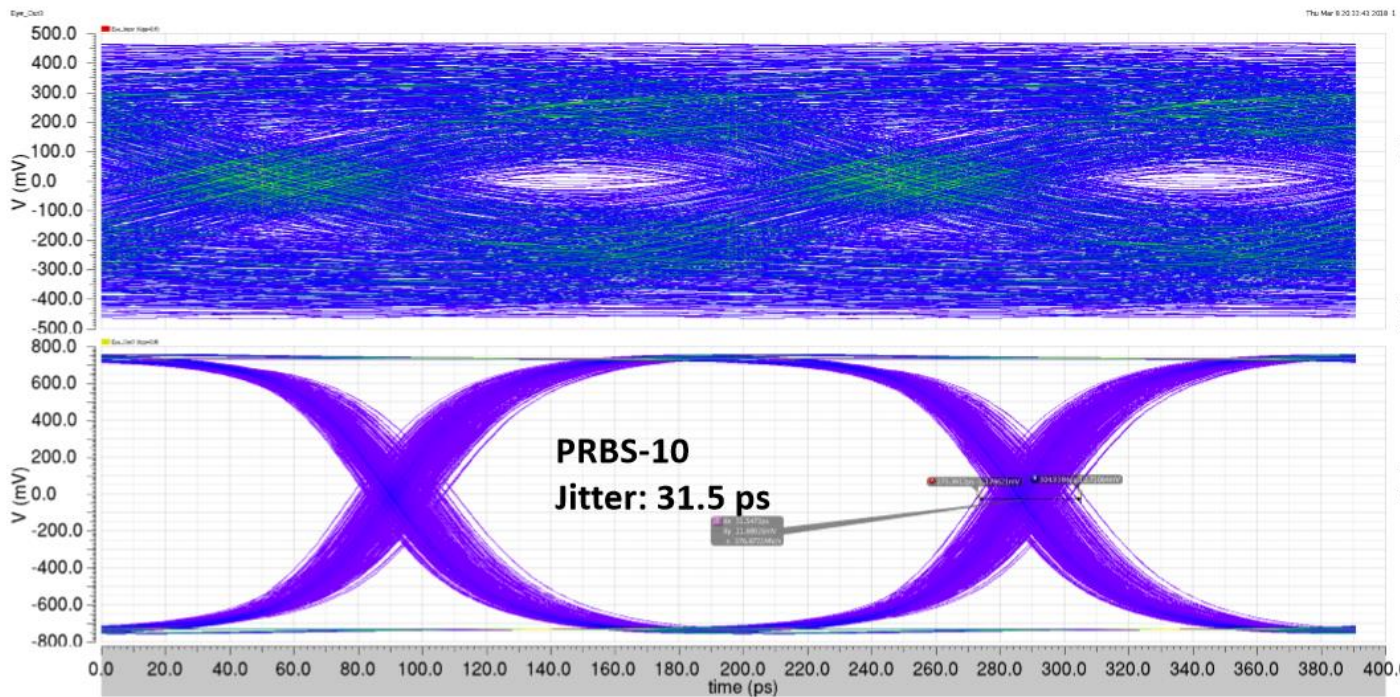


• Recapitulation table of the measurements

Measured by	Cable	Length (m)	dB loss at 3Ghz	dB loss per meter	dB loss for 5m cable
LBNL	28AWG Twinax	6	14	2.33	11.65
LBNL	30AWG Twinax	6	17	2.83	14.15
LBNL	34AWG Twinax	4	20	5.00	25.00
Glasgow	30AWG Twinax	8	19	2.38	11.9
Glasgow	28AWG Twinax	8	16.6	2.08	10.4
Glasgow	34AWG Twinax	8	32	4.00	20.00
Glasgow	36AWG TP_shield	3	12	4.00	20.00
Glasgow	36AWG TP_shield	1	5	5.00	25.00
New Mexico	Stave Flex	1	9	9.00	45.00
New Mexico	Data Flex	1	9	9.00	45.00
New Mexico	Stave Flex + 6m 30AWGTwinax	7	25	3.57	17.85



- Equalizer behaviour simulation modelling a cable with the s-parameter of the previous slide
- Voltage input 1.2 V and signal type PRBS10
- Voltage swing and jitter levels at the output still to be verified with versatile link plus although less than 50 ps is a good sign



- The jitter was 31.5 ps after updating the model with a 1.2 V PRBS-10 input.
- Results are sensitive to the cable's model, signal swing, and the circuit parameters.
- The CDR succeeding the equalizer would mitigate this issue

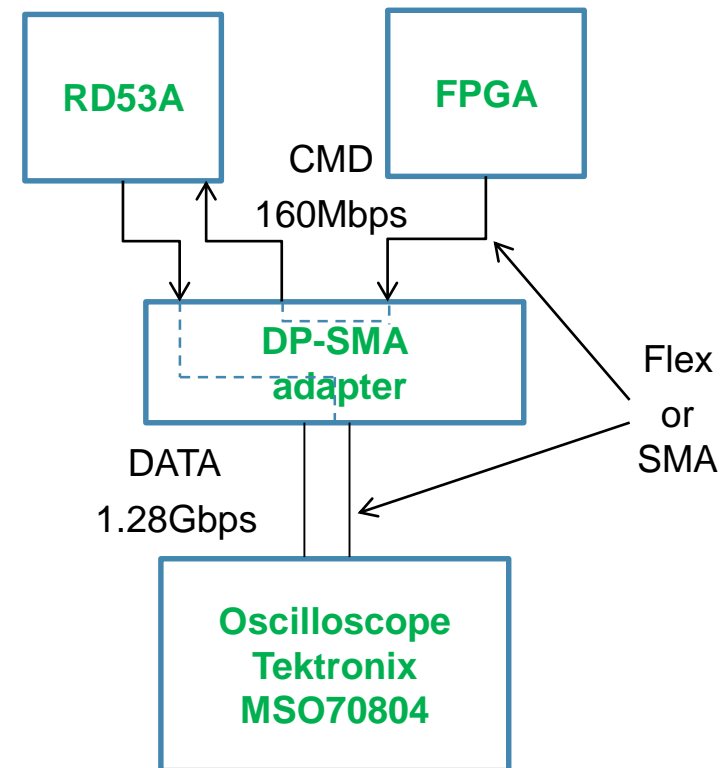


## • First results of flex testing with RD53A

**Preliminary Results**

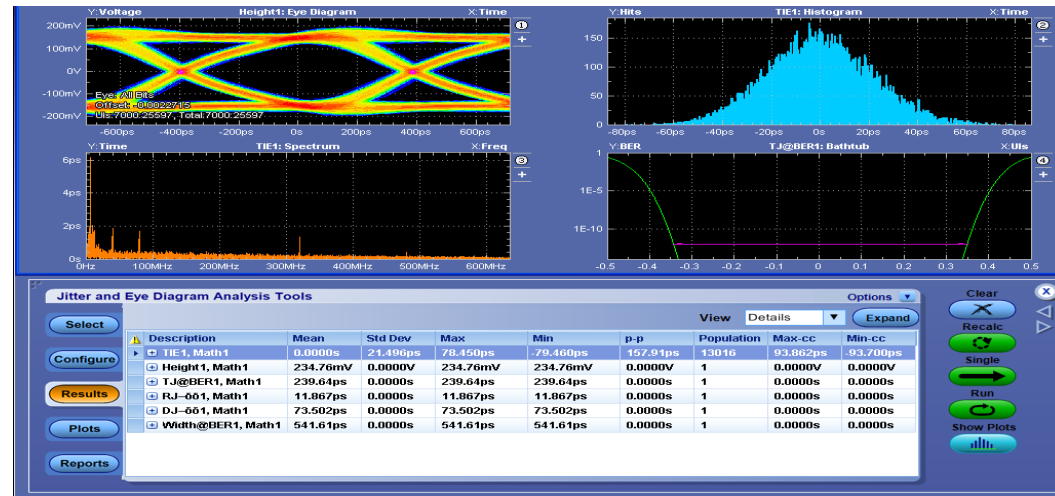
- Signal quality measurement using Tektronix DPOJET package
- Used RD53A chip was FIB edited in order to fix a design bug, which degraded jitter performance. Signal quality of RD53B should be similar (or better) than with this correction

DP-SMA adapters are needed to drive RD53A from FPGA (CMD signal) and at the same time send RD53A output via Flex/SMA to oscilloscope



- RD53A running on default settings, except CML output driver and pre-emphasis settings (still not fully optimized)
- CMD (160Mbps RD53A input) send through SMA cable
- Very preliminary results as this measurement was done a couple of days ago in the lab and more parameters need to be considered, that is why the eye diagram characteristics are not commented
- Transmission over a prototype flex with the layout described in slide 20
- Further studies completely necessary but promising results

Preliminary Results



- Data transmission with the Upgrades has become a very challenging task and requires a lot of effort from the community to make it possible
- Data cables have become an important percentage of the total material budget so they need to be designed with care
- Milestones: link designs (flexes and cables), ASIC designs (FE chip, aggregator, equalizer, LpGBT), optobox and careful module layout of the data lines
- Testing should guarantee that the degradation of the data is in within the limits that make it recoverable (jitter tolerance, voltage swing, etc.) and testing equipment will be qualified against industrial reports.
  - ATLAS requirement of 20 dB loss over the full transmission chain must as well be fulfilled